ATLAS project	IBL & nSQP Opto-board QA					
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IBL & nSQP Opto-board QA

Prepared by:	*Checked by:*	*Approved by:*
K.K. Gan, R.D. Kass, D.S. Smith, Yi Yang, M. Ziolkowski		

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1 SCOPE OF THE DOCUMENT

This document defines the electrical and optical measurements that will be performed on the components of the opto-board and the associated accept/reject criteria.

2 INTRODUCTION

The existing ATLAS pixel detector has three barrel layers and six disks. In transitioning from the present service quarter panels (SQP) to the new SQP (nSQP) no changes will be made to the detector. Considering the years of successful operation of the opto-boards within the pixel read out system, we see no need to adjust any of the electrical or optical specifications used to construct the existing opto-boards.

To service the outer two barrel layers (L1 and L2) and disks, each nSQP opto-board contains seven pairs of data (DTO1 and DTO2) links and seven clock/command links (TTC). Depending on the occupancy of the link in question, DTO1 may be used alone. To achieve a higher bandwidth, both DTO1 and DTO2 may be used. Because of this, fourteen DTO lines are present on each opto-board. For compliance with the connectivity between the SQP opto-boards and the off detector readout, two flavors of nSQP opto-board must be fabricated. The two flavors are called B-Layer and D-Tall.

The insertable B-layer (IBL) detector will be an addition of a single barrel layer inside the innermost barrel layer of the existing pixel detector. To service this new barrel layer, each IBL opto-board contains sixteen DTO and eight TTC links. For the IBL there is only a single DTO line per data link. Unlike nSQP, only one flavor of IBL opto-board will be fabricated.

Each DTO line contains one VDC (VCSEL Driver Chip) channel driving a VCSEL channel. Each TTC link contains one DORIC (Digital Opto-Receiver Integrated Circuit) channel receiving a signal from a PIN channel. The VDC and DORIC are fabricated in 4-channel arrays. The VCSEL and PIN are 12-channel arrays. For integration of the VCSEL and PIN on the opto-board, the arrays are mounted to a custom package called an opto-pack. Therefore each opto-board contains four VDCs, two DORICs, one PIN opto-pack, and two VCSEL opto-packs. All individual components must be certified to meet their own quality assurance (QA) tests before being mounted on an opto-board. The assembled opto-board must then pass a series of QA tests before shipment to CERN.

3 QA DEFINITIONS OF THE ASICS

3.1 VDC QA

The VDC converts an LVDS input signal into an output current appropriate to drive a VCSEL. There is one control current (I_{set}) per each chip to adjust the modulation current, traditionally called “bright” (on). The control of the bias current of the VCSEL, traditionally called “dim” (off), is internally generated within the VDC and set to 1 mA to ensure fast on/off switching of the VCSEL.

Due to observed high yields, we only perform a simple test of the VDC at 2.5 V. Using a probe station and probe card, a 20 MHz signal is sent to all four channels simultaneously with I_{set} at 0.5 mA and each channel driving a 25 Ω resistor to simulate a VCSEL. The total current consumption is required to be approximately 75 mA. The output of each channel should show a respectable signal and all signals should be similar in amplitudes. This test was proven to be sufficient to produce opto-boards of high yield in the existing detector and so we plan to make no changes to this procedure.

3.2 DORIC QA

The DORIC decodes a bi-phase mark encoded (BPM) signal received by a PIN into clock and command LVDS signals. Like the VDC, due to observed high yields, we only perform a simple test of the DORIC at 2.5 V. Using a probe station, probe card, PIN array, and a fiber, four independent BPM signals are sent to the four channels of the DORIC simultaneously. The BPM signal corresponds to a data bit for every 16 clock cycles. The PIN current in each channel is set to be ~500 µA. The current consumption is required to be approximately 80 mA. Both polarities of the decoded LVDS clocks should have a frequency of 40 MHz and a duty cycle of (50 ± 4)%. The clock signals are also required to have approximately the expected amplitude. Similarly the decoded command signals should have the correct data structure, 1 in 16, with approximately the expected amplitude. This test was proven to be sufficient to produce opto-boards of high yield in the existing detector and so we plan to make no changes to this procedure.

4 QA DEFINITIONS OF THE OPTO-BOARD

An assembled opto-board must pass the optical and electrical QA listed below.

4.1 OPTO-ELECTRICAL QA

The measurements that must be performed on an opto-board after the burn-in and thermal cycling are listed in Table 1. All measurements are taken with VVDC set to 2.5 V with the PIN currents listed referring to the current amplitude. The results on the optical power measurement must be stored in the production data base (PDB). This will result in the pass/fail tests listed in

Table 2.

Table 1: Opto-board measurements.

Test	Item	Comments
5.1	current consumption	I_{set} = 2.0 mA, 40 Mb/s PRBS @ I_{PIN} = 100 µA, 160 Mb/s PRBS on all DTOs
5.2	optical power	I_{set} = 2.0 mA, 40 MHz on all DTOs
5.3	optical rise & fall time	40 MHz on all DTOs @ I_{set} = 2.0 mA
5.4	recovered clock jitter	40 Mb/s PRBS @ I_{PIN} = 50, 1000 µA, 160 Mb/s PRBS on all DTOs

5.5	recovered clock duty cycle	40 Mb/s PRBS @ I_{PIN} = 50, 1000 μA, 160 Mb/s PRBS on all DTOs
5.6	clock & command common mode level and amplitudes	40 Mb/s PRBS @ I_{PIN} = 100 μA, 160 Mb/s PRBS on all DTOs
5.7	dark current	+10 V
5.8	recovered data BER < $7x10^{-12}$ (no errors in 1 hour of operation)	40 Mb/s PRBS @ I_{PIN} = 50, 1000 μA, 160 Mb/s PRBS on all DTOs
5.9	transmitted data BER < $1.7x10^{-12}$ (no errors in 1 hour of operation)	40 Mb/s PRBS @ I_{PIN} = 50, 1000 μA, 160 Mb/s PRBS on all DTOs

Table 2: Opto-board QA.

Test	Item	Units	Min	Max	Comments
6.1	IBL current consumption	mA	360	400	
6.2	nSQP current consumption	mA	340	380	
6.3	optical power	μW	500	-	change of no more than 20% from the opto-pack QA value
6.4	rise & fall time	ns	-	1	
6.5	jitter	ns	-	1	
6.6	duty cycle	%	46	54	
6.7	clock and command +/- common modes	V	0.9	1.5	
6.8	clock and command +/- amplitudes	V	0.2	0.5	
6.9	dark current	nA	-	36	
6.10	bit errors (in transmitted and recovered data)	-	-	0	