10 Gb/s Radiation-Hard VCSEL Array Driver

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Outline

- Introduction to a compact solution
- Results with 5 Gb/s VCSEL array driver
- Design of 10 Gb/s VCSEL array driver
- Summary
Use of VCSEL Arrays in HEP

- Widely used in off-detector (no radiation) data transmission in high energy physics (HEP)
- First on-detector implementation in pixel detector of ATLAS
  - experience has been positive
    - compact and robust
    - opto-links built by OSU have ~0.1% broken links
  - use arrays for the replacement optical links for current 3-layer pixel detector and new inner layer (IBL) (160 Mb/s)
- Currently designing 10 Gb/s VCSEL array driver
  - aggregate bandwidth of 120 Gb/s for 12-channel array
Radiation Hardness of 5 Gb/s Array Driver

- Have fabricated a 12-channel VCSEL array driver
  - 4.5 mm x 1.5 mm ASIC fabricated in 130 nm CMOS
  - LVDS signals from the inner 8 channels can be steered to any of the 4 outer channels designated as spares
  - 8 bit DAC per channel for setting modulation current
  - Global 8 bit DAC for setting bias current

- All channels work at 5 Gb/s with bit error rate (BER) < 5x10^{-13} with all other channels active

- Performed an irradiation at LANL with 800 MeV protons to 0.92x10^{15} 1 MeV n_{eq}/cm^{2}
  - 2 chips irradiated (powered)
Irradiated 5 Gb/s Array Driver

- ASIC still works at 5 Gb/s but degraded jitter performance
10 Gb/s VCSEL Array Driver

- 4-channel test chip (65 nm CMOS) submitted early October
- Use only core transistors to achieve maximum radiation-hardness
- 8 bit DACs to control the VCSEL modulation and bias currents
  - Single event upset (SEU) tolerant registers to store DAC settings
10 Gb/s VCSEL Array Driver

- Negative VCSEL cathode bias provides voltage overhead
- Four separate channels with different VCSEL driver and differential receiver topologies
  - Guide in tuning and selecting preferred topology for design of 12-channel ASIC
CML Receiver

- Channels 1-3 have a current mode logic (CML) receiver
  - Commonly used in commercial 10 Gb/s links
- CML receiver is a four-stage limiting amplifier
- Each stage is a common mode feedback amplifier with feed forward capacitors on the input differential pair to enhance the higher frequency signal components
- Channel 3 employs inductive peaking at last stage
CML Receiver (continued)

- Consumes 43 mW (36 mA @ 1.2 V)
- Eye diagram from extracted layout is wide open

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LVDS Receiver

- channel 4 has an LVDS receiver
  - implemented to reduce link power consumption
  - consumes 36 mW (30 mA @ 1.2 V)
- eye diagram from the extracted layout is wide open
VCSEL Driver

- VCSEL current is set by two transistors
  - One with constant bias
  - Second biased by a capacitive feed forward of the negative half of the differential input signal
- Creates pre-emphasis and improves VCSEL current rise/fall times

![Diagram of VCSEL Driver](image)
Complete VCSEL Driver Channel

- Active layout is 125 $\mu$m x 125 $\mu$m
  - long 50 $\Omega$ transmission lines to transmit CML/LVDS across chip
- Driver consumes 18 mW (15 mA @ 1.2 V)
  - full channel is 60 mW
- Open eye diagram from extracted layout including pad, wire-bond, and VCSEL parasitics
8 Bit DAC

- Scaled from existing 130 nm design
- Use external reference for the prototype
  - CERN bandgap reference IP should be available soon
- Consumes 270 $\mu$A @ 1.2 V
- Output sweep is non-linear
  - acceptable for our application
SEU Tolerant Registers

- Used to store DAC values for VCSEL modulation/bias currents
  - Design scaled from 130 nm ASIC
- SEU register based on triple redundant dual interlocked cell
- X1 to X4 store data as complementary values
- Requires two sensitive nodes storing the same logic state X1/X3 or X2/X4 to change state at the same time to upset the DICE latch
- Upset probability reduced by separating the drain area corresponding to the sensitive nodes
  - Will be tested in irradiation

Diagram of the SEU Tolerant Registers with dimensions 15 µm x 5 µm.
Summary

- irradiated 12-channel VCSEL array driver
  - ASIC still works at 5 Gb/s but degraded jitter performance
- designed a 4-channel VCSEL array driver
  using 65 nm CMOS process for 10 Gb/s operation
  - design submitted for fabrication in early October
  - will evaluate radiation hardness
  - will implement lesson learned into 12-channel VCSEL array driver