EasyEDA
Digital Circuits

0) A ground is required for the simulator to run. If a ground is not needed in the circuit, just add a ground without connecting it to the cirucit.

1) For the voting circuit, you can use "Logicstate" as the input for each vote and "Logic_Probe" to see if the measure has passed. After pushing the run arrow, the probe should indicate the status of the measure.

2) Use a "Logic Analyzer" to indicate the output of the JK flip-flops (JKFF's). Unlike the standard JKFF in the lab, the JKFF in EasyEAD has the following unusual characteristcs:

- It triggers on the rising edge of the clock instead of falling edge. Add an inverter to the master clock so that it is easier to design the counter.
- Reset (R) and set (S) operate at active high, i.e. tight it high (5 V) if you want it to reset or set the output Q (and Q bar).
- This is the biggest surprise of all (a bug?): Q (Q bar) is high (low) when the JK is just being turn on (t = 0). So the Q bar output is more useful…

3) For the DACs, use "Voltage_Source" to set the input voltages.