HV Capacitor Information

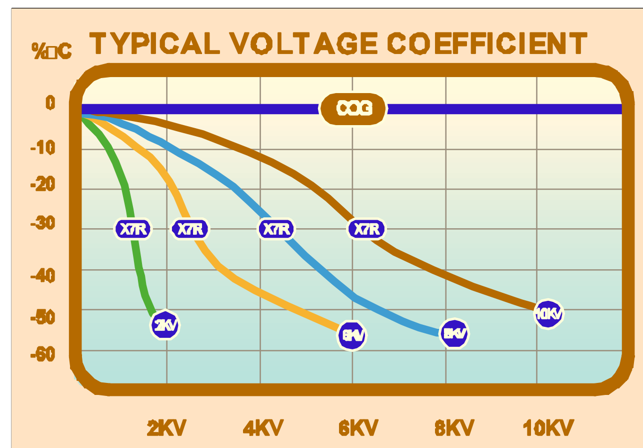
Here is a summary of the information I have collected on HV capacitors. Most of it comes from a view phone calls with engineers at Kemet and Novacap, two manufacturers of ceramic HV capacitors. I also talked to D. Nelson from SLAC.

If you don't want to read all of the following, here is a quick summary:
The manufacturers are confident that their capacitors are very reliable. Reliability increases with voltage and temperature rating. We are considering capacitors rated for 9 KV and 125 degrees C. Our operating conditions are 6 KV and less than 40 degrees C. Furthermore we can choose to have two capacitors (per HV segment) in series which significantly increases reliability since the typical failure mode is a short in the dielectric. The information I have collected suggests that the capacitor failure rate is much below the 1 % failure rates we expect for the tubes.

Dielectric

Our requirements on the ceramic material, i.e. the dielectric are not very demanding. A COG type material would be ideal; X7R would be fine as well.

X7R has a larger temperature and voltage coefficient. For example, a 7.5KV rated X7R capacitor operated at 6 KV will loose ~30-40% of its capacitance. X7R capacitors also age which leads to a further reduction in capacitance. We can address this buy choosing a larger capacitance value to start with but this will usually lead to larger devices. COG capacitors are stable with respect to time and voltage. Here is a plot from the Novacap web site that showing the effects of the different voltage coefficients.



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Here is the definition of aging from the Kemet web site:

Aging" refers to the natural process wherein X7R, X5R, Z5U, & Y5V capacitors exhibit a change in capacitance after their temperature is raised above the Curie point for their particular formulation. (This can happen during soldering, and also during some life or temperature cycling tests.) When the capacitor is heated above the Curie point, a change in the crystal structure occurs, and the capacitance increases. This increase in capacitance is called "deaging." As the temperature is later reduced below the Curie point, the capacitance gradually returns to its previous values. The decline in capacitance is called "aging" and occurs at a rate that decreases roughly linearly with the log of time. Interestingly, the C0G capacitors have a

different formulation which does not display any aging characteristic. Thus, C0G capacitors remain constant with time

Reliability

I discussed reliability issues with an engineers from Kemet. He provided me with an equation that is used by the industry to calculate reliability information at a user selected operating point based on test data obtained at max. voltage and temperature.
This so called PV equation (Prokopoviz and Vaskas) is used predict lifetime at a given temperature and voltage if you have known lifetime data from an accelerated test (higher temp and voltage). Unfortunately, he didn't have test results for exactly the capacitor we are considering but from the information he found he estimated that that the lifetime is >>>15000 h at 125^0 C and the rated voltage (RV). He stressed the much greater (>>>) and that this is conservative estimate (no capacitor failed in their test of 15,000 h).

He provided the PV equation in form of a spreadsheet that I have used to obtain the following information (He suggested to use the generally accepted Ea and n numbers of 1.5 eV and 3 respectively. To increase the reliability of this prediction for our environment we would have to determine Ea and n experimentally for our setup)

Inputs	Variable	Units
n	3	Unitless
Ea	1.5	eV
k	8.60E-05	eV/K
T1	40	C
T2	125	C
V1	6000	Volts
V2	9000	
t2	15,000	h
t1	7,312,664,312	predicted hours

The PV equation

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{1_{abs}}} - \frac{1}{T_{2_{abs}}}\right)\right]$$

t1=time to failure under conditions of interest
t2=time to failure under test conditions (known)
V1=voltage under conditions of interest
V2=voltage under test conditions
n=voltage acceleration exponential
Ea=activation energy
T1=absolute temperature of interest
T2=absolute temperature of test
k=Boltzman's constant (8.6E-5 eV/K)

For a capacitor rated at 9 KV and 125^0 C but operated at 6 KV and 40^0 C the predicted lifetime is > 7 x 10^9 hours. We have 4000 capacitors. Assuming the LST detector runs for 5 years (=43,800 hours) we have only 1.7 x 10^8 part hours.

If we lower the temperature to 25^0 C the predicted lifetime goes up to 1.2 x10^{11} h.
If we lower the voltage from 6000 to 5500, the lifetime goes up to 9.5 x 10^9 h.
These predicted lifetimes are for a single capacitor. If we use two in series the failure rate should be extremely small.

Failure Modes

I tried to collect some information on typical failure modes. Here is what I found:

1. From the Kemet knowledge base (on their web site):
   For chip capacitors, the most common failure mode is low resistance, usually due to mechanical damage, such as a thermal or mechanical crack induced during board mounting or subsequent board handling. For leaded ceramic capacitors, the most common failure mode is a very low resistance or short circuit due to dielectric breakdown, caused by over voltage, transient voltage spikes, severe environmental stress such as thermal stress or thermal shock, or an imperfection in the dielectric.
2. Also from Kemet:

   Are Ceramic Capacitors Reliable?
   Yes, ceramic capacitors are generally quite reliable. It requires much greater levels of voltage to puncture their dielectric than are present in most circuits. Indeed, they have a very high safety margin built in. However, it is important to remember that the SMT chip is a mechanically non-resilient package, and can be mechanically damaged.

   How do Failures Show Up?
   This depends on the circuit. However, the most commonly reported cause of field failures is low insulation resistance, equivalent to high leakage. This low IR is most often due to cracks, although voids in the dielectric occasionally occur. In the case of high energy levels, such damage can lead to catastrophic failure. Lower energy circuits may continue to function for some time, even if the chip has sustained damage.

   Can Damaged Chips be Screened Out?
   In-circuit and functional testers cannot be relied on to guarantee removal of damaged chips, since the initial leakage levels may be very low and difficult to detect in in-circuit and functional testing. As a result, primary emphasis must be placed on capacitor selection and proper application. More information on all failure modes is noted below:

   What are the Most Typical Failure Modes (and Root Causes)?

   Low IR/High Leakage

   a. **Cracks** - These are by far the most common reason for chip failure. Cracks can result in internal ionic conduction or in dielectric reduction through voltage gradient. If a crack occurs in the dielectric, the air gap initially acts as a capacitor, making the damage difficult to detect. However, the voltage stress is concentrated in the area of the crack. This tends to degrade the bulk resistivity, since the dielectric material in the area is chemically reduced via loss of oxygen. Reduced dielectric allows more current to flow, which causes further chemical reduction, and can lead to avalanche of the leakage current over time - particularly when high operating temperatures and moisture are involved.
      i. Mechanical Cracks & Possible Root Causes:
         Board Flex ("45° Signature" Cracks) - board handling after chip solder freezes
         Impact (Board Handling and Tool Impact - ICT, function, depanelization, etc.)
         Pick/place (Z-axis force or centering jaws)
      ii. Thermal Cracks & Possible Root Causes:
         Excessive thermal shock (delta T) in wave
         Improper manual rework and touchup
         Chip microcracks from internal stress
         Chip damage prior to firing by chip supplier
         Glue dots (tensile stress, fulcrum)
         External chip damage
         Inclusions (Fibers, Folded Sheet, Delaminations, Voids)
         Excessive TCE mismatch (worsened by rapid forced cooling, especially on alumina substrates)

   b. **Dielectric voids** - Manufacturing defect in chips - uncommon - usually very low level.

   c. **Surface conduction**
      i. Entrapped flux, cleaners under chip or poor board cleaning in general

ii. External surface contamination ("No clean" systems more critical)
iii. External surface growths (Moisture/voltage generated)
iv. Normal aging - Capacitance decline through the normal aging process. Voltage and temperature changes can also affect the capacitance of EIA Class II & III (X5R, X7R, Z5U, Y5V, etc.) dielectrics.

d. High surge currents, damaging electrode system (uncommon failure mode)

Failure Mode: Intermittents or "opens"

a. Mechanical fracture of chip
(this is more of a problem for chip capacitors which we will not be using)

b. Open/intermittent solder joint due to:
...Tombstoning
...Board solderability
...Chip solderability/tarnish
...Leaching of the chip end metallizations
...Inadequate amount or placement of solder paste
...Narrow/unequal end met areas
...Off-center chip placement
...Inadequate flux activity
...Cold solder (movement during solder freeze)

The engineer I spoke to told me that high leakage current/shorts is by far the most common failure mode (as compared to disconnects). He didn't have a number but he said certainly more than 95% of the failures fall in this category.

Costs

I have a quote from Novacap and expect one from Kemet very soon. There is not much difference between the X7R and COG versions. A high reliability COG type HV capacitor (800 pF, 9 KV) will cost around $4.50. With out the extra screening ("mil specs") it will be around $3.80 per piece. The lead time for all of these is very long: 16 weeks. We will need about 9,000 capacitors.