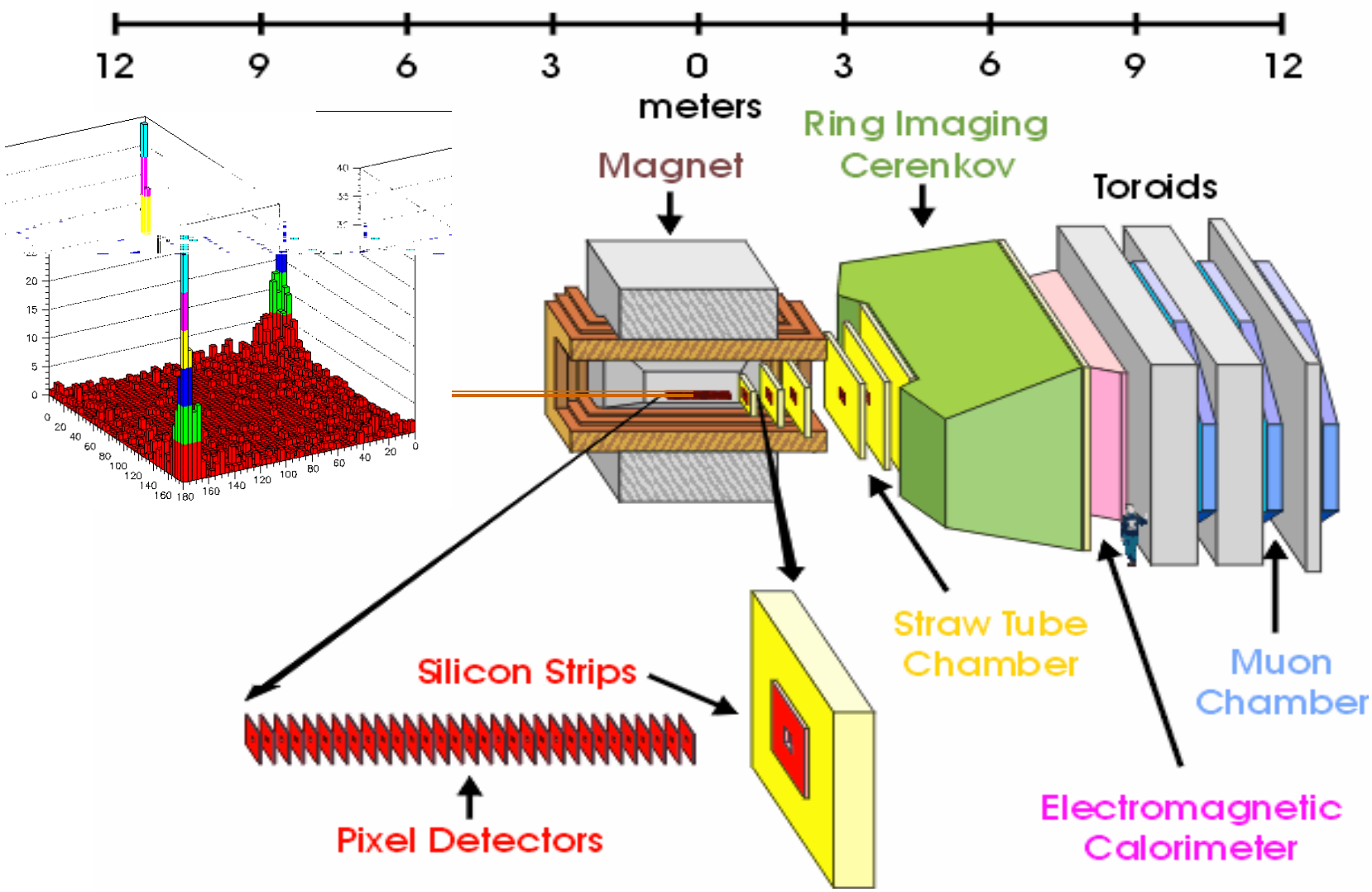
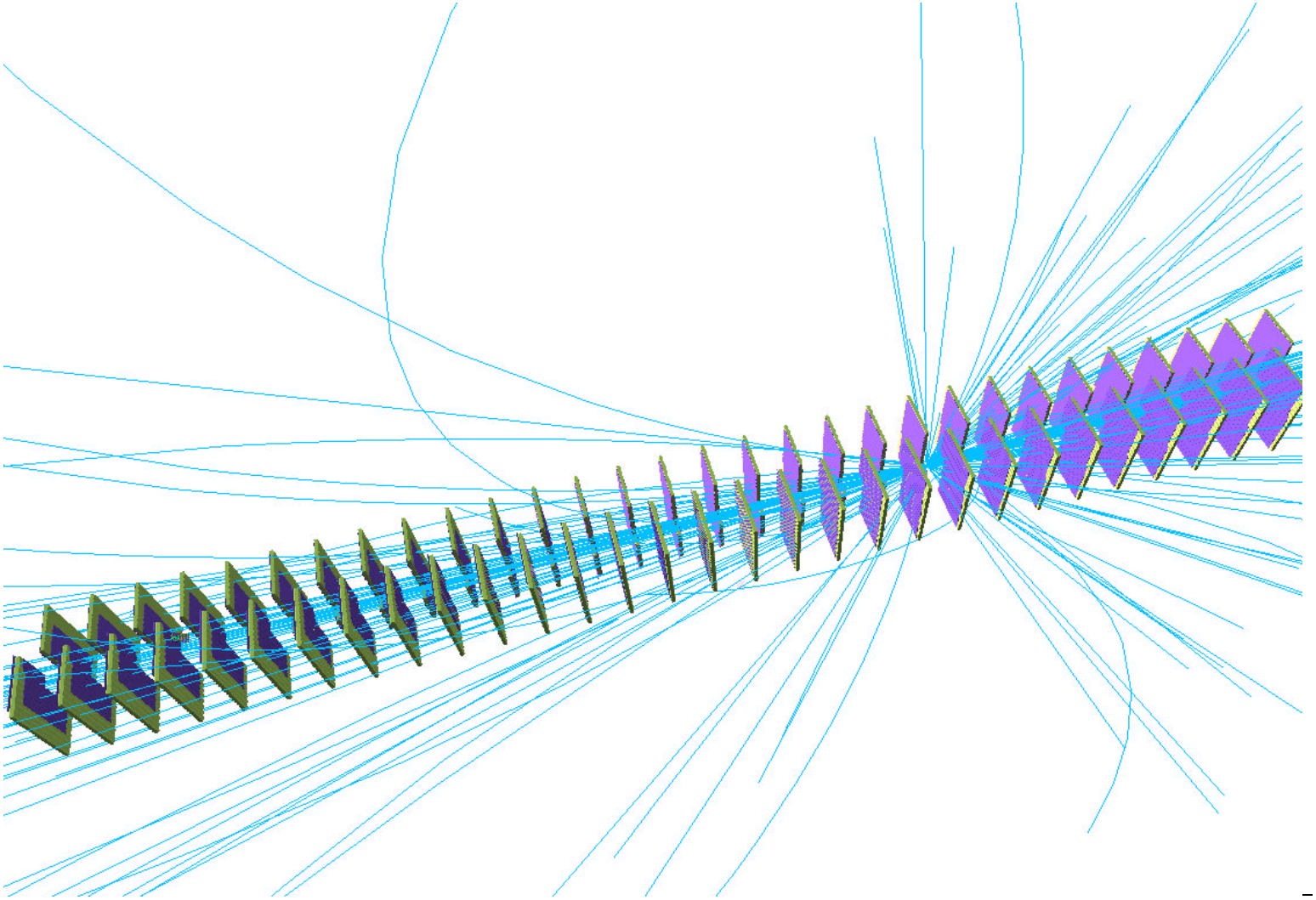
The BTeV Data Acquisition System

- The BTeV Challenge
- The Project
- Readout and Controls

The BTeV Detector at the Tevatron



Simulated B Bbar, Pixel Vertex Detector



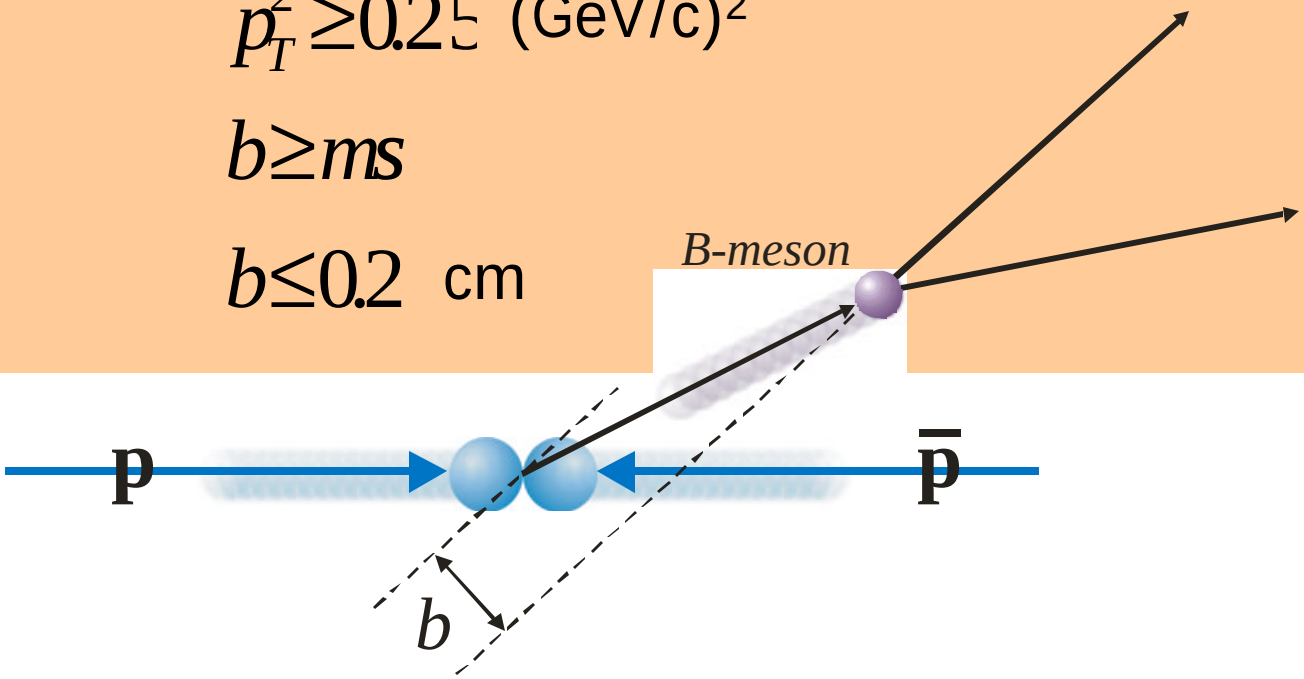
L1 vertex trigger algorithm

- Generate Level-1 accept if ≥ 2 "detached" tracks in the BTeV pixel detector satisfy:

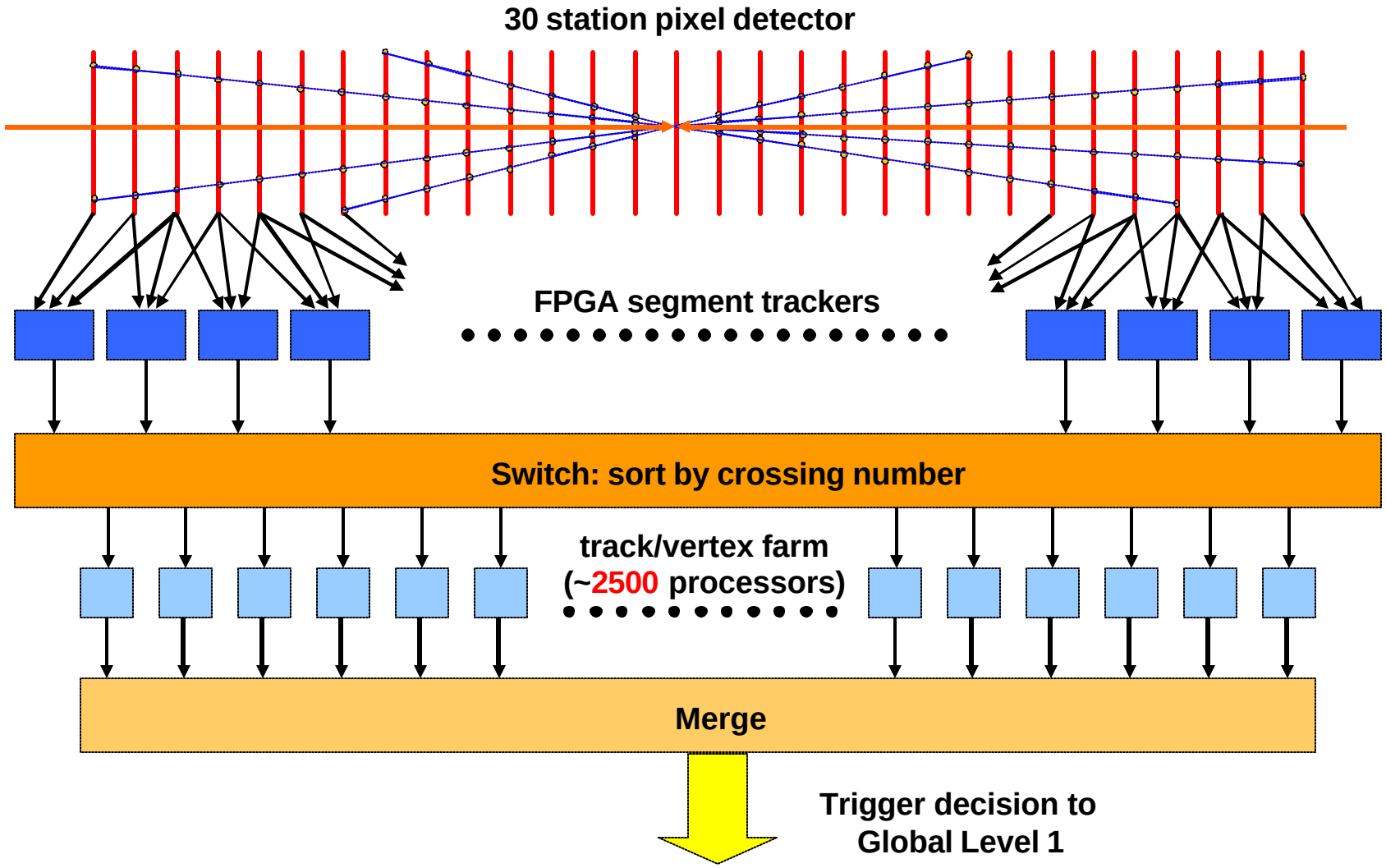
$$p_T^2 \geq 0.25 \text{ (GeV/c)}^2$$

$$b \geq ms$$

$$b \leq 0.2 \text{ cm}$$



Level 1 vertex trigger architecture



DAQ Requirements

Identify interesting events based on the long lifetimes of heavy quarks (b and c)

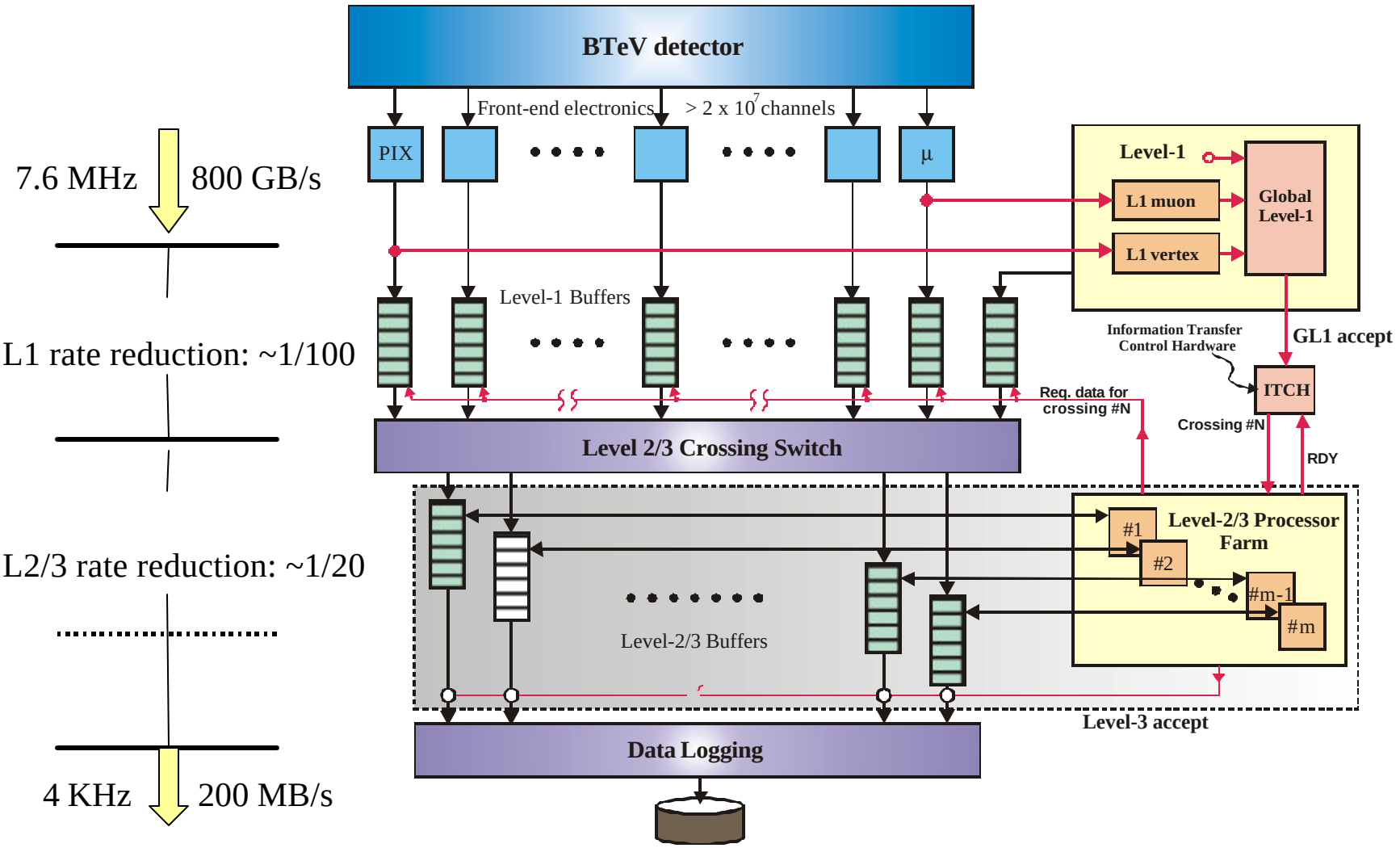
Detached Vertex Trigger at Level 1
(i.e. every crossing)

Complex algorithm => Long latencies (~ 1ms)

We will need lots of memory to buffer the detector data

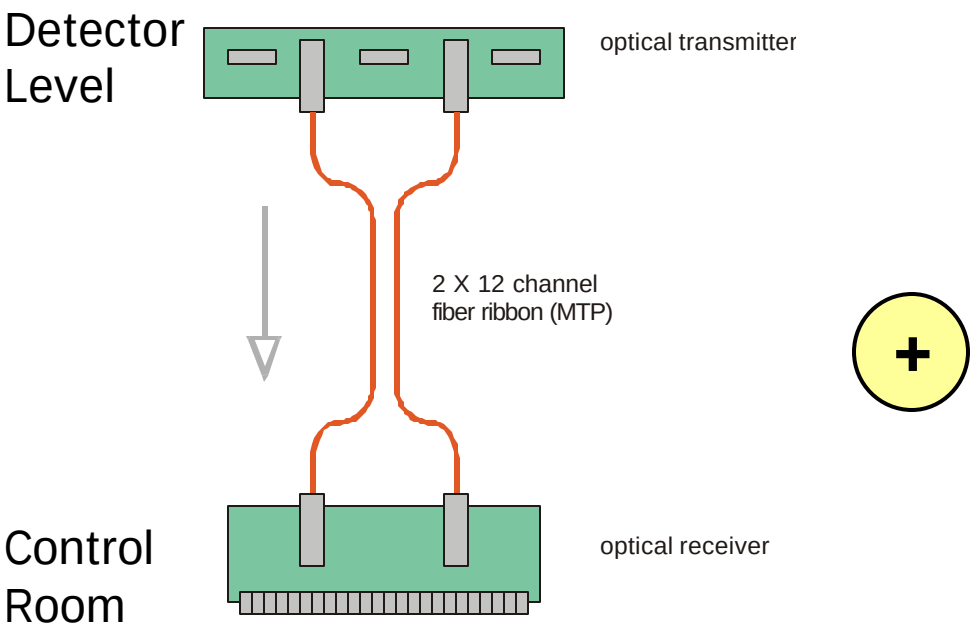
Estimated event size (Geant): 50-80 Kbytes
Event rate (in): 7.6 MHz
(out): 4 kHz

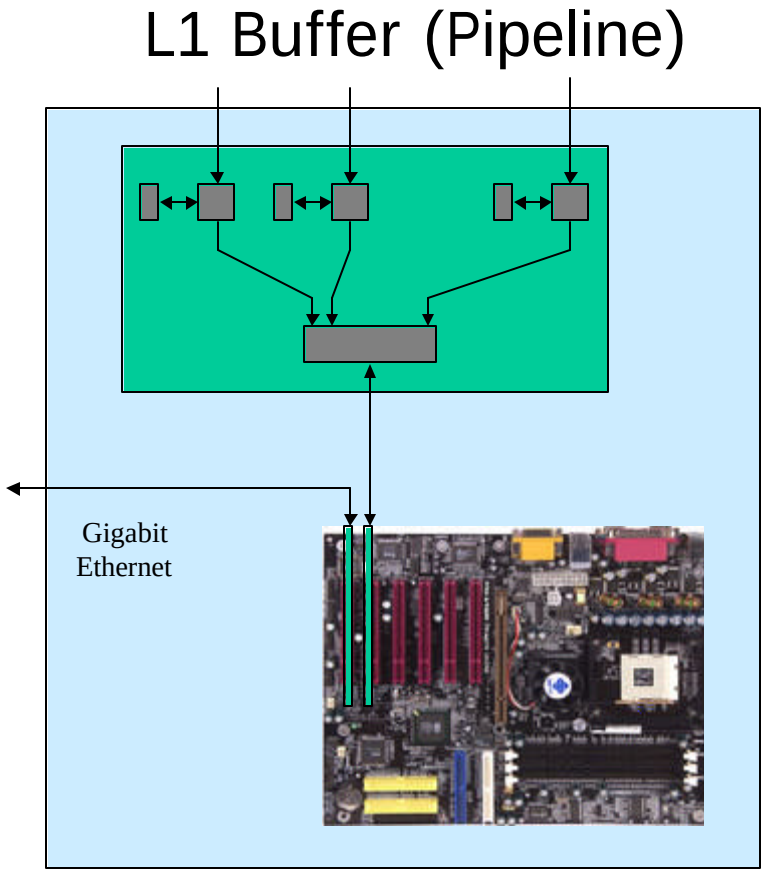
BTeV Data Acquisition Architecture



BTeV Solution

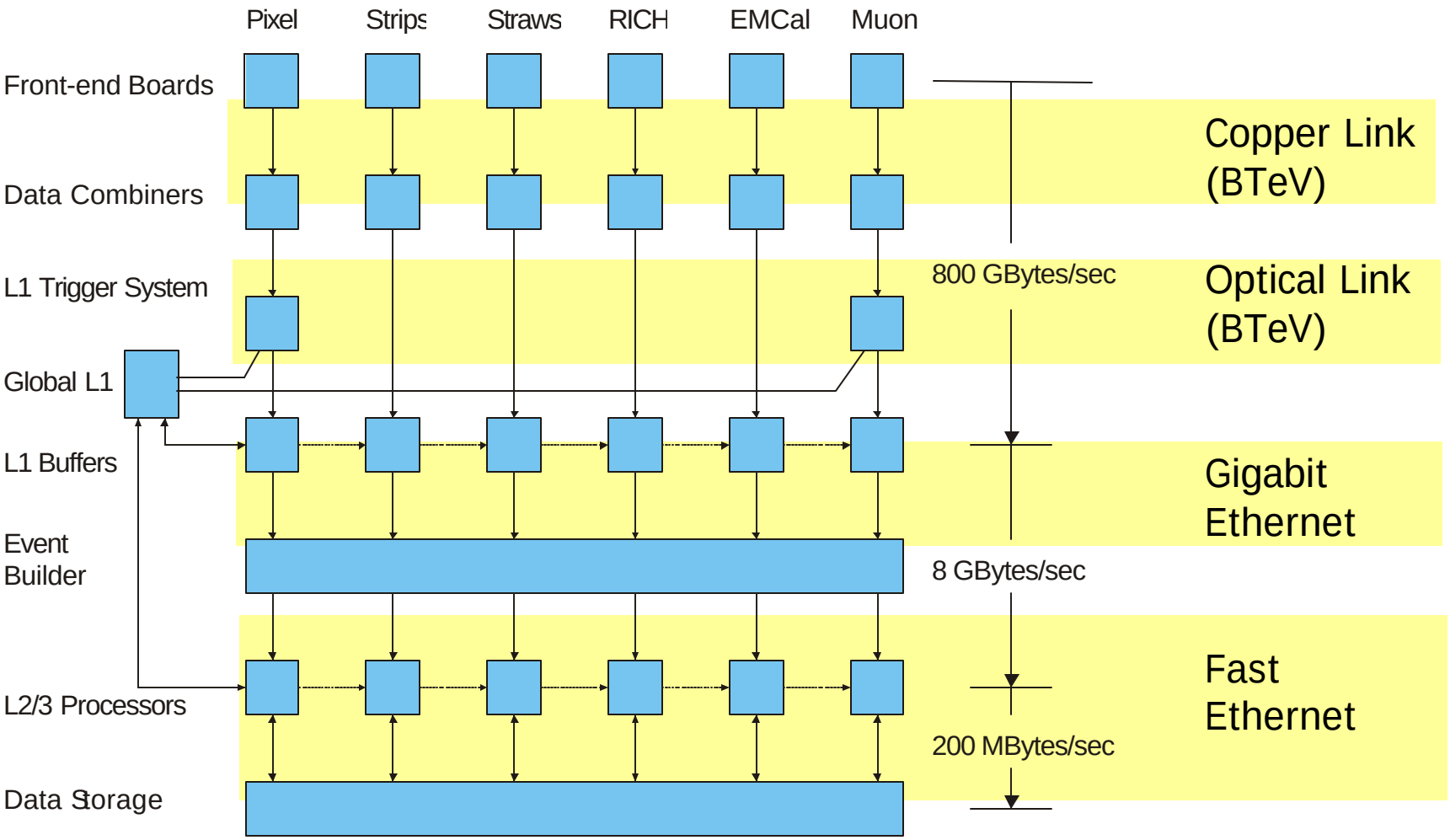
Fast optical data link between detector and DAQ system





Very large buffer memory

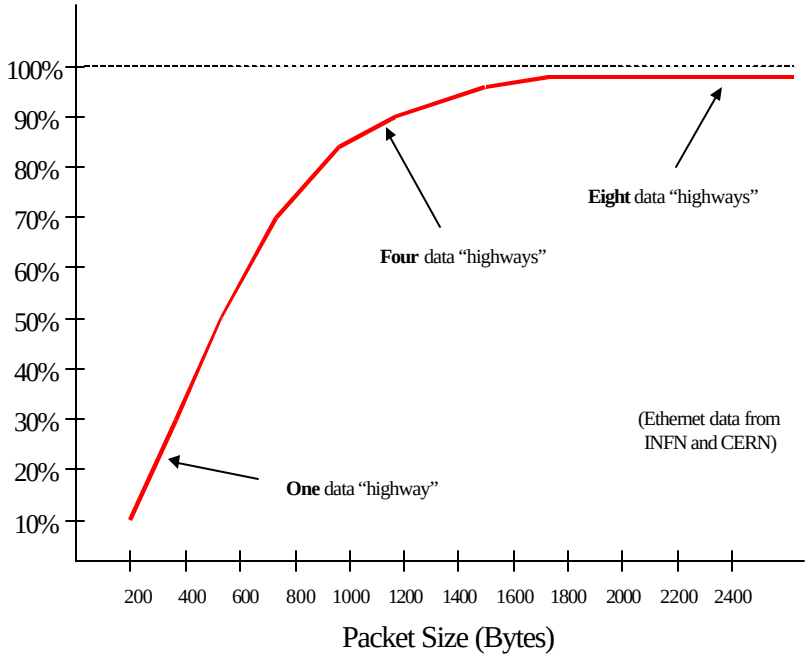
BTeV Data Acquisition Architecture II



Highways

Potential Problems:

1. Very large, very expensive switching network
   ~1000 x 2000
2. Data-rate per readout channels is very small (10s of bytes)
   large number of small messages
3. Large volume/high rate control traffic (e.g. broadcast Level 1 accepts at 100 kHz to a few hundreds buffers



Our Solution:

1. (8) Parallel Highways
   Larger packets, smaller switch, fewer messages

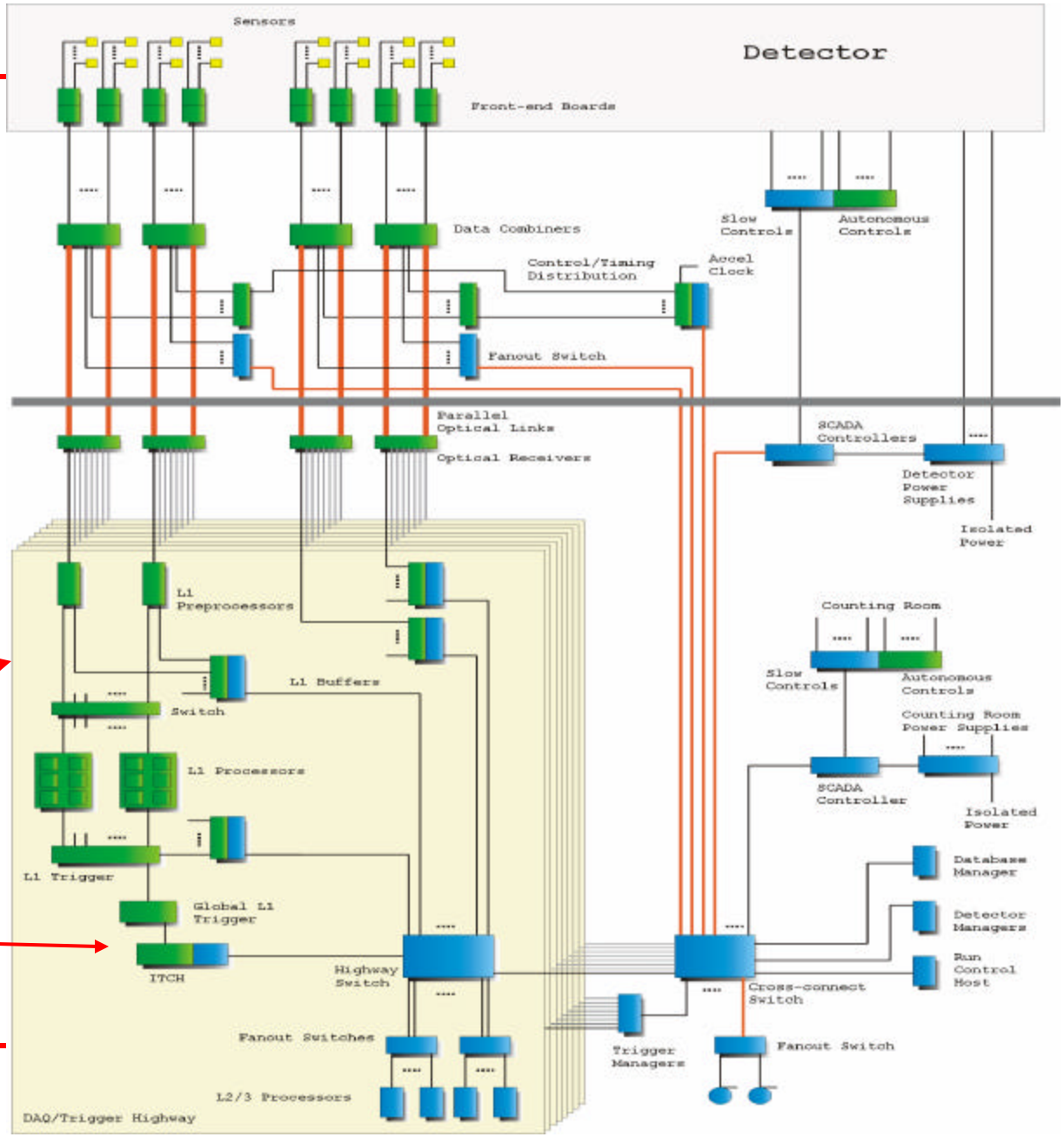
Implementation

Collision Hall

Counting Room

8 Highways

Event Distribution

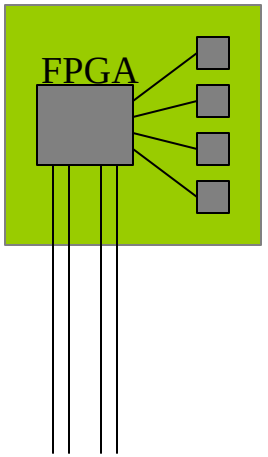


Front-end Interface Prototype

Proposal for prototype work

standard network cables (CAT 6 + RJ45)
620 Mbps serial data rate
LVDS

evaluate other connectors
follow pricing of high speed connectors & optical



HSSDC2

~ $80/cable
separate clock

Standard FE digital interface

In: Crossing clock (7.6 MHz)
Message (620 Mbps serial)

Out: Data 0 (620 Mbps serial)
Data 1 (620 Mbps serial)

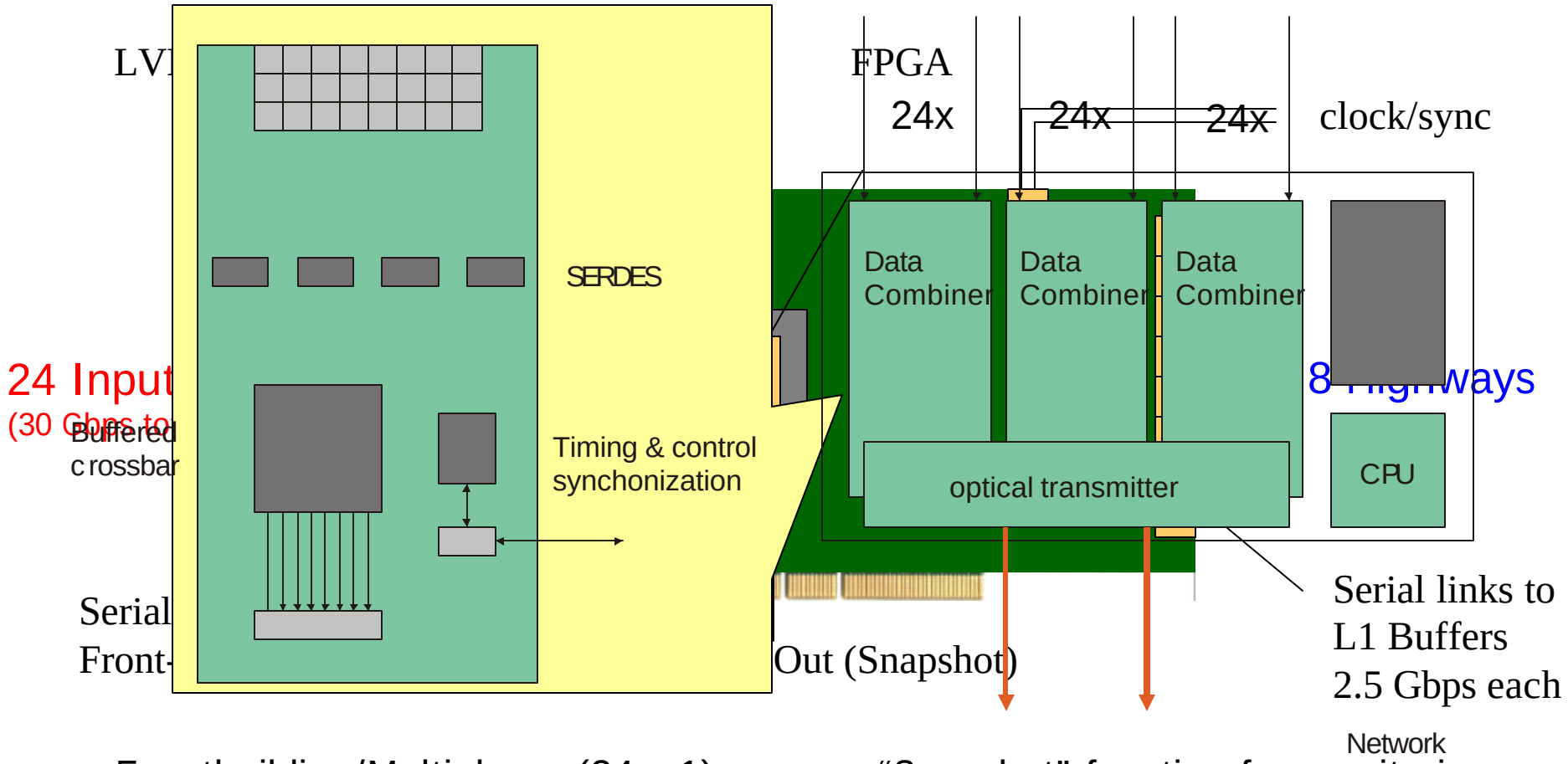
Dual LC (optical)

~ $50/cable
+ $80/cable for transceivers
separate clock

CAT 6

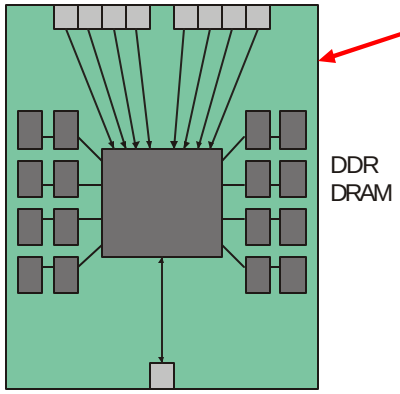
~ $6/cable
clock included

24 Channel Data Combiner Module (Prototype)



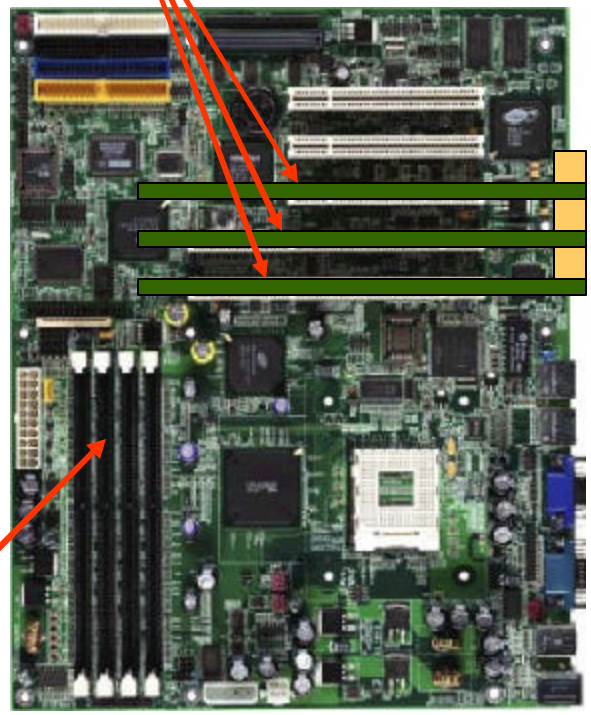
- Eventbuilding/Multiplexer (24->1)
- Event distribution (highways)
- Data reduction (for some sub-systems)
- "Snapshot" function for monitoring
- Located near detector

L1 Buffer (Prototype)



Circular Buffer
(up to 400,000 crossings)

L1 Buffer Modules



from Data Combiners
or L1 Trigger
(24 channels each)

- L1 accepted events are stored in PC memory until requested
  512 MBytes => ~ 100K events
  ~ 8 sec of data

to Highway Switch
(Gigabit Ethernet)

Event-builder (EB) Performance Tests

Assumptions

100 KHz GL1 accept rate (could be 200 KHz!)
30-60 Kbytes Event Size
8 Highways

Events will be built in steps

DCB: Combine data from several front end sources
L1B: Combine data from 24 DCBs
EB: Combine data from 32 L1Bs (in each highway)

Rate Estimates

~30 L1Bs, each containing a 1 - 2 Kbytes fragment
300 L2/L3 CPUs per highway,
Request Rate per L2/L3 CPU: 100 KHz/8/300 ~ 40 Hz

Question

Do we need dedicated event-builder hardware?

Test Configuration

Source: (2) Sun workstation(s), Solaris 2.7, FastEthernet

HP FastEthernet Network Switch

Sink: Linux workstation, Dual Athlon MP2000+, 1 GB, FastEthernet
Red Hat 7.2, Kernel 2.4.18/5 SMP-Athlon

- Accept N TCP/IP connections
- Event-Loop
  - Select/Read data from each Source
  - Simple error checking
  - Complete one event before starting the next
  - Discard data

Test Results

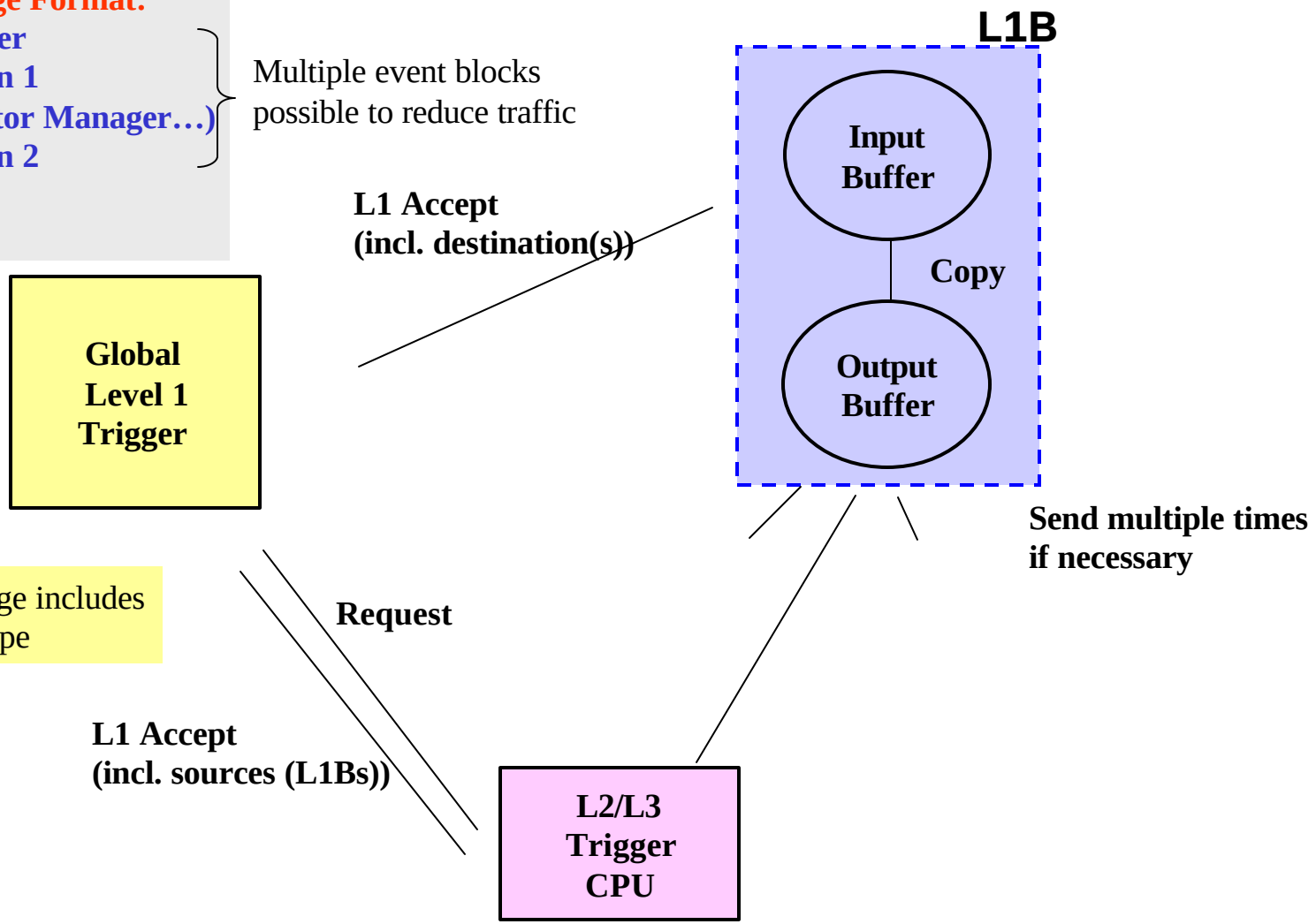
Configuration	Event Size	Rx KB/s	Rx Pkt/s	Tx KB/s	Tx Pkt/s	Int/s	CPU Load
30 Sources 1 Kbyte 40 Hz	30 KB	1200	1200	50	850	1850	1.7%
30 Sources 1 Kbyte 80 Hz	30 KB	2470	2420	80	1500	3300	2.6%
30 Sources 2 Kbytes 80 Hz	60 KB	4900	4800	140	2400	6000	2.1%
30 Sources 2 Kbytes 80 Hz Simulated Load	60 KB						6.0%

⇨ Software Event-Builder is our baseline solution

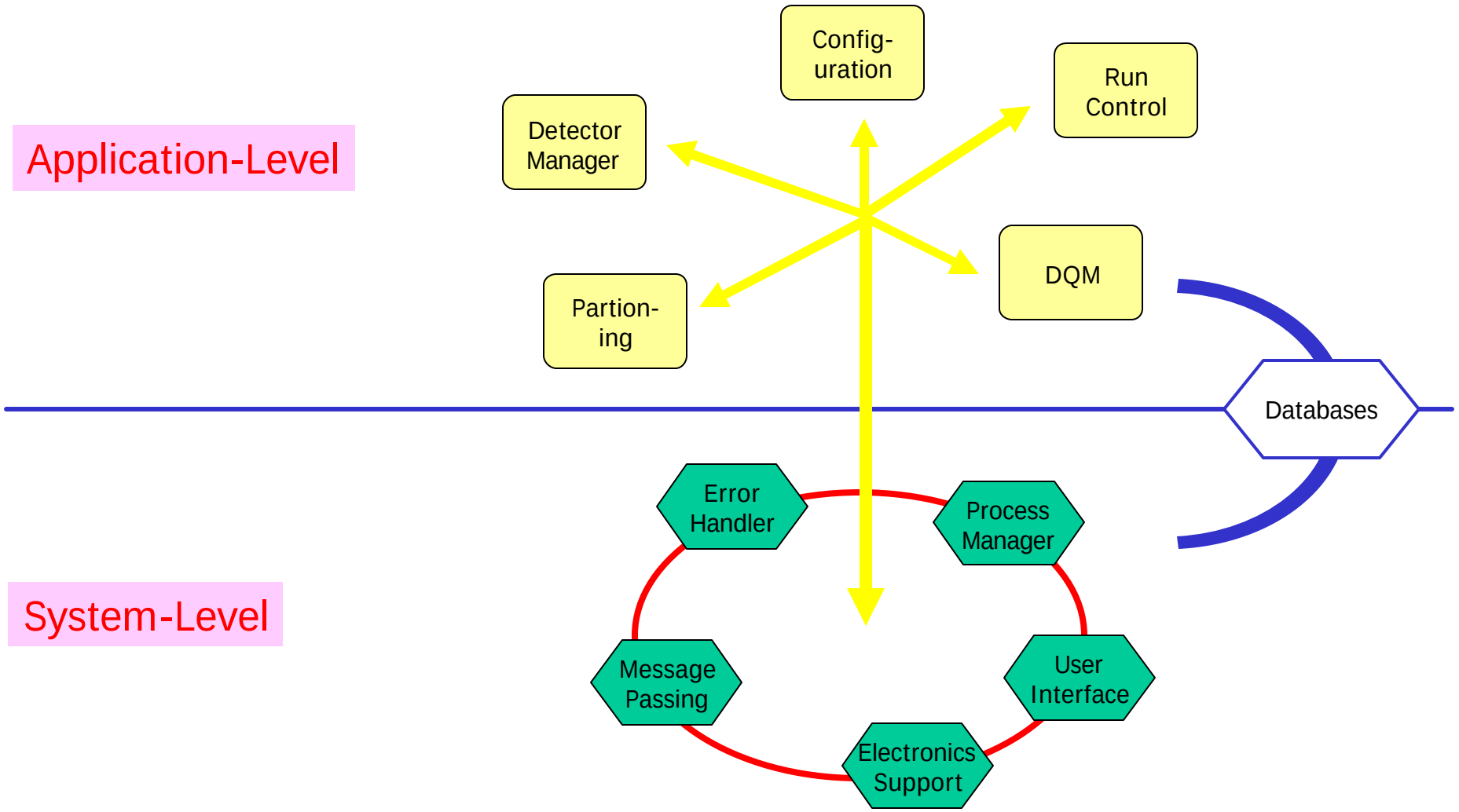
Data Flow Model and Event Distribution

L1 Accept Message Format:
- **Crossing Number**
- **IP of Destination 1**
  - **(L2/L3, Detector Manager…)**
- **IP of Destination 2**
- **…**

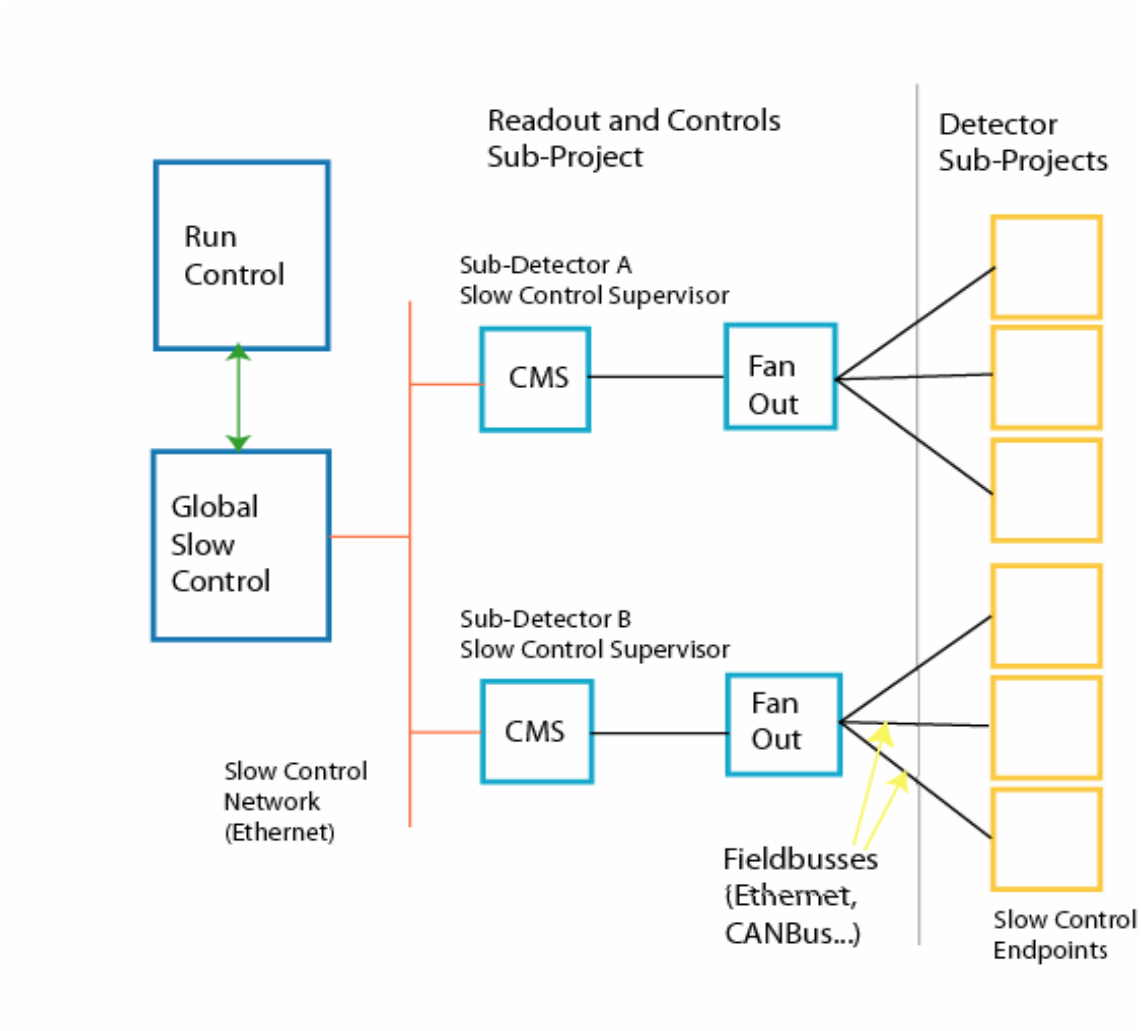
Multiple event blocks possible to reduce traffic



Readout Software



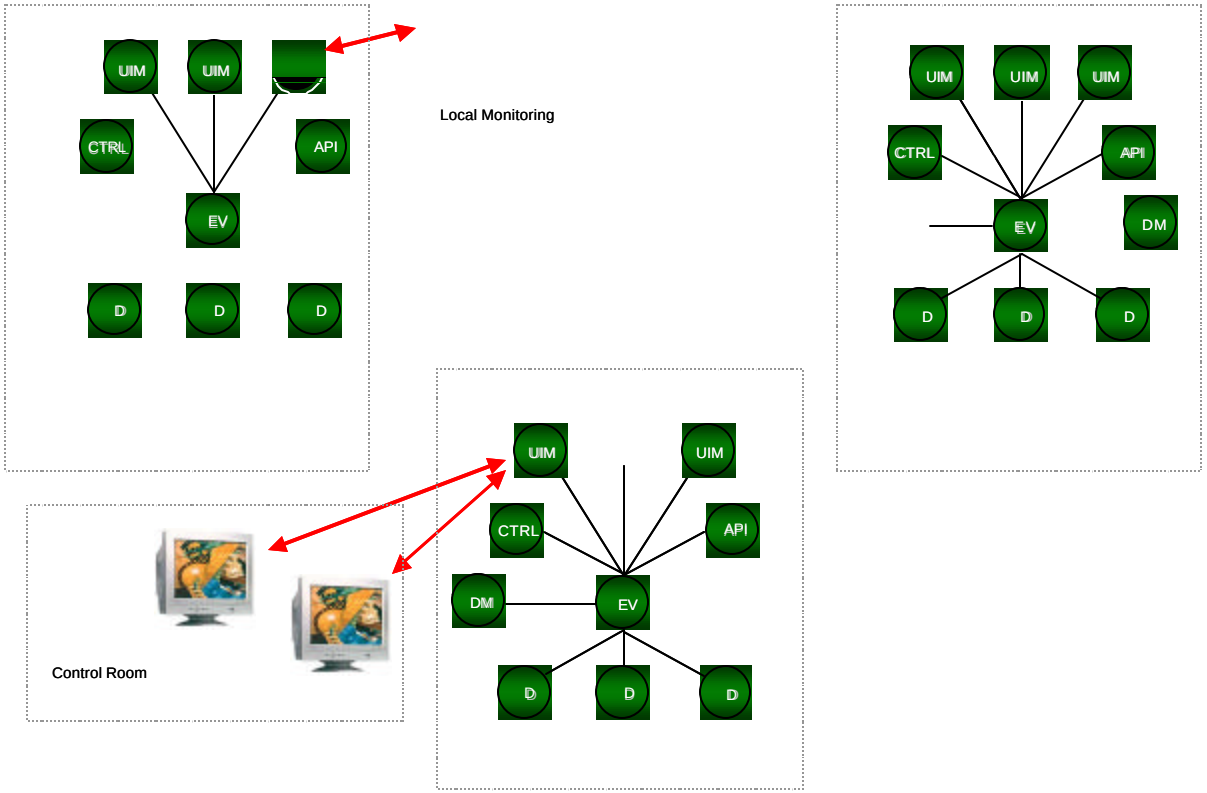
BTeV DCS Diagram



ntrol System (PVSS II)

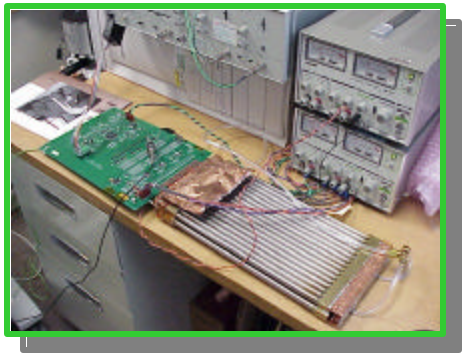
RN

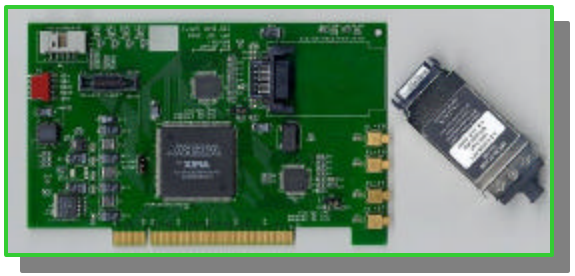
and

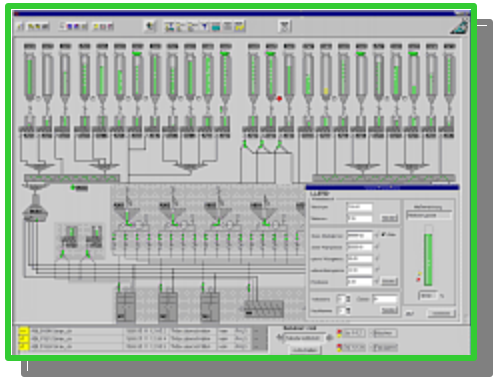


R&D

- System Architecture
- Front-end noise studies
- Cable tests
  - CAT 6, USB-2, Firewire
- Timing & Clock distribution
  - Fan-out vs. multi-drop line with reflection
- Optical link test
- Gigabit Ethernet Switch
- PVSS II Evaluation







Summary

- High performance DAQ at very reasonable costs
  - Use fast links to get data off detector quickly
  - Use inexpensive DRAM instead front-end buffers
- Moderate technical risk, commercial solutions where possible
- Full support for BTeV Trigger, i. e. large Level 1 latency
- No busses – only point-to-point links
- Conceptual Design complete, now we have to build it:
  a) Readout Hardware
     Design L1B, DCB FPGAs, Prototypes, Protocols
  b) Readout Software and Run-Control
     System Software, message passing
  c) Event-Building
     Evaluate commercial network hardware
  d) Detector Control
     Follow CERN/LHC approach, commercial solutions