



IBL & nSQP Opto-board Assembly Procedure

ATLAS Project Document No:

ATL-IP-AP-0040

Institute Document No.

Created: **29/11/2012**

Page: **1 of 10**

Modified: **3/14/2021**

Rev. No.: **2**

IBL & nSQP Opto-board Assembly Procedure

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Distribution List

Atlas Collaboration for comments

History of Changes

<i>Rev. No.</i>	<i>Date</i>	<i>Pages</i>	<i>Description of changes</i>
1	29/11/2012	All	First revision
2	25/5/2019		Second revision, minor wording changes
3	14/3/2021		Third update

Table of Contents

1. INTRODUCTION	4
2. LIST OF ASSEMBLY TOOLS	4
3. MAJOR ASSEMBLY STEPS	5
Mounting of passive components.....	5
Electrical short test.....	6
Scoring of opto-boards.....	6
Mounting of optical connectors.....	7
Mounting of opto-packs.....	7
Cleaning of the opto-boards.....	8
Die attachment of the VDCs and DORICs	8
Wire bonding of VDCs and DORICs	8
Wire bonding of the opto-packs	8
Encapsulation and Testing	9
4. LIST OF INDIVIDUAL OPTO-BOARD ASSEMBLY STEPS.....	9

1. Introduction

The original ATLAS pixel detector has three-barrel layers and six disks. The original service quarter panels (SQP) was replaced by the new SQP (nSQP) in 2013/14. To service the outer two barrel layers (L1 and L2) and disks, each nSQP opto-board contains seven pairs of data (DTO1 and DTO2) links and seven clock/command links (TTC). Depending on the occupancy of the link in question, DTO1 may be used alone. To achieve a higher bandwidth, both DTO1 and DTO2 may be used. Because of this, fourteen DTO lines are present on each opto-board. For compliance with the connectivity between the SQP opto-boards and the off-detector readout, two flavors of nSQP opto-board must be fabricated. The two flavors are called B-Layer and D-Tall.

The insertable B-layer (IBL) detector is a barrel layer installed inside the innermost barrel layer of the original pixel detector. To service this new barrel layer, each IBL opto-board contains sixteen DTO and eight TTC links. There is therefore one DTO line per data link. Unlike nSQP, only one flavor of IBL opto-board was fabricated.

Each DTO line contains one VDC (VCSEL Driver Chip) channel driving a VCSEL channel. Each TTC link contains one DORIC (Digital Opto-Receiver Integrated Circuit) channel receiving a signal from a PIN channel. The DORIC and VDC are fabricated in 4-channel arrays. The VCSEL and PIN are 12-channel arrays. For integration of the VCSEL and PIN on the opto-board, the arrays are mounted to a custom package called an opto-pack. Therefore each opto-board contains four VDCs, two DORICs, one PIN opto-pack, and two VCSEL opto-packs. All individual components must be certified to meet their own quality assurance (QA) tests before being mounted on an opto-board. The assembled opto-board must then pass a series of QA tests before shipment to CERN.

The nSQP requires 44 opto-boards for the B-layer and 228 opto-boards for L1 and L2 and disk (D-Tall). A photo of a completely assembled IBL opto-board is shown in Fig. 1. Please note that both flavors of nSQP opto-board will have a nearly identical appearance.

2. List of assembly tools

The following is a summary of the tools needed for the assembly:

- Electrical short tester
- Opto-pack mounting jig
- Tweezers
- Scalpels
- 3 MPO connectors with slightly over-polished (100 μ m) MT ferrules

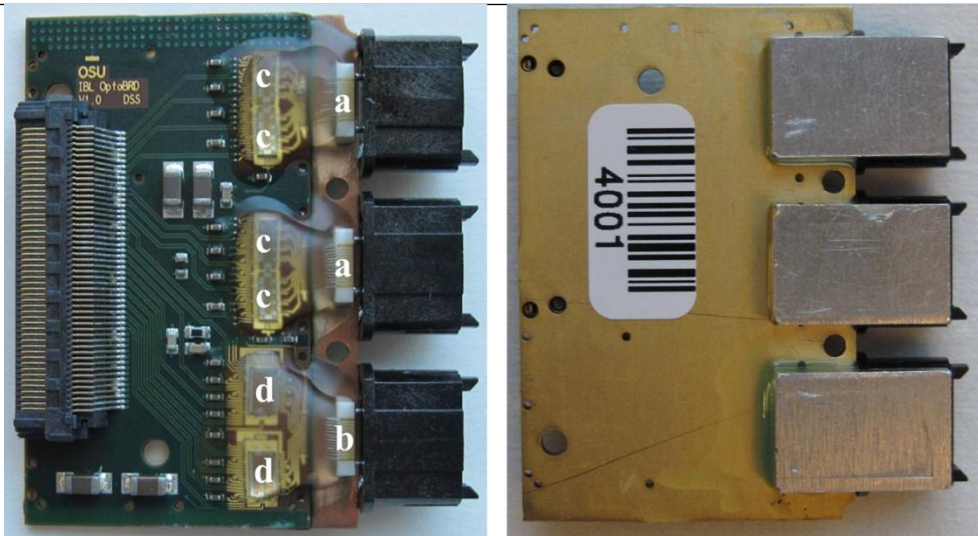


Figure 1: (Left) top view of a fully assembled IBL opto-board: (a) VCSEL opto-packs, (b) PIN opto-pack, (c) VDC, (d) DORIC. (Right) bottom view of the same opto-board.

3. Major assembly steps

The following is a summary of the major assembly steps:

- Mounting of passive components
- Electrical short test
- Scoring of the opto-board
- Mounting of the optical connectors
- QA measurements on the VCSEL and PIN opto-packs
- Mounting of the opto-packs
- Cleaning of the opto-board
- Mounting of VDCs and DORICs
- Wire bonding of VDCs and DORICs
- Wire bonding of opto-packs
- Encapsulation and testing

Mounting of passive components

The opto-board PCBs are fabricated by the Cirexx, the same vendor as the second generation opto-boards. Each board is comprised of a 6-layer printed circuit board adhered to 1 mm thick copper plate for thermal management. A simplified cross section of an opto-board and a table of the material stack up are shown in Fig. 2. Avcom SMT Inc. populates the blank boards with ~45 passive components: 22 nF, 100 nF, and 1 μ F capacitors, 75 and 100 Ω resistors, and an 80-pin (nSQP) or 100-pin (IBL) Samtec LSHM hermaphroditic connector. This is the same vendor that populated the second generation opto-boards. The solder paste used is AIM NC257-2 SN100C with a maximum reflow temperature of 270°C.



Figure 2: Simplified cross section of the opto-board (left). Complete listing of opto-board stack up information (right).

Electrical short test

Cirexx performs a netlist verification using a flying probe tester on all opto-boards. We therefore will not perform any further testing.

Scoring of opto-boards

Scoring is applied to both the front and back of each opto-board. This ensures strong adhesion when mounting the opto-packs/braces and optical connectors, respectively. The front is scored using the height measurer shown in Fig. 3 (a) with the opto-board fastened in the jig shown in Fig. 4 (b). Lines are scored across the surface in increments of 0.012 in. until the scoring reaches the guide holes, as shown in Fig. 5. A hatch pattern is scored on the back of the board where each optical connector will be mounted as shown in Fig. 3 (b). The front and back are both cleaned with acetone and blow dried before any mounting on the surfaces.

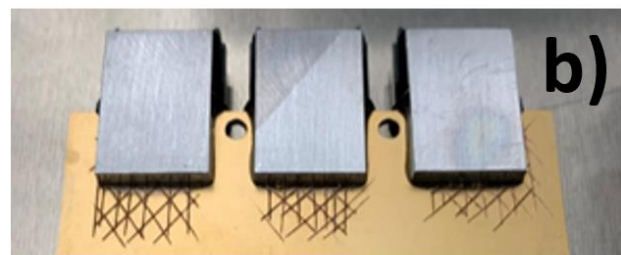
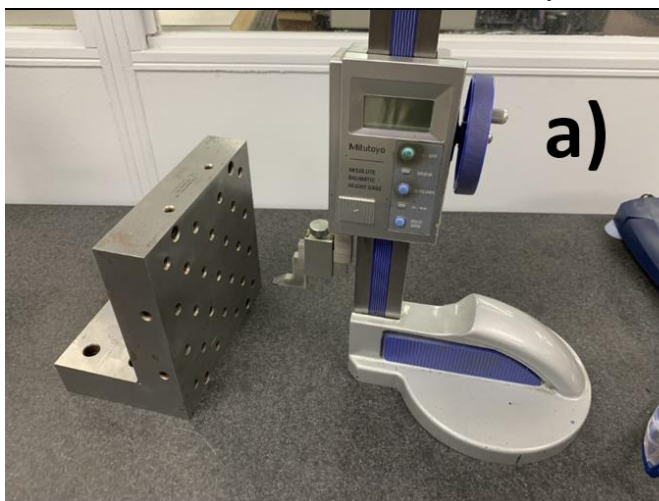


Figure 3: Pictures of the height measurer used for scoring the front of each opto-board (a) and the scoring applied to the back of the opto-board where the opto-connectors are mounted (b).

Mounting of optical connectors

To interface with an industry standard MPO optical connector, custom optical connectors are glued to the opto-boards. Each optical connector consists of a standard part from USCONEC called an MTP inner adapter (part #C10196) attached to a machined aluminium part using Loctite Hysol EA 9396. A photo of an optical connector is shown in Fig. 4 (a). The machined aluminium part assists in alignment of the MTP inner adapter and the opto-pack and provides a large surface area for glue (Hysol EA 9396) adhesion to the opto-board itself. The attachment of the optical connectors is accomplished using a jig shown in Fig. 4 (b) and (c). The jig holds the optical connectors in their proper locations with respect to the opto-boards in place while the glue (Hysol EA 9396) is being cured.

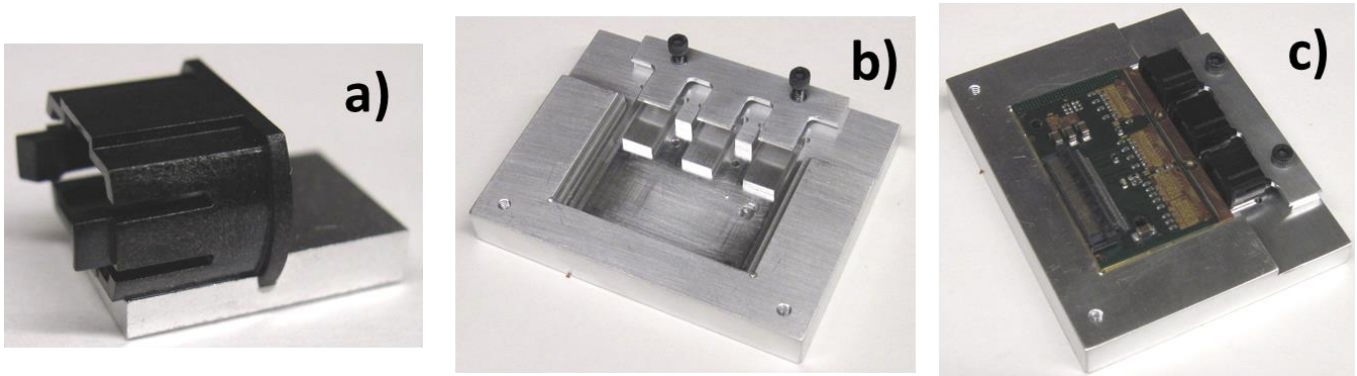


Figure 4: Pictures of the optical connector (a), gluing jig (b), and gluing jig with opto-board (c).

Mounting of opto-packs

Once the optical connectors are securely glued, the opto-packs are glued (Hysol EA 9396) in position on the copper plate. Proper alignment of the opto-packs on the opto-board is critical to ensure good coupling with an industry standard MPO optical connector. This alignment is accomplished by inserting a complete MPO optical connector into the optical connector and then pushing the opto-pack to be glued into this MPO connector. It is important to note that the completed MPO connectors used are made with MT ferrules that have been slightly over polished by 100 μm . The purpose of the over polishing is to ensure that the opto-packs are positioned closer to the edge of the board thus forcing an MPO with a standard polished MT (as will be used during testing and in the detector) to be pressed into the opto-pack completely. Once inserted, small droplets of Hysol EA 9396 are placed at the back corners of the opto-pack as far from the MT ferrule as possible and cured. When this cure is complete, the MPO connectors are removed and more Hysol EA 9396 is placed on the back of the opto-pack to glue it even more securely. The reason for using the two gluing steps is due to the low viscosity of the Hysol. If too much is applied when the MPO connector is mated to the opto-pack, it is possible for the glue to wick up the face of the MT ferrule and permanently glue the MPO connector to the opto-pack. This can ruin both the opto-pack and the MPO connector. The opto-pack is then reinforced with an aluminium brace using Hysol EA 9396 as shown in Fig. 5.

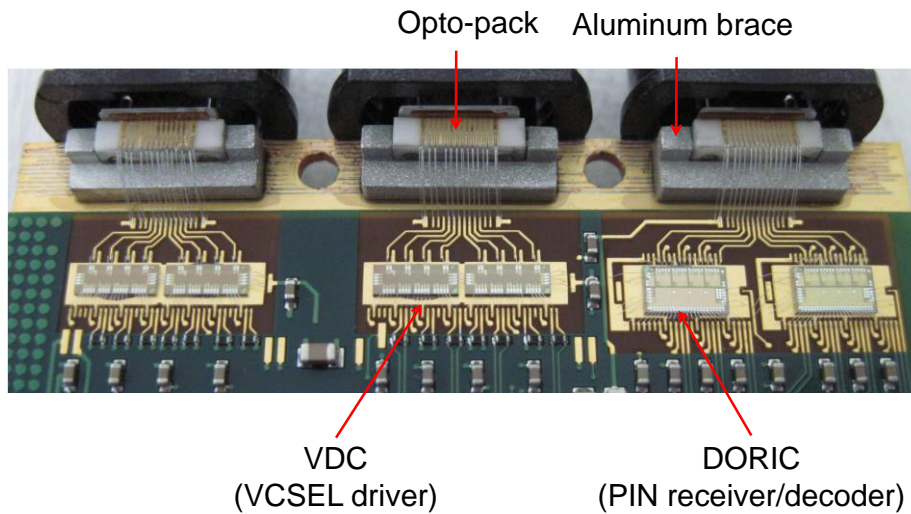


Figure 5: Close-up view of an opto-board.

Cleaning of the opto-boards

With the opto-packs securely in place it is easy to swab them clean with acetone and blow them dry. Following this, the other surfaces to be wire bonded on the opto-board are swabbed and dried similarly.

Die attachment of the VDCs and DORICs

The VDCs and DORICs are attached to the opto-board with Epotek H20E, a conducting epoxy. This is a manual process requiring a technician to apply an appropriate amount of glue to the pads where the chips are to be placed. Once this is complete, the die are picked up using ESD safe plastic tweezers and placed into their appropriate positions. The alignment of the die is not critical because the wire bonding machine can easily compensate for varying chip position with respect to the opto-board bond sites. Once the dies are in place, the H20E is cured for 3 hours at 80°C.

Wire bonding of VDCs and DORICs

To simplify wire bonding, care was taken in the design of all flavors of opto-board so that the same bonding program works for all boards. For enhanced reliability, all wire bonds are doubled whenever possible. Since no test pads for wire bonding were designed on the chips, we use unused active pads on the chips to monitor pull strengths. The first step in our wire bonding process is to add these test wire bonds to each chip and then pull them to measure the pull strengths. If the pull strengths are all above 7 gf, the rest of the bonds on the board can be made. If a wire bond fails the pull strength test, the bonding areas must be cleaned and a second set of test bonds attached and pulled. If the new pull strengths are all above 7 gf, the chips can then be fully bonded or else the board is abandoned.

Wire bonding of the opto-packs

The opto-packs are wire bonded to the opto-board using a similar approach to what is used for the ASIC chips. We first put a test bond between each opto-pack and opto-board and then pull them to measure the pull strengths. If the pull strengths are all above 7 gf, the rest of the bonds

on the opto-packs can be made. If a wire bond fails the pull strength test, the bonding areas must be cleaned and a second set of test bonds attached and pulled. If the new pull strengths are all above 7 gf, the opto-packs can then be fully bonded or else the board is abandoned. For enhanced reliability, all wire bonds are doubled whenever possible.

Encapsulation and Testing

With the assembly steps complete, some basic functionality tests will be performed after the wire bonding. If the opto-board passes the tests, the wire bonds will be encapsulated. Following encapsulation, a Kapton bar code serial number label is adhered to the back of the opto-board. All nSQP D-Tall boards will have 4XXX serial numbers, all nSQP B-Layer boards will have 5XXX serial numbers, and all IBL boards will have 6XXX serial numbers. Following the assembly described above, we will perform burn-in, thermal cycling, and QA measurements all to be discussed in a separate document.

4. List of individual opto-board assembly steps

The following is a list of individual assembly steps. Each opto-board has a status sheet that must be updated after each step.

- 1) Score the opto-board:
 - a. Score the front of the opto-board as described in Section 3.
 - b. Score the back of the opto-board as described in Section 3.
- 2) Clean the opto-board:
 - a. Rinse the opto-board with isopropyl alcohol then de-ionized water for 60 seconds
 - b. Blow dry with nitrogen
 - c. Bake in oven for 1 hr. at 100°C
- 3) Mount the optical connectors
 - a. Assemble three optical connectors
 - i. Apply a dot (4 mm x 4 mm) of Hysol near the channel on the machined aluminium part
 - ii. Press MTP inner adapter into the aluminium channel and the Hysol dot
 - iii. Clamp the MTP inner adapter and the machined aluminium part together
 - iv. Bake in oven for 1 hr. at 80°C
 - b. Insert three assembled opto-connectors into the gluing jig
 - c. Bolt down the opto-connector holding clip
 - d. Apply a dot (4 mm x 4 mm) of Hysol to the exposed region of the aluminium part of the optical connector away from the plastic part of the optical connector
 - e. Place the opto-board into the gluing jig
 - f. Screw the opto-board down to the jig using 1-74 screws through the extraction tool holes
 - g. Cure for 45 min. at 80°C
 - h. Take the board out of the jig

- 4) Mount the opto-packs
 - a. Re-clean, using acetone and swabs, the surface on the opto-board that will be used for gluing the opto-packs
 - b. Select two VCSEL packs and one PIN pack that have passed the QA
 - c. Insert 3 complete MPO connectors into the opto-board optical connectors
 - d. Clean, using acetone and swabs, the PIN and VCSEL opto-pack surfaces that will be used for gluing
 - e. Insert the PIN opto-pack into its associated MPO connector
 - f. Insert the VCSEL #1 opto-pack into its associated MPO connector
 - g. Insert the VCSEL #2 opto-pack into its associated MPO connector
 - h. Apply small dabs of Hysol to the corners of the opto-packs and opto-board
 - i. Cure for 30 min. at 80°C
 - j. Remove the three MPO connectors
 - k. Apply large dabs of Hysol to the back edge of each opto-pack that will be in contact with the aluminium brace and opto-board and push the brace against the opto-pack and opto-board
 - l. Cure for 45 min. at 80°C
- 5) Clean the opto-board
 - a. Using several swabs, clean the traces on the opto-packs with acetone
 - b. Using several swabs, clean the bonding areas on the opto-board
 - c. Blow dry the board and opto-packs with nitrogen
- 6) Attach the DORIC and VDC die
 - a. Apply a thin layer of adhesive (Epotek H20E with 50% resin (part A) by weight) on the VDC pads and the DORIC pads on the opto-board
 - b. Mount the VDCs on the opto-board
 - c. Mount the DORICs on the opto-board
 - d. Cure the opto-board at 80°C for 3 hours
- 7) Wire bond the DORICs and VDCs
 - a. Wire bond the test pads on the DORICs and VDCs
 - b. Perform pull test on the wire bonds
 - c. If the pull strengths are all above 7 gf bond all chips. Otherwise repeat the steps on the second set of test pads. If the pull strength of a test bond is below 7gf, abandon the board
- 8) Wire bond the opto-packs
 - a. Wire bond the large pads on the opto-packs
 - b. Perform a pull test on the wire bonds
 - c. If the pull strengths are all above 7 gf bond all opto-packs. Otherwise repeat the steps on the same large pads. If the pull strength of a test bond is below 7gf, abandon the board
- 9) Perform the basic functionality test procedures
- 10) Encapsulate wire bonds
 - a. Apply the encapsulant (Dymax 9001 V.3.1) on all wire bonds

- b. Cure the encapsulant with UV for 60 seconds
- c. Apply encapsulant to any bonds not coated in the first step
- d. Cure the encapsulant with UV for 60 seconds

11) Apply the Kapton serial number label

12) Run the board through burn-in, thermal cycling, and QA