EMU DAQ MotherBoard

Jianhui Gu

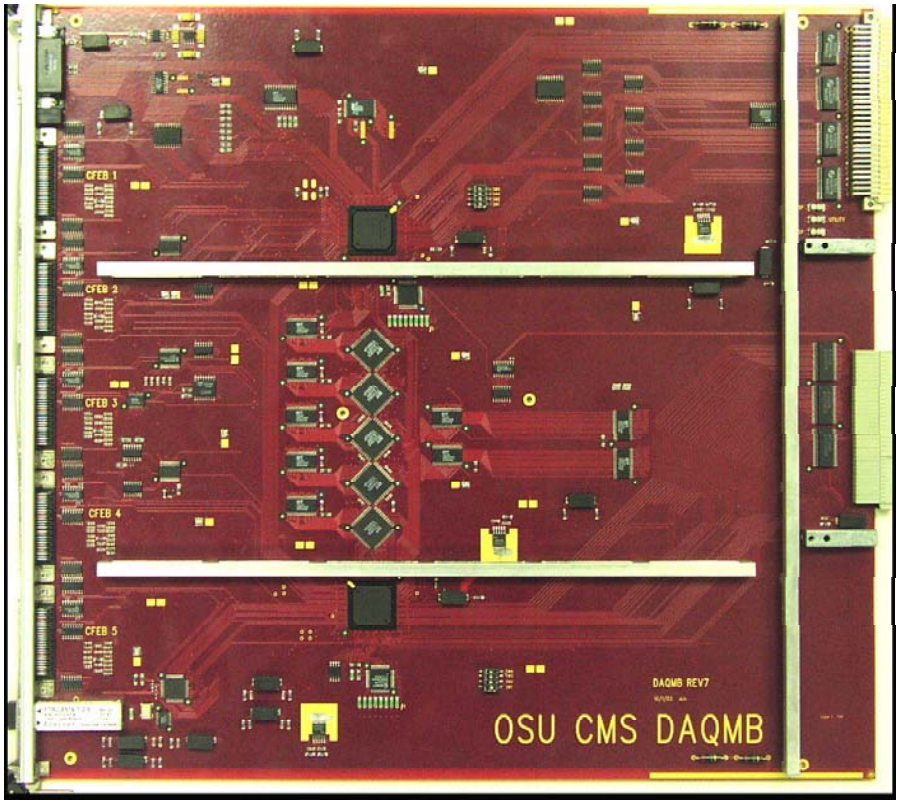
The Ohio State University

ESR, CERN, November 2003

Outline

- DAQMB Function
- DAQMB tests
- DAQMB procedures
- Production preparation

DAQMB Function



Each DAQMB serves one CSC
1 ALCT, 1 TMB, 5 CFEB

Data Acquisition

- LCT Initiates CFEBs digitization
- L1A Receives and sends FE data to counting house

Fast Control

- L1A and BX number
- synchronization
- Reset and Initialize CFEBs

Slow Control

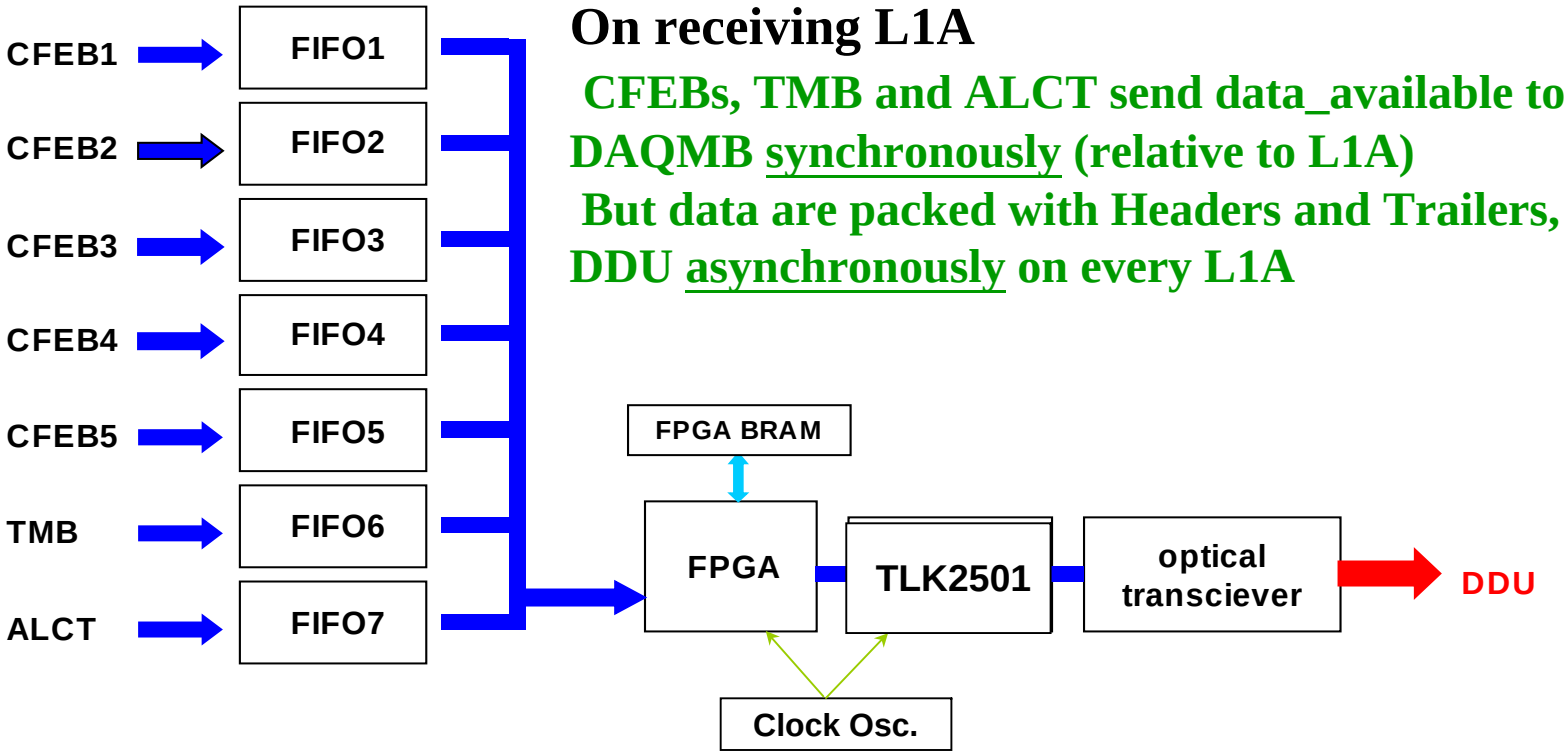
- Provides Slow Control to CFEBs
- Calibrates CFEBs
- Controls and interfaces LVMB to VME

Misc.

- 9U x 400mm VME slave
- +5V (~1A), +3.3V (~1A)
- Regulators for +2.5V, +1.5V, +3.3V

DAQMB Function: Data Acquisition

Data Funneled through 16Kx18bit FIFOS



On receiving L1A

CFEBs, TMB and ALCT send data_available to DAQMB synchronously (relative to L1A)

But data are packed with Headers and Trailers, sent to DDU asynchronously on every L1A

DAQMB Function: Data Acquisition

Header 1: 1 0 0 D?[12] TMBdav[11:10] CFEBActive[9:5] CFEBdav[4:0]
Header 2: 1 0 0 D?[12] L1aNumLow[11:0]
Header 3: 1 0 0 D?[12] L1aNumHigh[11:0]
Header 4: 1 0 0 D?[12] Bxn[11:0]
Header 5: 1 0 1 0 Duplicate Header 1[11:0]
Header 6: 1 0 1 0 CrateID[11:4] BoardID[3:0]
Header 7: 1 0 1 0 CFEBmultiOvlp[11:7] FifoHfull[6:0]
Header 8: 1 0 1 0 Rsvd[11:4] FreeCounter[3:0]
ALCT data if any
TMB data if any
CFEB data if any
Trailer 1: 1 1 1 1 Duplicate header 1[11:0]
Trailer 2: 1 1 1 1 Duplicate header 7[11:0]
Trailer 3: 1 1 1 1 L1aLength[11:4] Bxn[3:0]
Trailer 4: 1 1 1 1 Duplicate header 6[11:0]
Trailer 5: 1 1 1 0 FifoEmpty[11:6] FifoFull[5:0]
Trailer 6: 1 1 1 0 NodataTimeout[11:6] NoendTimeout[5:0]
Trailer 7: 1 1 1 0 Duplicate Trailer 6[11:0]
Trailer 8: 1 1 1 0 Duplicate Trailer 6[11:0]

Input

CFEB→FIFOs: 40MHz channel link

ALCT/TMB→FIFO: 40MHz LVTTL

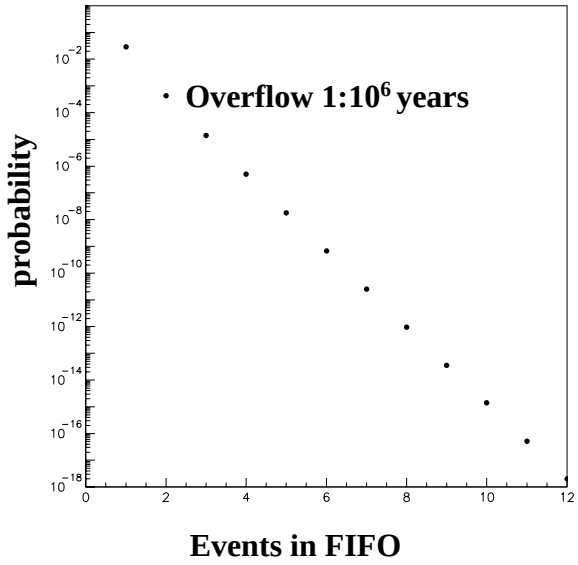
Output

DAQMB→DDU: 80 MHz Glink Fiber

DAQ is Asynchronous
Data is always sent on L1A
N_bx, N_evt for sync check

CSC Event Size

no data 8 bytes
1 CFEB ~2K bytes
5 CFEB ~9K bytes



DAQMB Function: Slow Control

VME A24/D16 in VME64X P1 Backplane

- A[23:19] match with GA[4:0] for specific slot, broadcast.
- A[18:12] is used to address the different slow control paths (devices)
- A[11:1] are specific to the given device

A[18:12] device definition:

00: VME interface FPGA
01: JTAG for CFEB
02: JTAG for Controller FPGA
03: JTAG for Controller PROM
04: JTAG for VME interface PROM
05: Pulser DAC
06: FIFOs
07: DMB ADCs
08: LVMB
09: Flash Memory
… …
0F: Emergency loading of VME PROM

The DAQMB and CFEBs are always VME controllable even after FPGA ISPROM get SEU

DAQMB Function: Slow Control

DAQMB Slow Control

- Programming Prom/FPGA
- Debugging
- CFEB→DAQMB timing
- ALCT/CLCT timing
- Parallel and serial FLASH memories for constants
- Alternative DAQ data path by reading FIFO directly

CFEB Slow Control

- Programming Prom/FPGA
- Calibration Pulse height setting
  monitored by precision ADC (Bur-brown BB7809, 16-bit ADC)
- Voltage and Temperature Readback
- Buckeye Shift Registers (normal,pulsing,kill)

LVMB Slow Control

- Readout Voltage and Currents on LVDB for on-chamber elec.
- On-chamber electronics Power ON/OFF control

DAQMB Function: Fast Control

Custom Backplane carries all Fast Signal

- Local Charged Track (LCT) trigger from TMB.
- TTC → CCB → DAQMB: Clock, L1A, Broadcast and individually addressed command, FPGA reprogram
- The DAQMB fan out the L1A, LCT, Reset, Reprogram signals to CFEBs, monitor the synchronization, etc.

Actions on FPGA reprogram/reset by TTC

- DAQMB FPGA loaded from on-board PROM.
- Timing constants, stored in a serial flash memory (Atmel at45db011), automatically loaded on RESET
- CFEB shift channel masks, stored in a parallel flash memory (Atmel at49bv512), automatically loaded on RESET

DAQMB Function: Board Constants

CFEB constants

- **Buckeye Shift Registers -- normal/pulsing/kill operation 5x6x48 bits**
  - **May want to kill noisy channels for trigger**
- **Trigger Primitives – Timing(3bits), Mode(2bits), Threshold(12bits)**

DAQMB constants

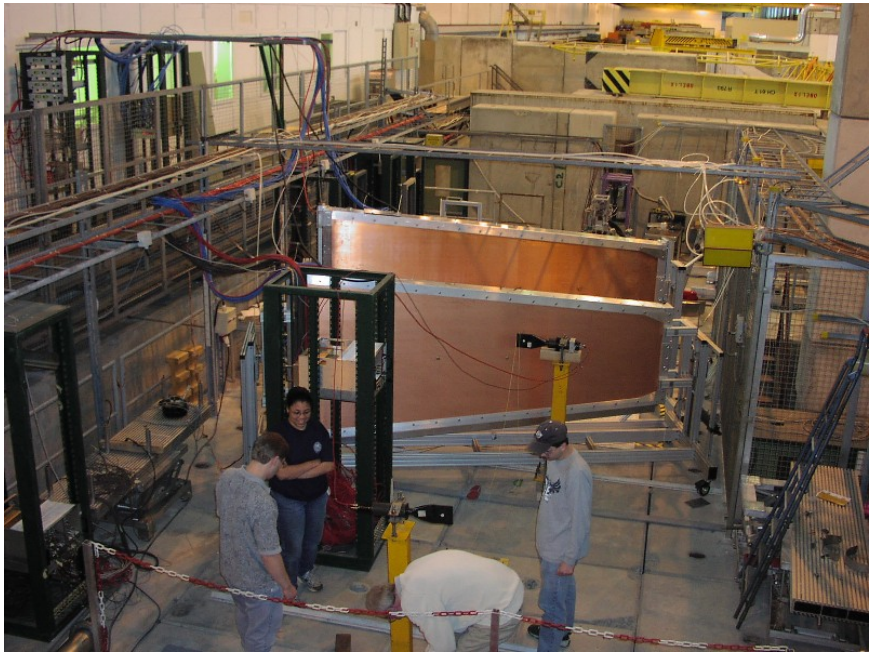
- **Chamber Number 8 bits**
- **Timing Constants 3x 24 bits**

Constants can be set using VME(slow control)
Constants also stored in Flash Memories or Firmware default
Constants will be loaded automatically on power-up or reset

DAQMB tests: 25 ns Structure Beam

Summer 2003, X5A Muon and Pion beams

- **Resets – no issues**
- **Timing – no issues**
- **Backplane communications – no issues**
- **DAQ Readout – no issues**



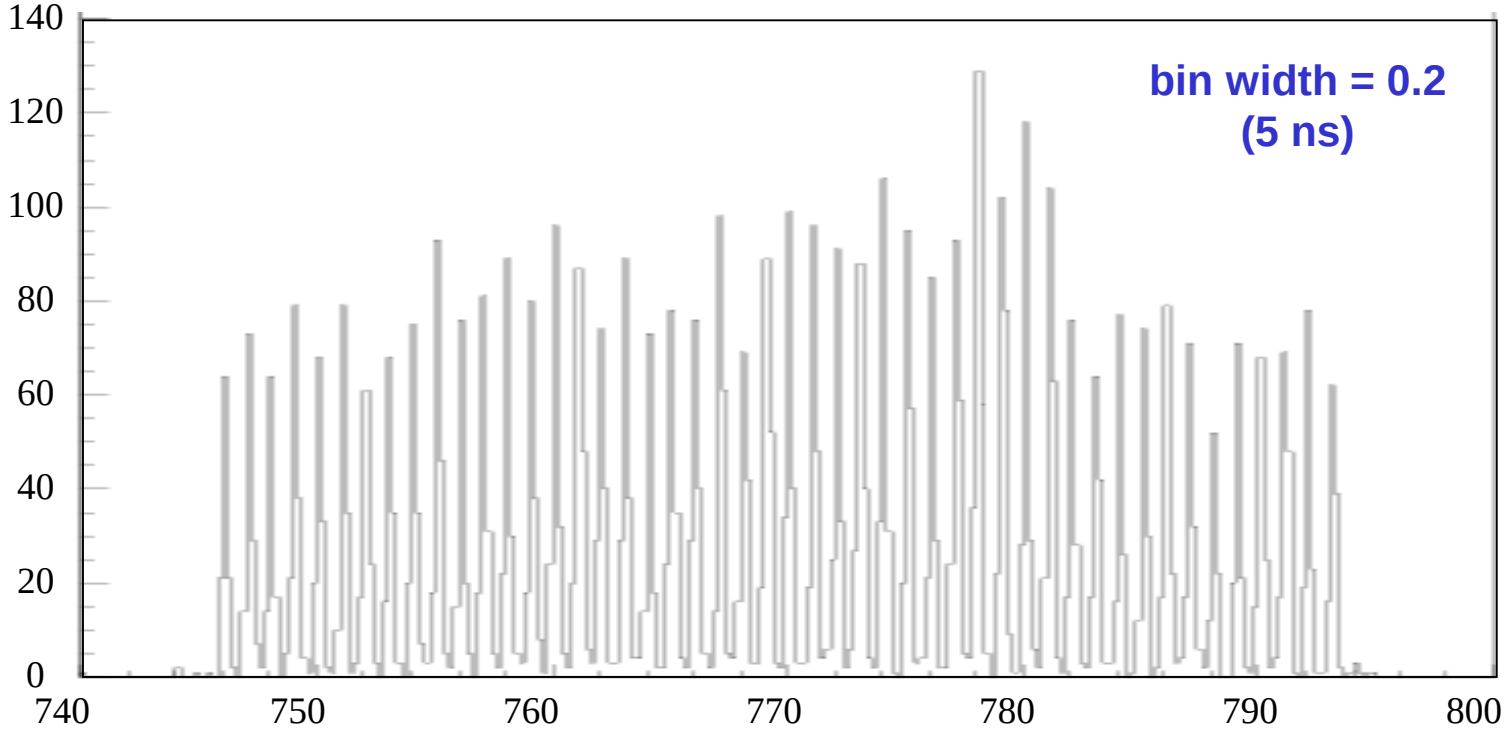
DAQ rate tests carried out with high intensity pion beam.

- **100 KHz L1A (scintillators), 100 KHz LCT, 1 KHz matched L1A-LCT with 16 SCA sample readout. No Problems.**
- **When L1A-LCT matching rate increased to 10 KHz, event got overwritten, DMB out of sync.**
- **Repeat above with 8 sample readout. No problems**

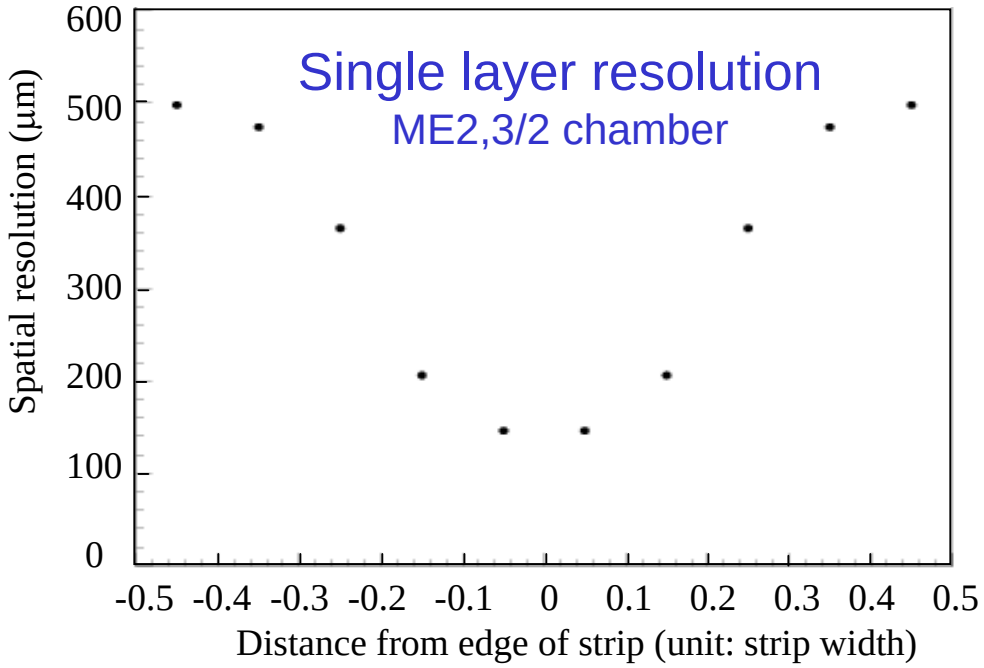
DAQMB tests: 25 ns Structure Beam

Cathode pulse timing (6 layer average)

relative to L1A (beam, scintillators)



DAQMB tests: 25 ns Structure Beam



- Resolution is best for hit near the edge of strip, worst at the center.
- In a CSC, the 6 layers are staggered alternately by ½ strip width. The combined resolution is ~ 100 μm per chamber

DAQMB tests: Fast site test

Older version DAQMBs are used for FAST site chamber test at UC, UF, IHEP, PNPI, ISR, DUBNA

Reliable and Stable over Several Years

All the functions are tested: data acquisition, calibration, slow control, LVMB interface etc.

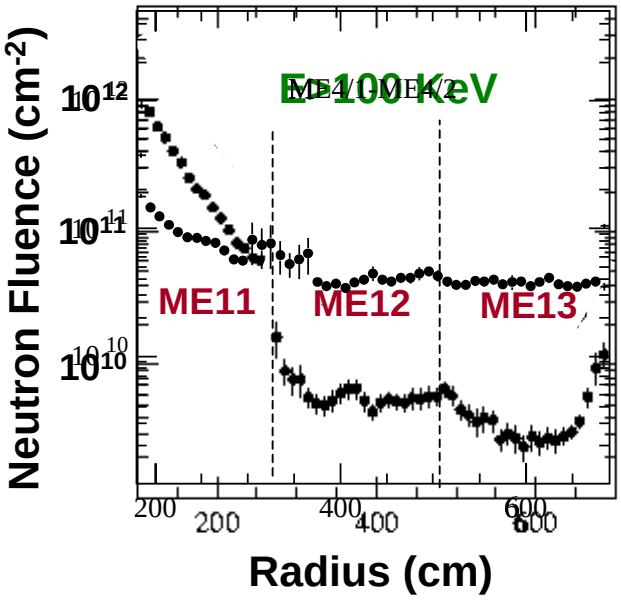
DAQMB tests: Radiation test

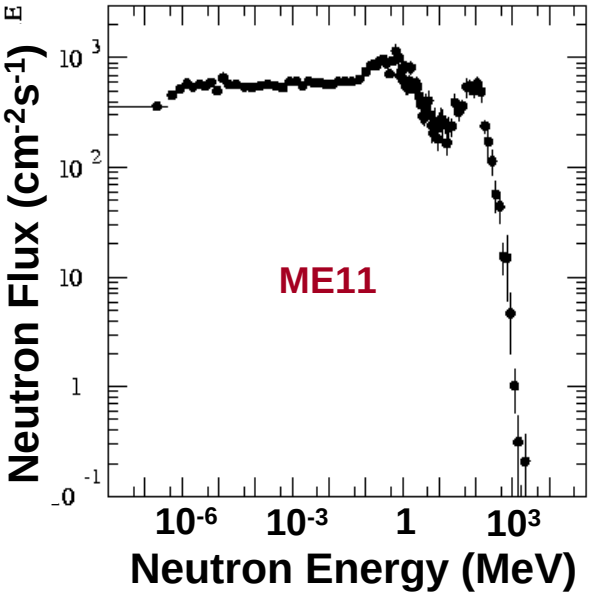
Radiation Levels at Peripheral Crates --**Calculations by *M. Huhtinen***

Integrated over 10 LHC years (5×10^7 s at 10^{34} $cm^{-2}s^{-1}$)

Neutron Fluence (>100 keV): (1 - 4) x 10^{10} cm^{-2}

Total Ionizing Dose: (0.07 – 0.7) kRad



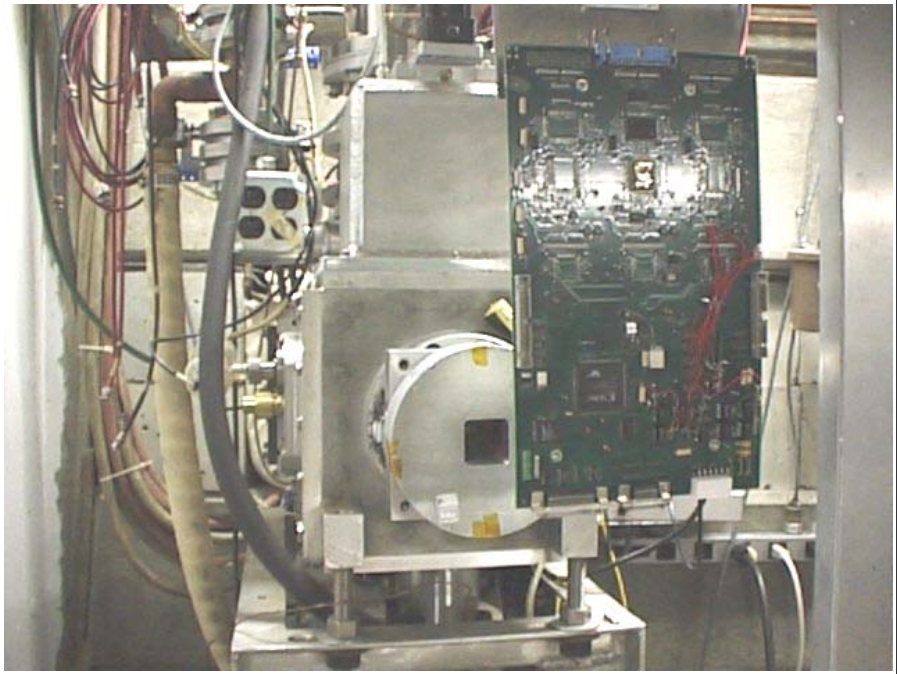


DAQMB tests: Radiation test

Radiation Tests with 63 MeV Protons at UCDavis

2 days in August 2002;

1 day in September 2003



Radiation Test Summary

Device (Function)	Proton Fluence (10^{10} cm^{-2})	Dosage (kRad)	Number of SEU's	SEU Xection (10^{-10} cm^{2})
16K FIFO 72V265	7.45	10	521 bit flips	-
Buffer IDT 74LVC16827	3.72	5	-	-
ADC BB7809	3.72	5	-	-
±10V Reference MAX 680	3.72	5	-	-
-5V Regulator MAX 664	3.73	5	-	-
DAC MAX5154	3.71	5	-	-
ADC MAX1271	3.72	5	-	-
1.5V Regulator Sharp 07VZ01	3.72	5	-	-
Register IDT 74FCT821	3.72	5	-	-
FPGA Virtex II XC2V500	3.72	5+15	9	2.7
Channel Link Receiver	148	200	277	1.9
Delay/Buffer DDD 3d3418	3.72	5	-	-
Ser Flash Mem ATMEL 45DB01	3.72	5	-	-
Spartan II XC2S200	3.72	5	0	0
Desc. Logic. 74LVC10,86,27,04…	3.72	5	-	-
Clock IDT 74LVC74	3.73	5	-	-

DAQMB tests: Radiation test

Cumulative effects

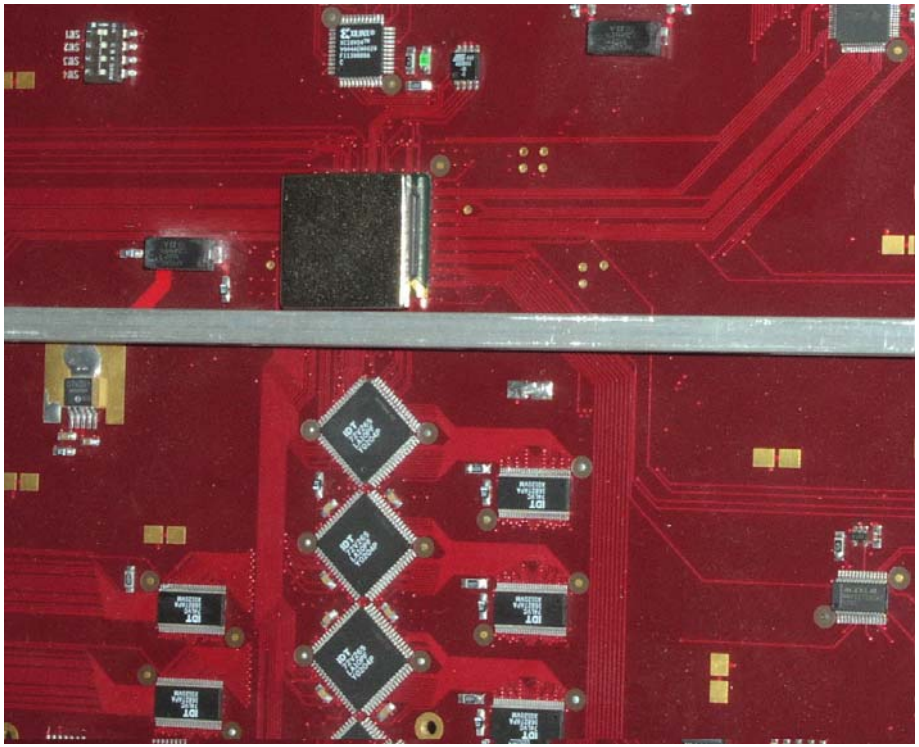
- Total ionization dosage (with 63 MeV protons)
  - No deterioration of performance up to 5 krad
- Displacement damage (with 2×10^{12} cm^{-2} n's @ 1 MeV)
  - Rad-tolerant voltage regulators and references are used

Single-Event Effects

- No latch-up for all chips up to 4×10^{10} p cm^{-2}
- Single Event Upset (SEU) in FPGA
  - All SEU's in FPGA's recoverable by reloading
  - Cross sections measured similar to those on cathode front-end boards, but neutron fluence 10 times lower and number of boards 5 times fewer.

SEU's dominated by FE Electronics ~50:1
FE Electronics resets will also reset DAQMB

DAQMB tests: Magnetic Field test



No magnetic effects observed

< 4 kGauss at Peripheral Crates

Rare Earth Magnet Rated 12 kG, Measured 4 kG (0.5 cm)

Run the Magnets over each component, while taking calibration data, no data interruption (or corruption) is seen. (checked by CRC)

Put the magnet on the oscillator, no frequency change is observed

Put on the delay chip, no delay change is observed

DAQMB procedures: Test Bench

- VME emergency load the VME interface PROM
- VME load the controller PROM
- Load in board ID

- Load in parameters (CFEB clock delay, CFEB hot channel mask, etc)
- Cable length detect,
- Every time after RESET, the DAQMB will be in a ready state

DAQMB Procedures: Peripheral crate installation

DAQMB Timing adjustment

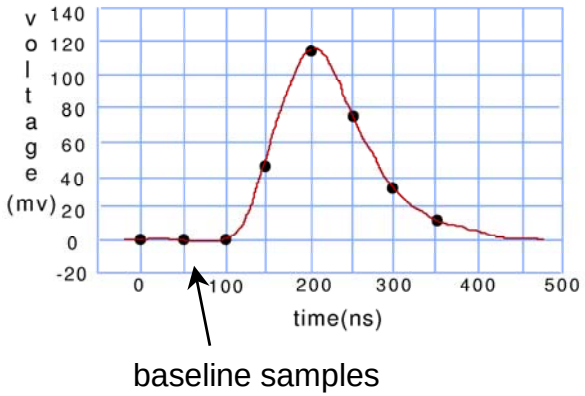
DAQMB data acquisition asynchronous

- Trigger/Beam Crossing timing on TMB/ALCT
- LCT,L1A, and Data Available from CFEBs timing
- Variations due to CFEB to DAQMB cable lengths
- Cable lengths fixed for given chamber
- Calibration timing

DAQMB timing constants easily determined remotely

- Slow Control VME: CFEB TIming
  - Pulse CFEBs, LCT/L1A from TMB/TTC
  - Vary timing and check data is latched

Position 8 time samples with two baseline samples available at beginning of pulse



DAQMB Procedures: LHC run

Startup

- No need to do anything
- VME to CCB issues backplane reprogram/reset loads constants
- Single LCT(TTC or Slow Control) will verify DAQMB running properly

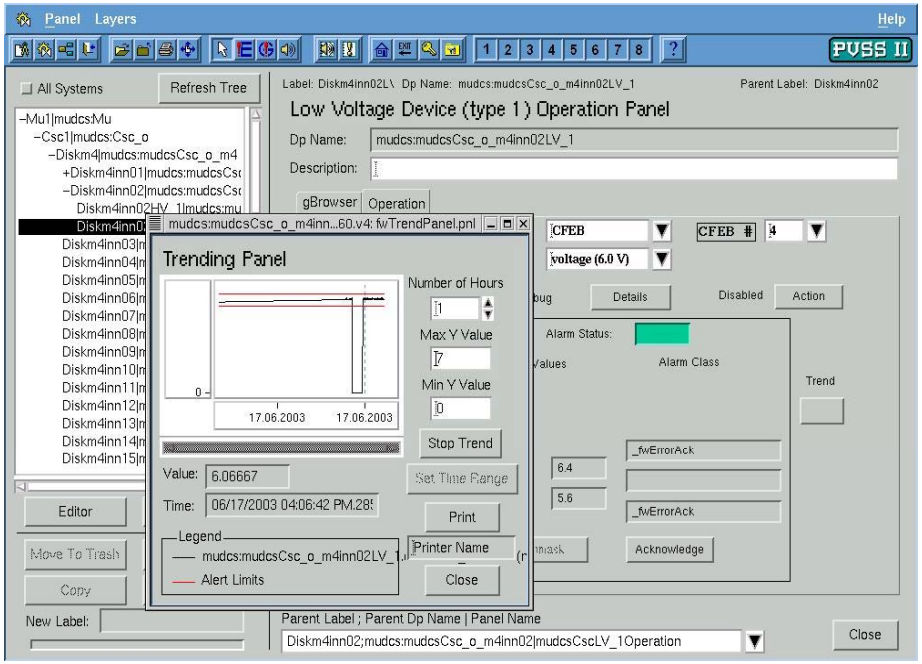
SEU Reprogram/Reset (Every 15 minutes)

- TTC -> CCB issues backplane reprogram/reset -> loads constants

DDU will monitor DAQMB status continually

- Will request Reprogram/Reset thru FMM

Slow Control VME will access LVMB voltages, DAQMB&CFEB temp. during data taking



Production preparation: Numbers

- How many boards do we need?

ME 1/2, 1/3, 2/1, 2/2, 3/1, 3/2	360
ME 1/1	72
ME 4/1	36
SubTotal	468
10% spare boards	47
Total boards producing	515
10% spare parts	

- The Ohio State University will maintain the DAQMB,
- 10% of spare boards will be built for anticipated swapping,
- 10% spare parts will be ordered for board repair

Production preparation: test setup

PC boards will be etched and stuffed commercially

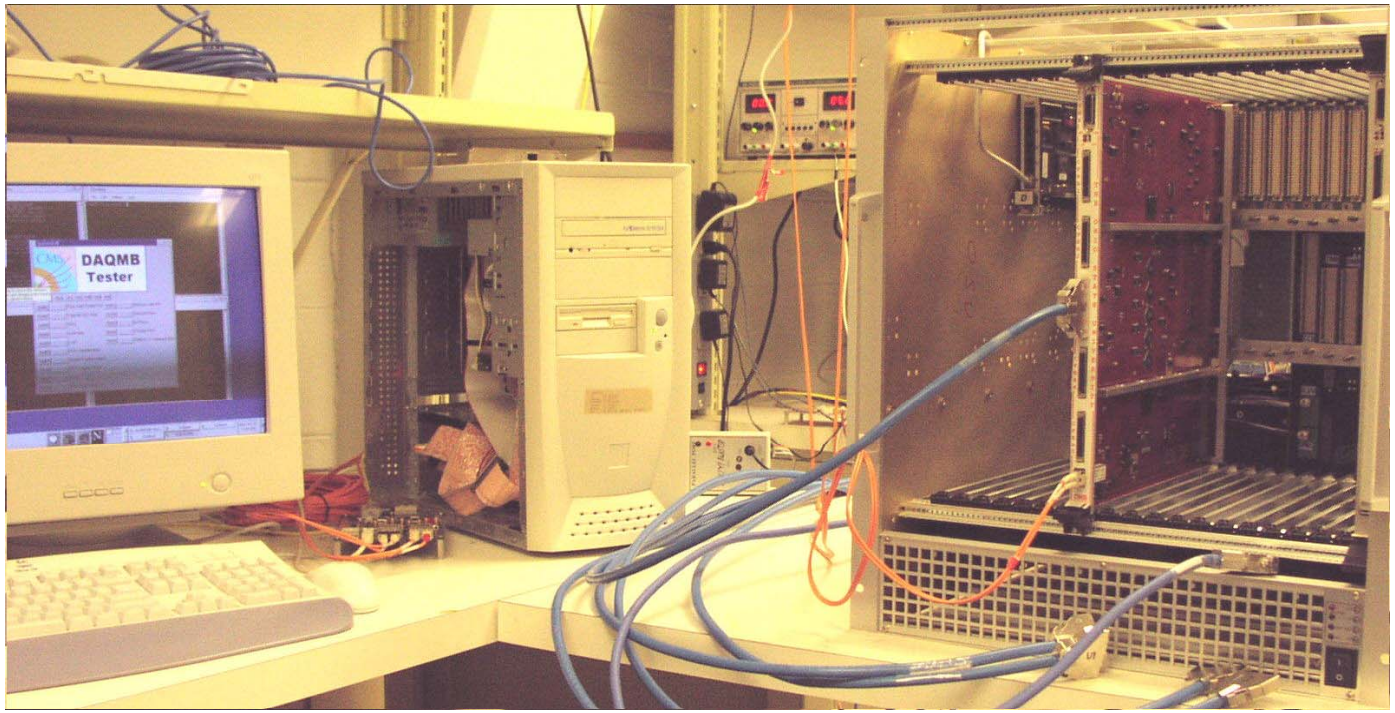
Boards will be measured and debugged on computerized tester before and after burn-in at OSU

Each board will have a unique ID

Board tracking: Microsoft Access

Production Test and Debugging

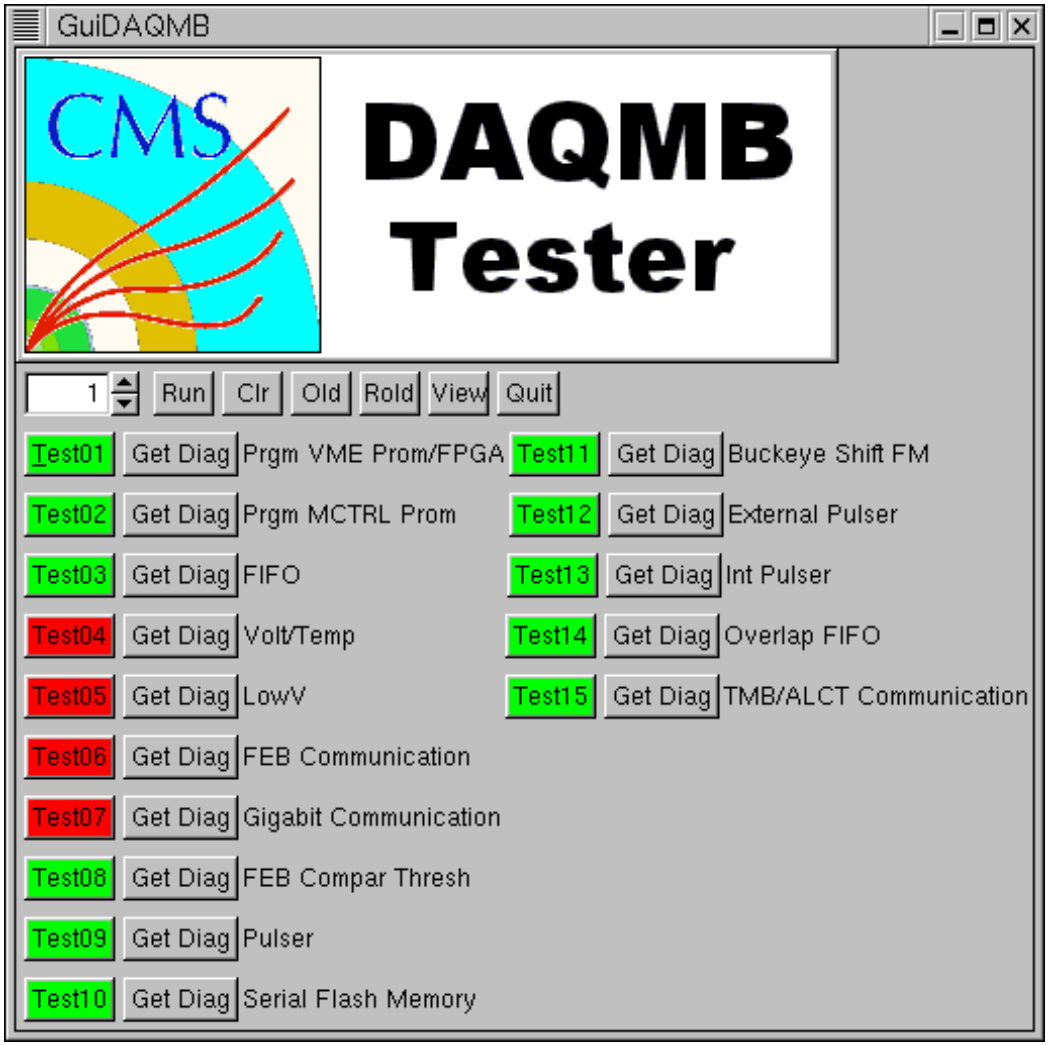
-Testing Station checks all input and output signals by computer
-Exercise 5 CFEB's and LVMB
-CCB,TMB signals mimicked by FPGA on backplane



Test Station Built and Working

Production preparation: test setup

Production Test Software written and tested.



Production preparation: Burn in

Burn In

CDF: 50-60 C for 8-24 Hrs
Sufficient for tantalums failures
No sensitivity to semiconductor failure

US Military: 125 C for 320 Hrs
Chip Makers recommend against this

CFEB: 65 C for 24 Hrs
Prove to be effective, not damaging

Each DMB: 65C for 24 Hrs

Test Before and After

Production preparation: Validation

-11 DAQMB ordered (October 8, 2003)

-One board is stuffed and tested. The PCB manufacture is OK, actually, it is the same company producing the CFEBs

- Ten Boards will be stuffed commercially to test the ball grid arrays and wave-soldering

A full load of peripheral crate will be tested sometime later this year, although we tested multiple boards in one crate.

DAQ MotherBoard Meets All Design Specifiations!

We are ready to procure the 515 DAQMB at The Ohio State University

Documentation for DAQMB

http://www.physics.ohio-state.edu/~cms/dmb/esr/

DAQMB User's Manual
DAQMB ESR at CERN (Powerpoint)
DAQMB-CFEB Software Manual
PCB schematic design
VME interface FPGA design
Controller FPGA design
SVF files for FPGA designs
Data Format