EMU Peripheral Crate Controller

Data Formats

Warning: The contents of this document are preliminary and are subject to change without notice!

Rev. 1.05

Document Revsion	Document Date	Firmware Revision	Firmware Date	Changes
1.01	6/29/2005			Fixed typoes in examples page (in VME control word).
1.02	7/8/2005	2.18	7/8/2005	Added new function codes and return data types corresponding to firmware version 2.18.
1.03	7/12/2005			Note that function codes 0x05 - 0x16, 0x21, and 0x23 are not yet implemented. Also return data header formats are not yet implemented as shown in this document.
1.04	9/29/2005	3.06	8/31/2005	Return data header format in firmware revision 3.06 and later now matches the format described in this document (except AK/Status codes are not yet implemented). Flash memory functions added (0x05 - 0x16). Separate path for spontaneous packets now implemented (Errors, Warnings, Info, and Interrupts) although interrupt handling is not yet implemented.
1.05	10/26/2005	3.06	8/31/2005	Configuration register bits specified; Restriction on MAC addresses detailed.

Ethernet Packet Format

Mnemonic	Meaning	Size (bytes)	Code/Value
SOP	Start of Packet	1	0xFB
Preamble	Bit patttern for synchronization.	7	6(0x55)(0xD5)
SOF	Start of Frame (last byte of preamble)	1	0xD5
MAC Dest.	Destination MAC address	6	Hardware Defined
MAC Src.	Source MAC address	6	Hardware Defined
LEN	Length of User Data in bytes	2	2-9000
User Data	User specified data	46-9000	User defined
CRC	Cyclical Redundency Check	4	Packet defined
EOP	End of Packet	1	0xFD

User Data Format

There are 3 general user data formats for the following 3 cases:

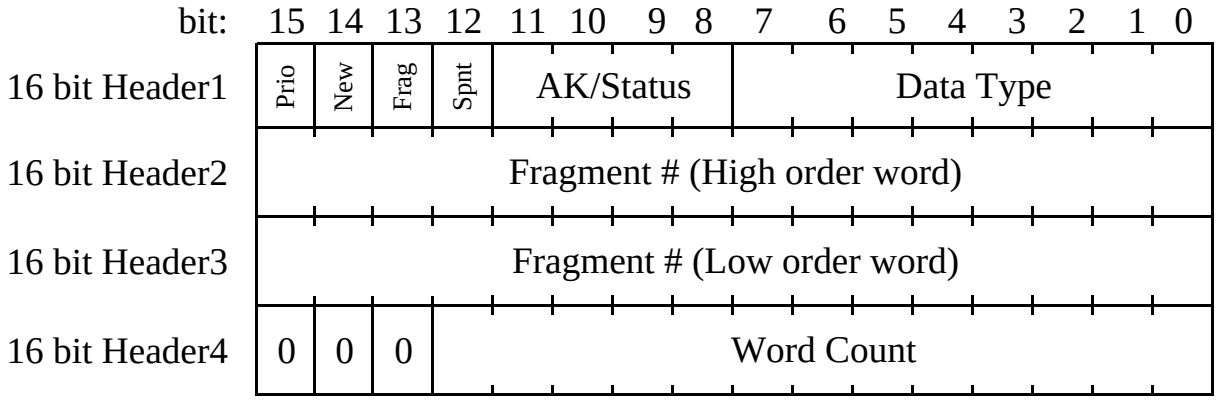
1) Packets sent to the controller.
2) Packets returning from the controller (with PROTOCOL disabled).
3) Packets returning from the controller (with PROTOCOL enabled).

Sequence (16 bit words)	Sent to	Received from (PROTOCOL disabled)	Received from (PROTOCOL enabled)
0	Header	Command Dependent Data	Header1
1	Command Dependent Data	Command Dependent Data	Header2
2	Command Dependent Data	Command Dependent Data	Header3
3	Command Dependent Data	.	Header4
4	.	.	Command Dependent Data
5	.	.	Command Dependent Data
6	.	.	Command Dependent Data
.	.	.	.
.	.	.	.
.	.	.	.

Header Formats

For packets sent to the controller:

For packets retruned from the controller:



Definitions of labels and abbreviations

Rsvd.	:	Reserved.
Prio.	:	Priority packet. To be executed or returned out of sequence ASAP.
AK/RQ	:	Acknowledgement of command execution is requested.
Controller Command	:	Function code to be executed: Data format is dependent upon this code.
New	:	Indicates that this is the first packet in a series of 1 or more packets.
Frag.	:	Indicates that the amount of data exceeds the maximum packet size. This packet contains only a fragment of the requested data.
Spnt.	:	Indicates that this packet was spontaneously generated by the controller and was not in response to a request.
AK/Status	:	Acknowledgement status. Indicates disposition of the requested function.
Data Type	:	Indicates the type of data contained in this packet. The data format is dependent upon this type.
Fragment #	:	A 32 bit number specifying this packets position in a sequence of packet fragments.
Word Count	:	The number of data words to follow the header.

Function Codes

Cat.	Mnemonic	OpCode	Functional Description	Data Format
Initialization/Configuration	Funct_NoOp	0x00	No action taken.	no data
	Set_FF_Test	0x01	Set test mode for external FIFO.	no data
	Set_FF_VME	0x02	Set VME mode for external FIFO.	no data
	ECC_enable	0x03	Enable Error Correcting Codes in external FIFO	no data
	ECC_disable	0x04	Disable Error Correcting Codes in external FIFO	no data
	Save_Cnfg_Num	0x05	Save current controller configuration as specified configuration number.	1 word
	Read_Cnfg_Num_Dir	0x06	Direct readback of specified stored configuration (raw data from Flash mem).	1 word
	Read_Cnfg_Num_Dcd	0x07	Decoded readback of specified stored configuration.	1 word
	Rstr_Cnfg_Num	0x08	Restore controller configuration to specified configuration.	1 word
	Set_Cnfg_Dflt	0x09	Set default controller configuration to specified number.	1 word
	Read_Cnfg_Dflt	0x0A	Readback the default configuration number.	no data
	Set_MACs	0x0B	Set MAC addresses.	4-17 words[1]
	Read_MACs_Dir	0x0C	Direct readback of stored MAC addresses (raw data from Flash mem).	no data
	Read_MACs_Dcd	0x0D	Decoded readback of stored MAC addresses.	no data
	Read_CRs	0x0E	Readback configuration registers (CR's).	no data
	Wrt_Eth_CR	0x0F	Write Ethernet CR with specified data.	1 words[2]
	Wrt_Ext_CR	0x10	Write External FIFO CR with specified data.	1 words[2]
	Wrt_Rst_CR	0x11	Write reset enables CR with specified data.	1 words[2]
	Wrt_VME_CR	0x12	Write VME CR with specified data.	2 words[2]
	Wrt_BTO_CR	0x13	Set VME Bus Timeout to specified data.	1 words[2]
	Wrt_BGTO_CR	0x14	Set VME BusGrant Timeout to specified	1 words[2]
	Wrt_All_CRs	0x15	Write all CR's and timeouts with specified	5 words[2]
	Set_Clr_CRs	0x16	Set or Clear individual bits of a CR.	2-3 words[2]
	Set_Inj_Err	0x17	Enable error injecting into FIFO data bits	no data
	Rst_Inj_Err	0x18	Disable error injecting into FIFO data bits	no data
	Warn_On_Shdwn	0x19	Enable warning packets prio to reloading.	no data
	No_Warn_On_Shdwn	0x1A	Disable warning packet on shutdown.	no data
		0x1F	Undefined	--

Function Codes Continued

Cat.	Mnemonic	OpCode	Functional Description	Data Format
VME functions	VME_Cmds	0x20	Specified data are VME commands and are sent through external FIFO.	VME_DAT_FMT
	VME_Cnfg	0x21	Specified data are VME configuration commands and are sent through external FIFO.	VME_CNFG_FMT
	VME_Dir_Cmds	0x22	Specified data are VME commands and are sent directly to VME interface.	VME_DAT_FMT
	VME_Dir_Cnfg	0x23	Specified data are VME configuration commands and are sent directly to VME interface.	VME_CNFG_FMT
		0x24	Undefined	--
		.	Undefined	--
		.	Undefined	--
		.	Undefined	--
		0x2F	Undefined	--
Undefined		0x30	Undefined	--
		.	Undefined	--
		.	Undefined	--
		.	Undefined	--
		0xDF	Undefined	--
External FIFO Testing and Programming	Wrt_Ext_FF	0xE0	Write specified data to external FIFO.	N words[3]
	Prg_Ext_Off	0xE1	Program offsets for external FIFO. (18-bit full offset, then 18-bit empty offset)	2 longwords[4,5]
	Rdbk_Ext_Off	0xE2	Readback offsets from external FIFO.	no data
	PRst_Ext_FF	0xE3	Partial reset of external FIFO.	no data
	Rd_Ext_FF	0xE4	Read specified number of words from external FIFO.	1 longword[4]
	RT_Ext_FF	0xE5	Retransmit specified number of words from external FIFO.	1 longword[4]
	MRst_Ext_FF	0xE6	Master reset of external FIFO.	no data
	ST_MK_Ext_FF	0xE7	Set MARK at current read pointer location.	no data
	RST_MK_Ext_FF	0xE8	Reset MARK; restore normal operation	no data
	Rst_Ext_Err_Cnt	0xE9	Reset FIFO data bit error counters.	no data
	Rd_Ext_Err_Cnts	0xEA	Readback FIFO data bit error counters.	2 longwords[4,6]
		0xEB	Undefined	--
		.	Undefined	--
		0xEF	Undefined	--

Function Codes Continued

Cat.	Mnemonic	OpCode	Functional Description	Data Format
Test and Diagnostic		0xF0	Undefined	--
		.	Undefined	--
		.	Undefined	--
		0xF8	Undefined	--
	Force_Reload	0xF9	Force reprogramming the FPGA.	no data
	Read_Drop_Mem	0xFA	Read all words from logic analyzer circular buffer A.	no data
	Read_WSOP_Mem	0xFB	Read all words from logic analyzer circular buffer B.	no data
	Flash_R_W	0xFC	Read or Write Flash memory. Data contains commands for Flash interface.	FLASH_FMT
	Send_N_Words	0xFD	Request specified number of words be sent from the controller.	1 longword[4]
	Load_User_Reg	0xFE	Load the 32 bit LED user register with specified data.	1 longword[4]
	Loopback	0xFF	Transmit the data in this packet back to sender as is.	N words[3]

[1]See MAC_FMT for details.

[2]See CR_FMTs for details.

[3]The number of words are defined by LEN in the MAC frame header.

[4]High order word sent first, with unused high order bits padded with zeros.

[5]Two words for the FULL offset come first followed by two words for the EMPTY offset.

[6]Two words for the uncorrected errors come first followed by two words for the corrected errors.

Function Specific Sub Formats

(After Header)

FLASH_FMT

Sequence (16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	Number of Pages (NP: 1-128)							
1	W[1]	Page Number (0-127)							C[2]	Number of Bytes (NB1: 1-64)						
2	0	0	Byte Address (0-63)						Data							
3	0	0	Byte Address (0-63)						Data							
4	0	0	Byte Address (0-63)						Data							
.	0	0	.						.							
.	0	0	.						.							
.	0	0	.						.							
(NB1+1)+1	W[1]	Page Number (0-127)							C[2]	Number or Bytes (NB2: 1-64)						
(NB1+1)+2	0	0	Byte Address (0-63)						Data							
(NB1+1)+3	0	0	Byte Address (0-63)						Data							
(NB1+1)+4	0	0	Byte Address (0-63)						Data							
.	0	0	.						.							
.	0	0	.						.							
.	0	0	.						.							
NB2+1)+(NB1+1)+1	W[1]	Page Number (0-127)							C[2]	Number or Bytes (NB3: 1-64)						
NB2+1)+(NB1+1)+2	0	0	Byte Address (0-63)						Data							
NB2+1)+(NB1+1)+3	0	0	Byte Address (0-63)						Data							
NB2+1)+(NB1+1)+4	0	0	Byte Address (0-63)						Data							
.	0	0	.						.							
.	0	0	.						.							
.	0	0	.						.							

First Page / Second Page / Third Page

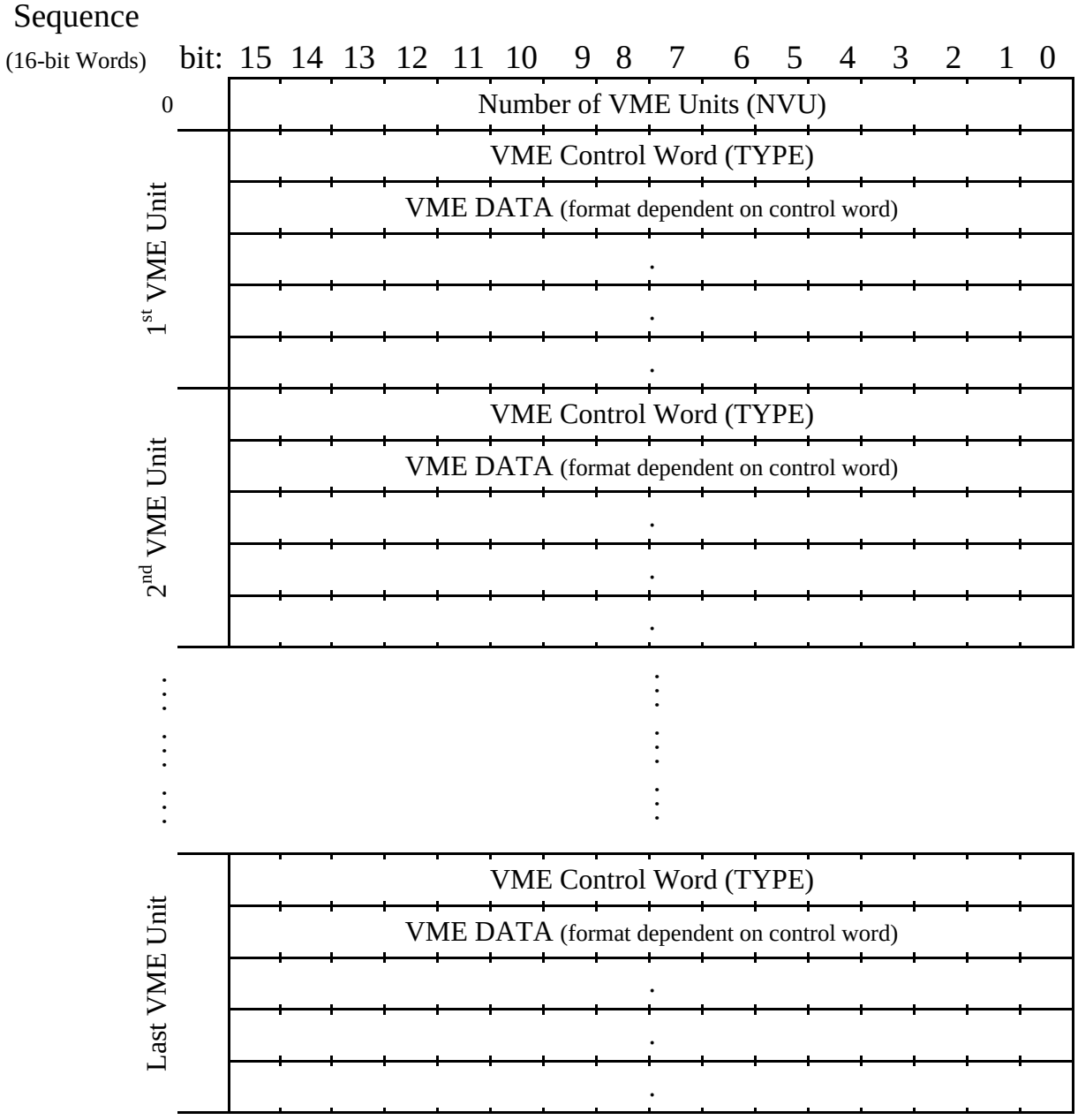
[1]W=1: write to specified page; W=0 : read from specified page.

[2]This bit is ignored on writes (W=1). When W=0; C=0 indicates that data readback is to be directed to the GbE transmitter; C=1 indicates that data readback is to be directed to the configuration registers.

Function Specific Sub Formats

(After Header)

VME_DAT_FMT



VME Unit Format

VME Control Word

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Rsvd.	Rsvd.	Rsvd.	Rsvd.	Rsvd.	Dly_Typ			Addr_Sz			Wrt_RdB	Data_Sz		Trns_Typ	

Transfer Types

Trns_Typ Code	Mnem.	Meaning
0	SNGL	Single transfer
1	BLOCK	Block transfer
2	RMW	Read Modify Write sequence
3	UNALG	Unaligned transfer (16-bits crossing word boundries)

Data Sizes

Data_Sz Code	Mnem.	Size	Number of supplied/expected words
0	D08	8 bits	1
1	D16	16 bits	1
2	D32	32 bits	2
3	D64	64 bits	4

Write Control

Wrt_RdB Value	Meaning
0	Read data from specified VME address.
1	Write data to specified VME address

Address Sizes

Addr_Sz Code	Mnem.	Size	Number of supplied/expected words
0	-	-	undefined
1	A16	16 bits	1
2	A24	24 bits	2
3	A32	32 bits	2
4	A40	40 bits	3
5	A64	64 bits	4
6	-	-	undefined
7	-	-	undefined

Delay Types

Dly_Typ Code	Mnem.	Clock Period	Num bits	Max Count	Max Delay	Comment
0	No_Dly	-	-	-	-	
1	D4nsX16	4 ns	16	65535	262,144 us	4 ns modes are disabled. If used, 2 bits are dropped and 16 ns clock is used.
2	D16nsX16	16 ns	16	65535	1.049 ms	
3	D16usX16	16.384 us	16	65535	1.074 s	
4	D4nsX32	4 ns	32	4.29E+09	17.18 s	4 ns modes are disabled. If used, 2 bits are dropped and 16 ns clock is used.
5	D16nsX32	16 ns	32	4.29E+09	68.72 s	
6	D16usX32	16.384 us	32	4.29E+09	1.95 hr	
7	undefined	undefined	-	undefined	undefined	

Note: The format of the data following the VME control word is dependent on the options specified in the control word. Please refer to the following pages for the details.

VME Control Word Dependent Data Format

Non Block Transfers: (Dly_Typ = 0 and Trns_Typ = SNGL, RMW, or UNALG)

Section / Order	Data Specified	Comments
Address Section:	1-4 Words	Dependent on Addr_Sz.
Data Section:	0-4 Words	Dependent on Wrt_RdB and Data_Sz.

Block Transfers: (Dly_Typ = 0 and Trns_Typ = BLOCK)

Section / Order	Data Specified	Comments
Address Section:	1-4 Words	Dependent on Addr_Sz.
Data Count:	1 Word (n)	Number of Data_Sz transfers.
Data Section:	0-4n Words	Dependent on Wrt_RdB, Data_Sz, and Data Count. 0-4 words repeated n times.

Delays: (Dly_Typ = Non-Zero and Trns_Typ = don't care)

Section / Order	Data Specified	Comments
Delay Section:	1-2 Words	Dependent on Dly_Typ.

Address Section:

	Addr_Sz				
Seq.	A16	A24	A32	A40	A64
0	Addr(15:0)	0x00Addr(23:16)	Addr(31:16)	0x00Addr(39:32)	Addr(63:48)
1	-	Addr(15:0)	Addr(15:0)	Addr(31:16)	Addr(47:32)
2	-	-	-	Addr(15:0)	Addr(31:16)
3	-	-	-	-	Addr(15:0)

Data Section:

	Reads	Data_Sz (for writes Wrt_RdB = 1)			
Seq.	Wrt_RdB = 0	D08	D16	D32	D64
0	-	0x00Data(7:0)	Data(15:0)	Data(31:16)	Data(63:48)
1	-	-	-	Data(15:0)	Data(47:32)
2	-	-	-	-	Data(31:16)
3	-	-	-	-	Data(15:0)

Delay Section:

	Dly_Typ	
Seq.	D4nsX16 D16nsX16 D16usX16	D4nsX32 D16nsX32 D16usX32
0	Delay(15:0)	Delay(31:16)
1	-	Delay(15:0)

Return Data Types

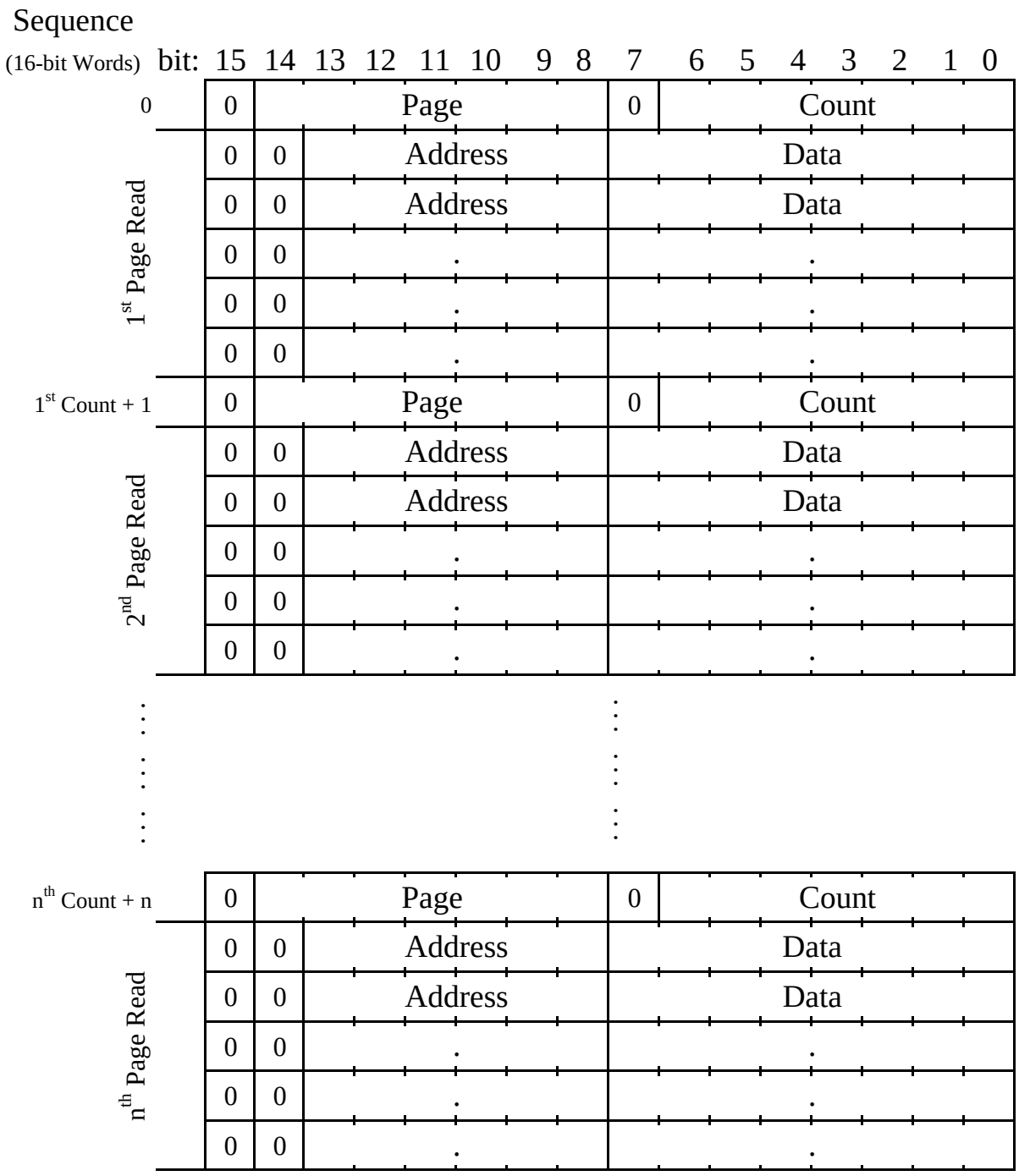
Code	Data Type		Words per Data Unit
0	No data		0
1	Loopback data		1
2	TX_N_Words requested data		1
3	External FIFO data or offsets		mixed[1]
4	VME D08 data	Type = {01,Data_Sz} (4+Data_Sz)	1
5	VME D16 data		1
6	VME D32 data		2
7	VME D64 data		4
8			
9			
10			
11	Flash readback data		mixed[2]
12			
13	Information packet		1
14	Warning packet		1
15	Error packet		1

[1]External FIFO Offset Data Format (two 18-bit words):

Sequence (16-bit Words)	bit: 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	b17	b16
1	Full Offset(15:0)															
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	b17	b16
3	Empty Offset(15:0)															

[2]Flash Readback Data Format (see following page):

Flash Readback Data Format:



Examples

Example 1: VME commands for 2 A24D16 single writes, a delay, and then an A24D16 single read.

		Sequence of 16 bit words (HEX)	Meaning
	Header	2020	Function is VME Comands with ackowlegment request
	NVU	0004	Number of VME units
1st VME Unit	Control Word	0054	A24D16 Single Write
	Address	00A(23:16)	High order byte of VME address
		A(15:0)	Low order word of VME address
	Data	D(15:0)	Data word to write
2nd VME Unit	Control Word	0034	A24D16 Single Write
	Address	00A(23:16)	High order byte of VME address
		A(15:0)	Low order word of VME address
	Data	D(15:0)	Data word to write
3rd VME Unit	Control Word	05XX	16 ns by 32 bit delay
	Data	Dly(31:16)	High order word of delay
		Dly(15:0)	Low order word of delay
4th VME Unit	Control Word	0044	A24D16 Single Read
	Address	00A(23:16)	High order byte of VME address
		A(15:0)	Low order word of VME address

Configuration Bits: Definitions and Defaults

Ethernet Configuration Register

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Bit definitions	reserved								switch control	spont. pkt ena	carrier extend	protocol enable	promisc.	passthru	tdis	tx inhibit	
Firmware default	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	(0x0050)

switch control : When set, ethernet configuration is under front panel switch control, (otherwise register control).

spont. pkt ena : Enables the controller to send spontaneous packets for errors, warnings, information, and interrupts, otherwise no packets will be sent that are not in response to a request for

carrier extend : For use in half duplex mode at speeds above 100 Mb/s to ensure proper operation of the CSMA/CD protocol (1000 BASE-T).

protocol enable : Specifies whether or not packets sent from the controller are sent with a header. When protocol is enabled, headers are included.

promisc. : Puts controller in promiscuous mode. In this mode the controller accepts all MAC addresses.

passthru : Puts controller in pass-thru mode. In this mode the controller returns the user data portion of all accepted packets received back to the sender without executing any instructions. A header is added if the protocol enable bit is set.

tdis : Disables the transmit side of the optical transceiver. Any established link will be lost. It is suggested that this bit be kept set to zero.

tx inhibit : Disables the transmit side of the RocketIO™. This prevents Idles from being transmitted and therefore any established link will be lost. It is suggested that this bit be kept set to zero.

External FIFO Configuration Register

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Bit definitions	reserved													Inject Errors	ECC enable	Test Mode	
Firmware default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	(0x0002)

Inject Errors : Injects errors into data written to the external FIFO for testing ECC function.

ECC enable : Enables Error Corrceting Codes to be used in the external FIFO.

Test Mode : When set, enables reading the external FIFO. When not set, data in the FIFO will be read by the VME controller.

Configuration Bits: Definitions and Defaults (Continued)

Reset Enables/Misc. Configuration Register

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Bit definitions	reserved									Send Pkt on Strt	Warn on Shtdwn	JTAG	Hard Reset	SYSRST	Front Panel	Internal	
Firmware default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	(0x0013)

Send Pkt on Strt : Enables an INFO packet to be sent after power-up or reprogramming informing the server that the controller is ready.

Warn on Shtdwn : Enables a Warning packet to be sent informing the server of an impending shutdown/reprogram. The server should stop sending commands to the controller.

JTAG : Enables resets via the CF pin on the program PROM. Used when loading new

Hard Reset : Enables resets via the CMS/EMU Hard Reset line.

SYSRST : Enables resets via the VME backplane SYSRST signal.

Front Panel : Enables resets via the front panel push button switch.

Internal : Enables resets via a command sent in an Ethernet packet.

Configuration Bits: Definitions and Defaults (Continued)

VME Configuration Register

High Order

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Bit definitions	reserved				IH Req. Level		IH Req. Type		rsvd	Interrupt Levels							
Firmware default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	(0x0000)

Low Order

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Bit definitions	rsvd	rsvd	Arbiter Type		Master Req. Level		Master Req. Type		User Defs	Interrupt Handler	Location Mon.	Slave enable	Arbiter enable	BTO enable	SYSCLK enable	Master enable	
Firmware default	0	0	0	1	1	1	0	1	0	0	0	1	1	1	1	1	(0x1D1F)

IH Req. Level : Specifies the bus request level for the Interrupt Handler's (IH) requester (0-3).

IH Req. Type : Specifies the bus requester type for the Interrupt Handler.
- 0: Release On Request (ROR)
- 1: Release When Done (RWD)
- 2: Fair ROR requester.
- 3: Fair RWD requester.

Interrupt Levels : Specifies the Interrupt ReQuest lines (IRQ's) that the IH services.

Arbiter Type : Specifies the Arbiter type.
- 0: No arbitration (disabled).
- 1: SinGle Level arbiter (SGL), uses BR3.
- 2: PRIoritized arbiter (PRI).
- 3: Round Robin Select arbiter (RRS).

Master Req. Level : Specifies the bus request level for the VME Master's requester (0-3).

Master Req. Type : Specifies the bus requester type for the VME Master.
- 0: Release On Request (ROR)
- 1: Release When Done (RWD)
- 2: Fair ROR requester.
- 3: Fair RWD requester.

User Defs : Enables the user defined I/O buffers on J2 signals.

Interrupt Handler : Enables the Interrupt Handler. (not implemented yet)

Location Mon. : Enables the Location Monitor. (not implemented yet)

Slave enable : Enables the Slave. The slaves functions are currently only for testing purposes.

Arbiter enable : Enables the Arbiter.

BTO enable : Enables the Bus Timer. The time out value can be set by the user.

SYSCLK enable : Enables the VME SYSCLK on the backplane (16 MHz).

Master enable : Enables the VME Master.

Assigning MAC Addresses

Notes on Representations:

Hexadecimal Representation:

MAC addresses are 48-bit addresses grouped into six octets. The standard representation of a MAC address is the hexadecimal representation (as defined by IEEE STD 802[1]) which is a string of six octets (in Hex) separated by hyphens, for example: AC-DE-48-00-00-80.

The ordering of the octets is as follows: octet0-octet1-octet2-octet3-octet4-octet5.

Bit-reversed Representation:

An alternative representation that is sometimes used (in the context of IEEE 802.5) is the bit-reversed representation in which the bits in each octet are reversed. In this representation the octets are separated by colons. The MAC address for the example used above in bit-reversed representation is 35:7B:12:00:00:01.

The ordering of the octets is unchanged: octet0:octet1:octet2:octet3:octet4:octet5.

Beware! Source of Confusion:

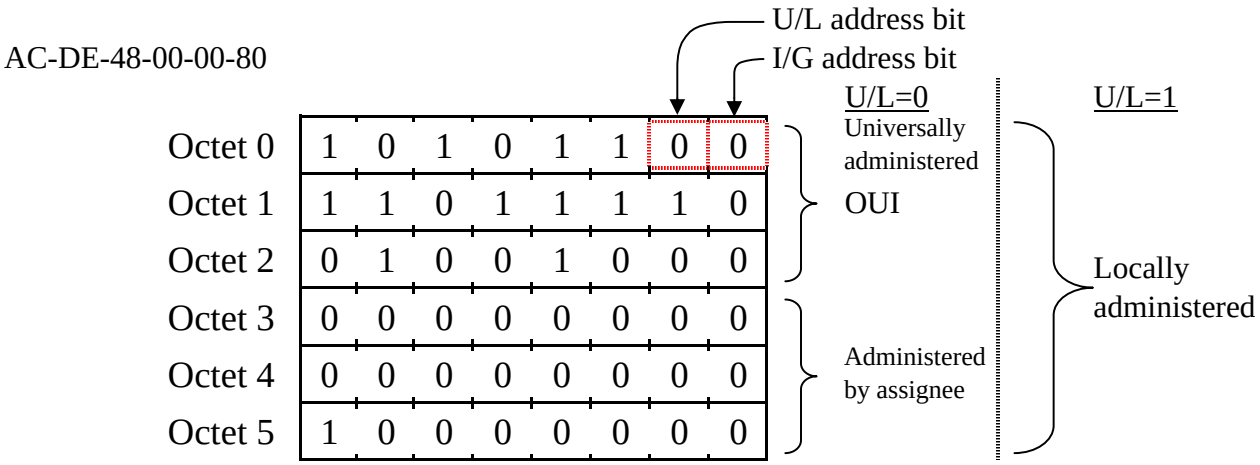
Often, MAC address are written or displayed in the hexadecimal representation but the octets are separated by colons! One example of this is the Linux /sbin/ifconfig command. In documentation and software for the Gigabit Ethernet VME Controller, the hexadecimal representation will always be intended (and should be assumed) regardless of the separater actually used.

[1]IEEE Standard for Local and Metropolitan Area Networks: Overview and Architecture, The Institute of Electrical and Electronics Engineers, Inc.; 2002. (Print: ISBN 0-7381-2940-2 SH94947; PDF: ISBN 0-7381-2941-0 SS94947)

Assigning MAC Addresses (continued)

Restrictions in MAC Address Assignments:

Structure of a MAC Address:



I/G: Individual or Group address. LSB of octet 0.
I/G=0 - Individual address.
I/G=1 - Group address.

U/L: Universally or Locally administered. Next to LSB of octet 0.
U/L=0 - Universally administered by IEEE.
U/L=1 - Locally administered.

OUI: Organizationally Unique Identifier.

Locally Assigned Addresses:

Locally assigned address must have the U/L bit set to 1.

Valid individual MAC addresses are:
x2-xx-xx-xx-xx-xx
x6-xx-xx-xx-xx-xx
xA-xx-xx-xx-xx-xx
xE-xx-xx-xx-xx-xx

Valid MAC group addresses are:
x3-xx-xx-xx-xx-xx
x7-xx-xx-xx-xx-xx
xB-xx-xx-xx-xx-xx
xF-xx-xx-xx-xx-xx

Where the x's can be assigned any value.