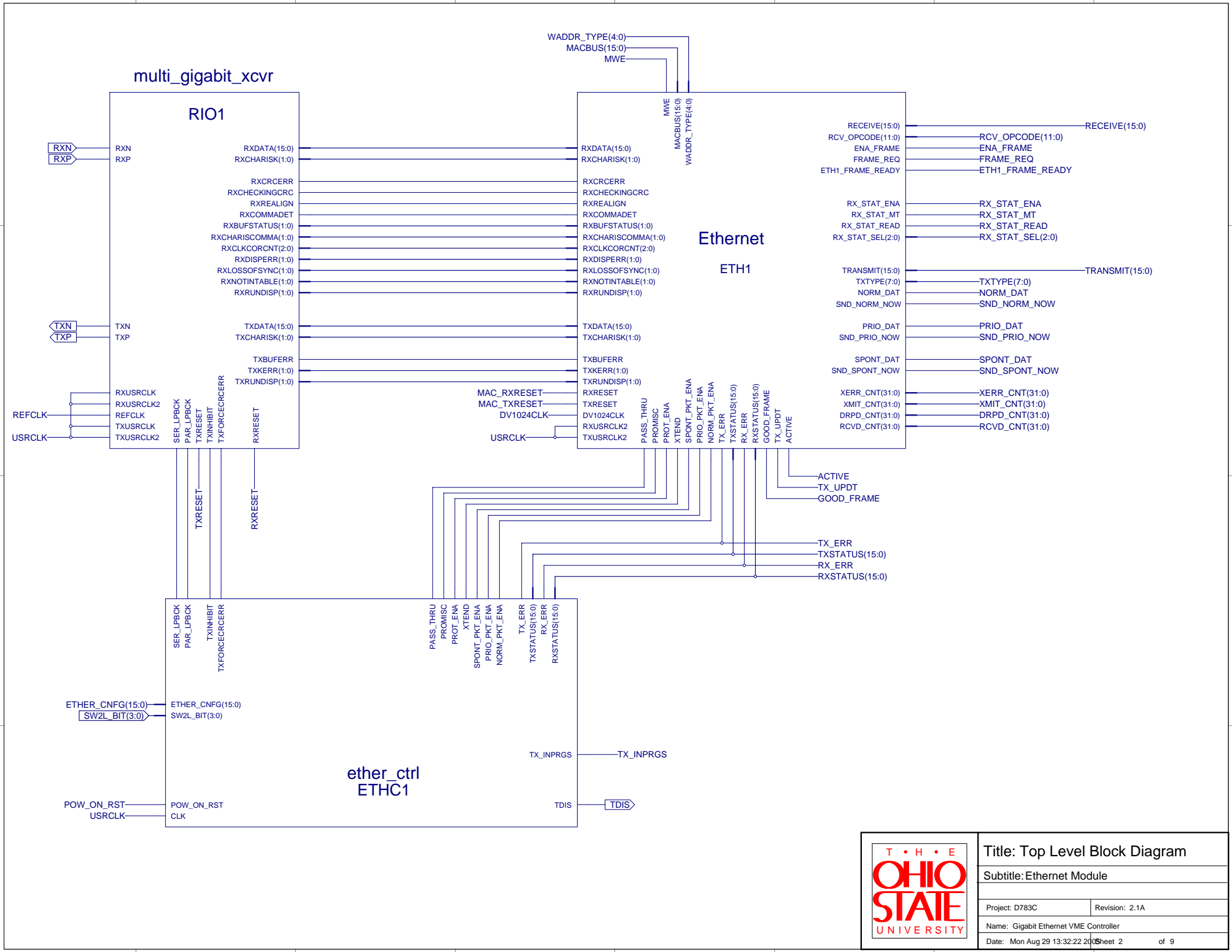
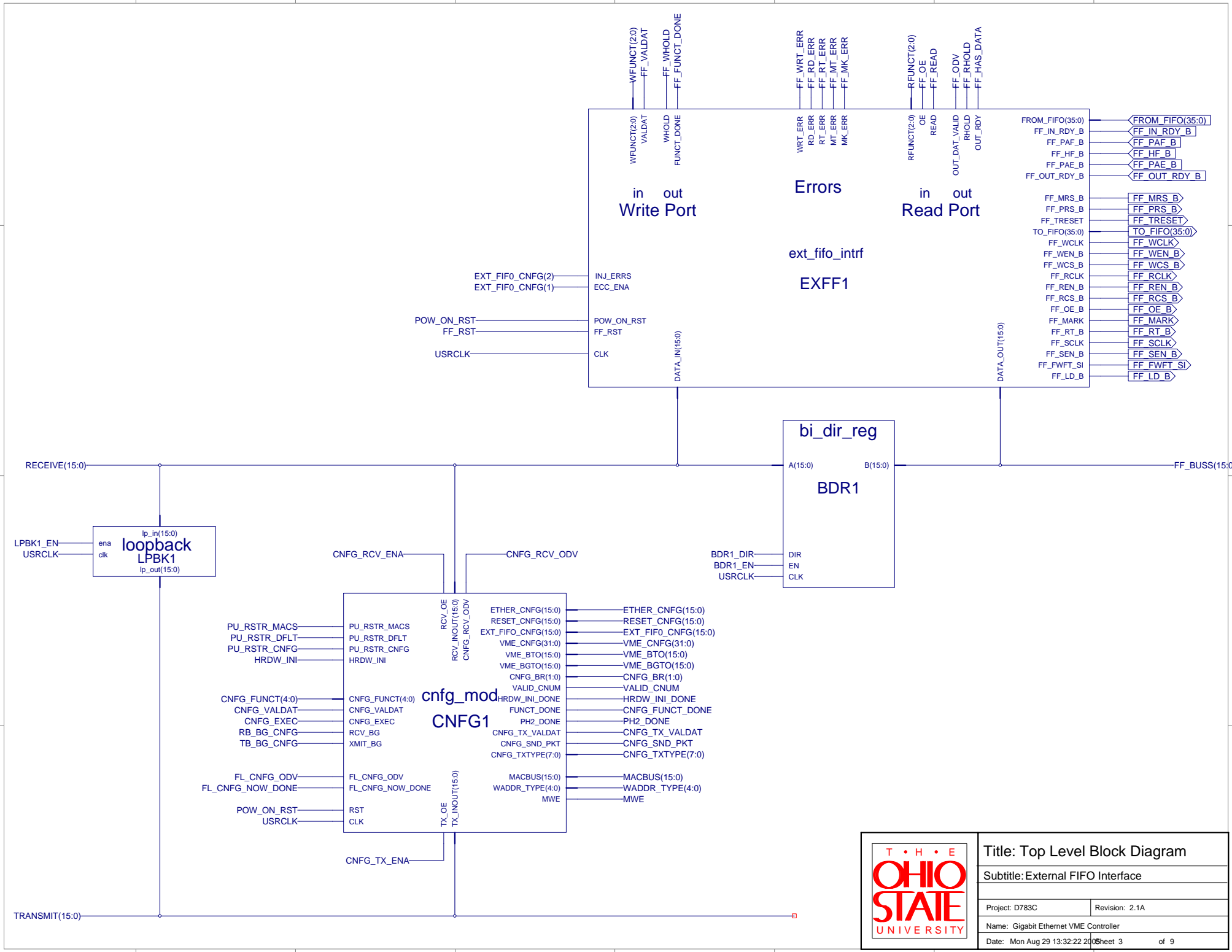

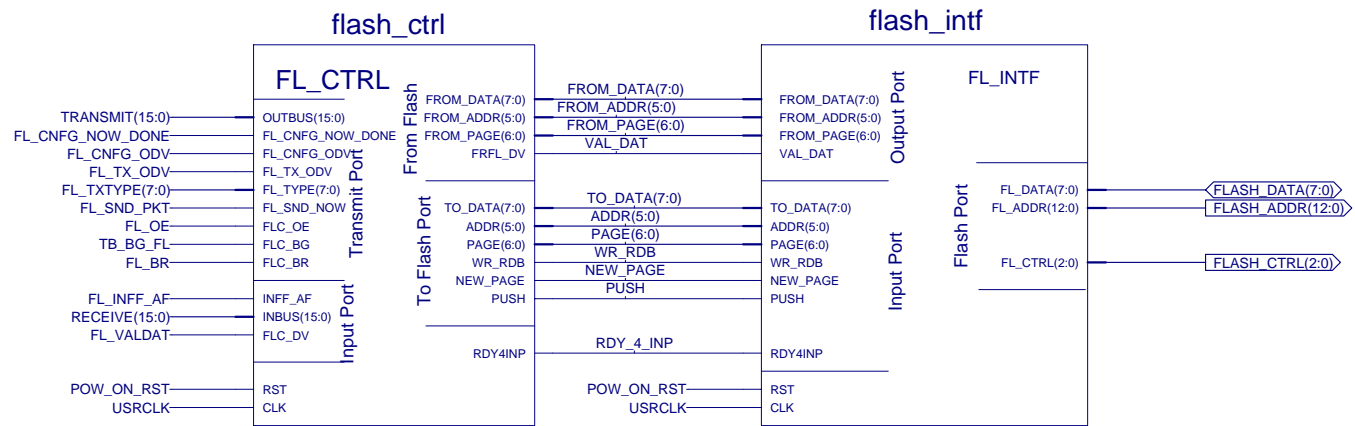
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	Subtitle: Start-up and Shutdown Sequencing	
	Project: D783C	Revision: 2.1A
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005		Sheet 1 of 9



Title: Top Level Block Diagram	
Subtitle: Ethernet Module	
Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005	Sheet 2 of 9



	Title: Top Level Block Diagram	
	Subtitle: External FIFO Interface	
	Project: D783C	Revision: 2.1A
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005		Sheet 3 of 9



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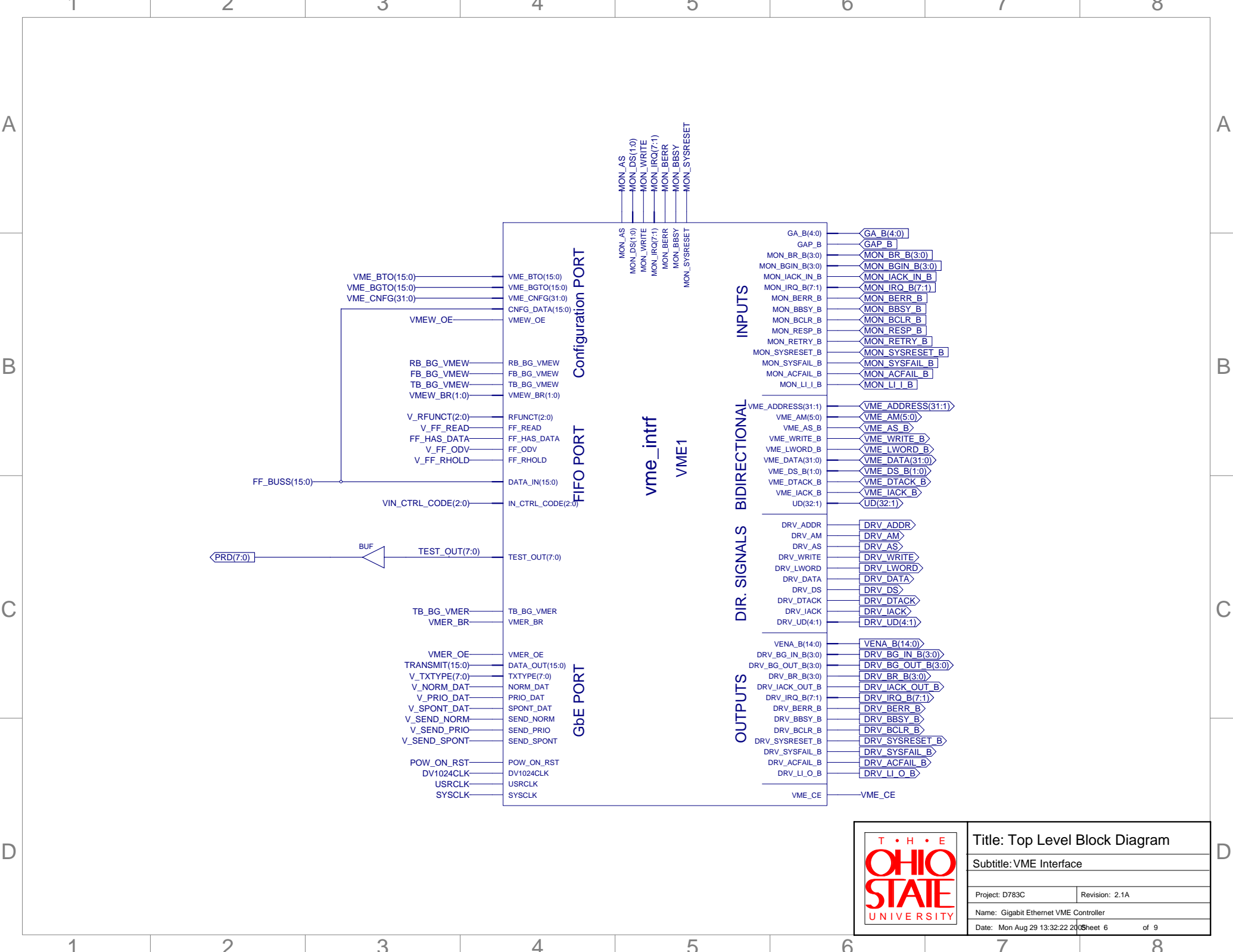
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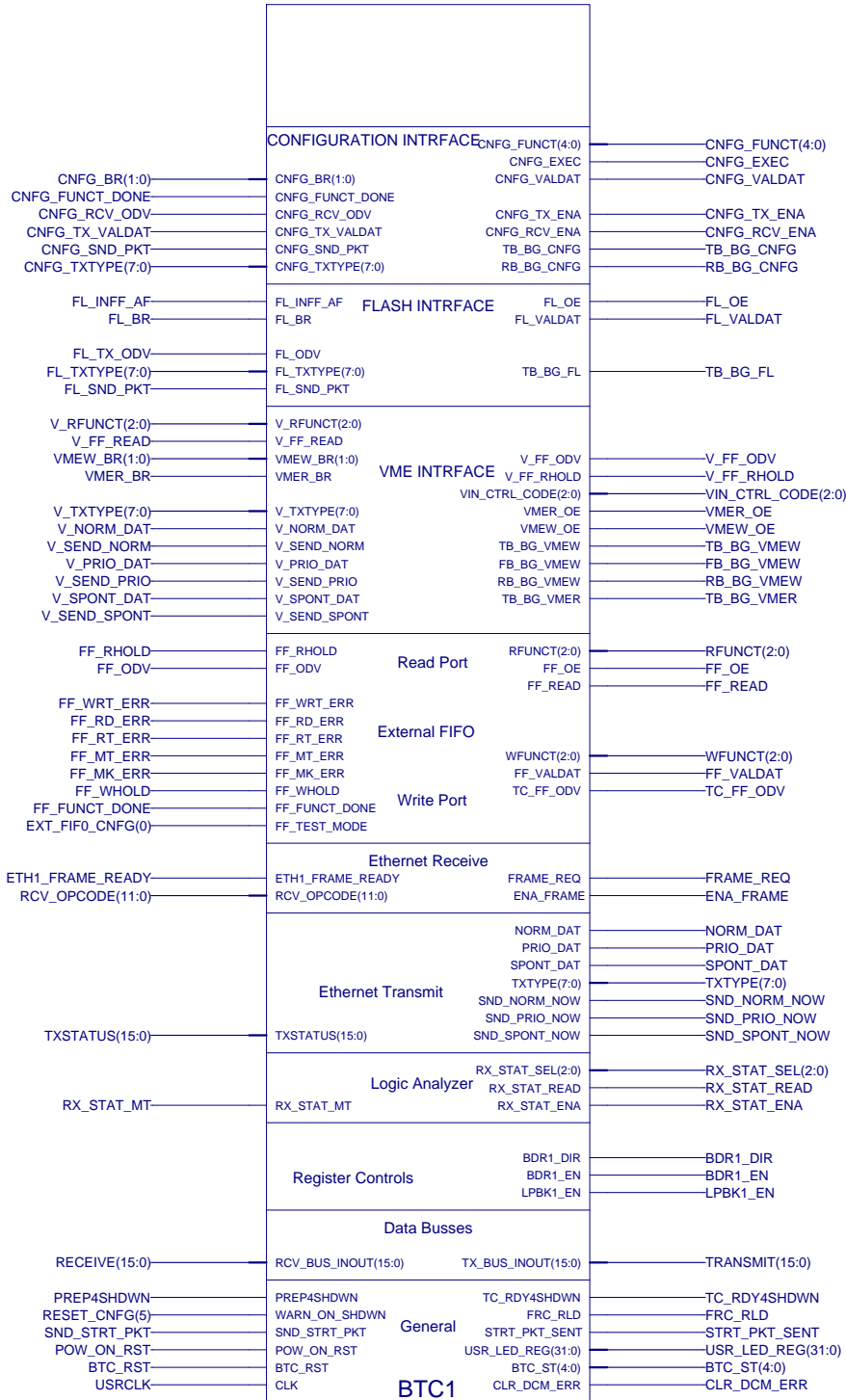
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	Title: Top Level Block Diagram	
	Subtitle: JTAG Interface	
	Project: D783C	Revision: 2.1A
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005		Sheet 5 of 9

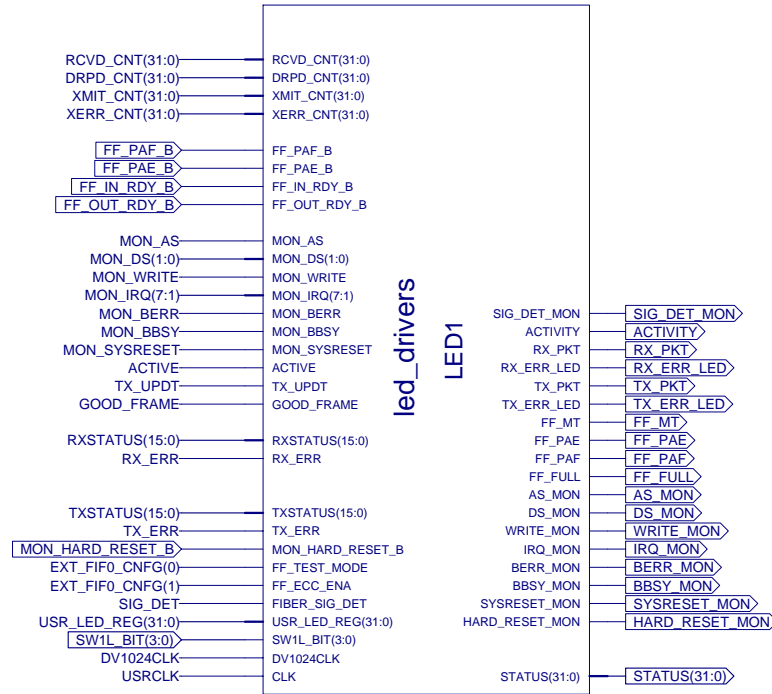


Title: Top Level Block Diagram	
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Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2011	Sheet 6 of 9

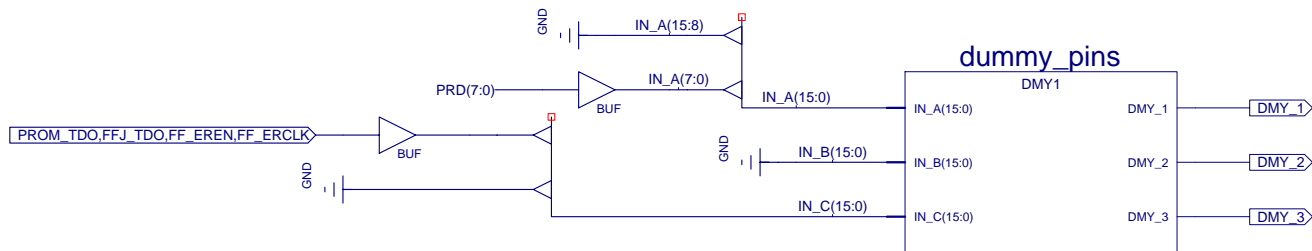
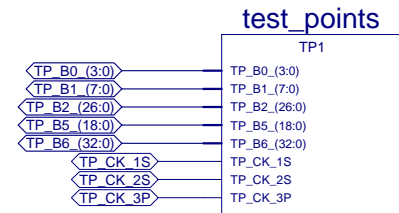
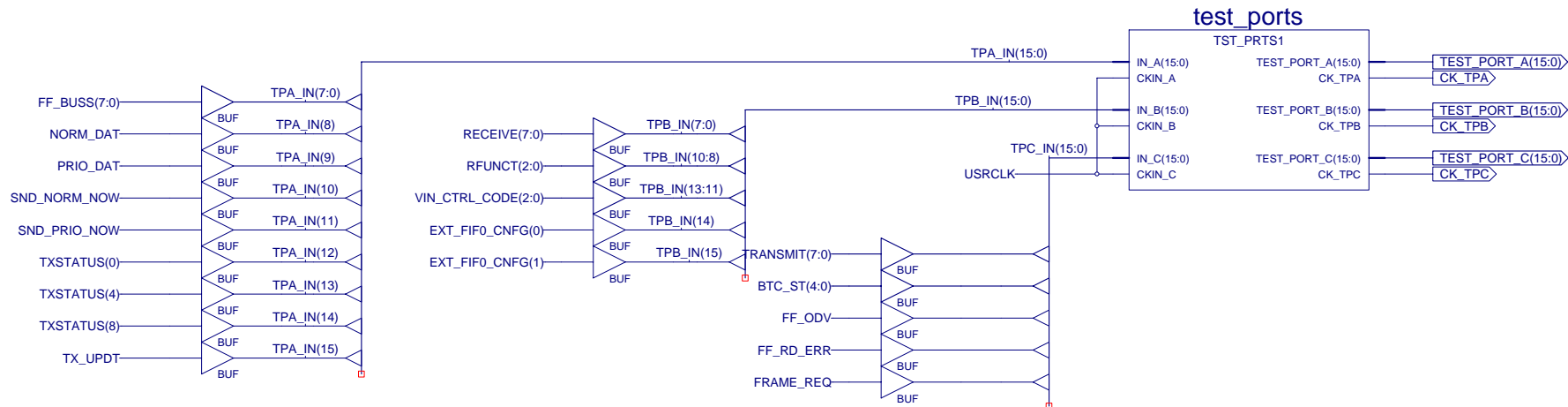
traffic_ctrl



Title: Top Level Block Diagram	
Subtitle: Bus Traffic Controller	
Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005	Sheet 7 of 9



	Title: Top Level Block Diagram	
	Subtitle: Status and Monitoring (LEDs)	
	Project: D783C	Revision: 2.1A
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005		Sheet 8 of 9



GND F2PRM_TCK,F2PRM_TDI,F2PRM_TMS,F2PRM,FFJ_TCK,FFJ_TDI,FFJ_TMS



Title: Top Level Block Diagram

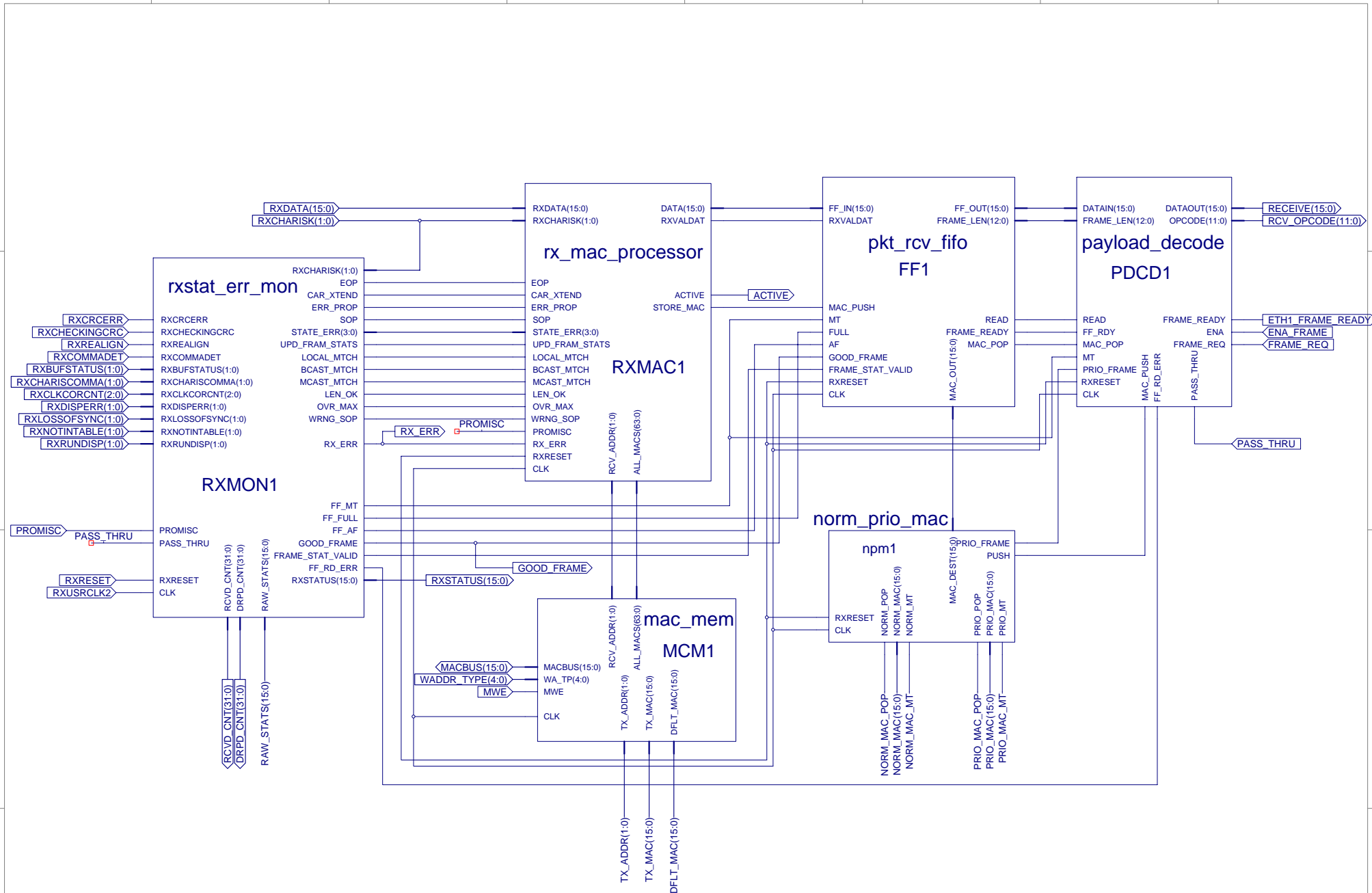
Subtitle: Test Ports and Test Points

Project: D783C

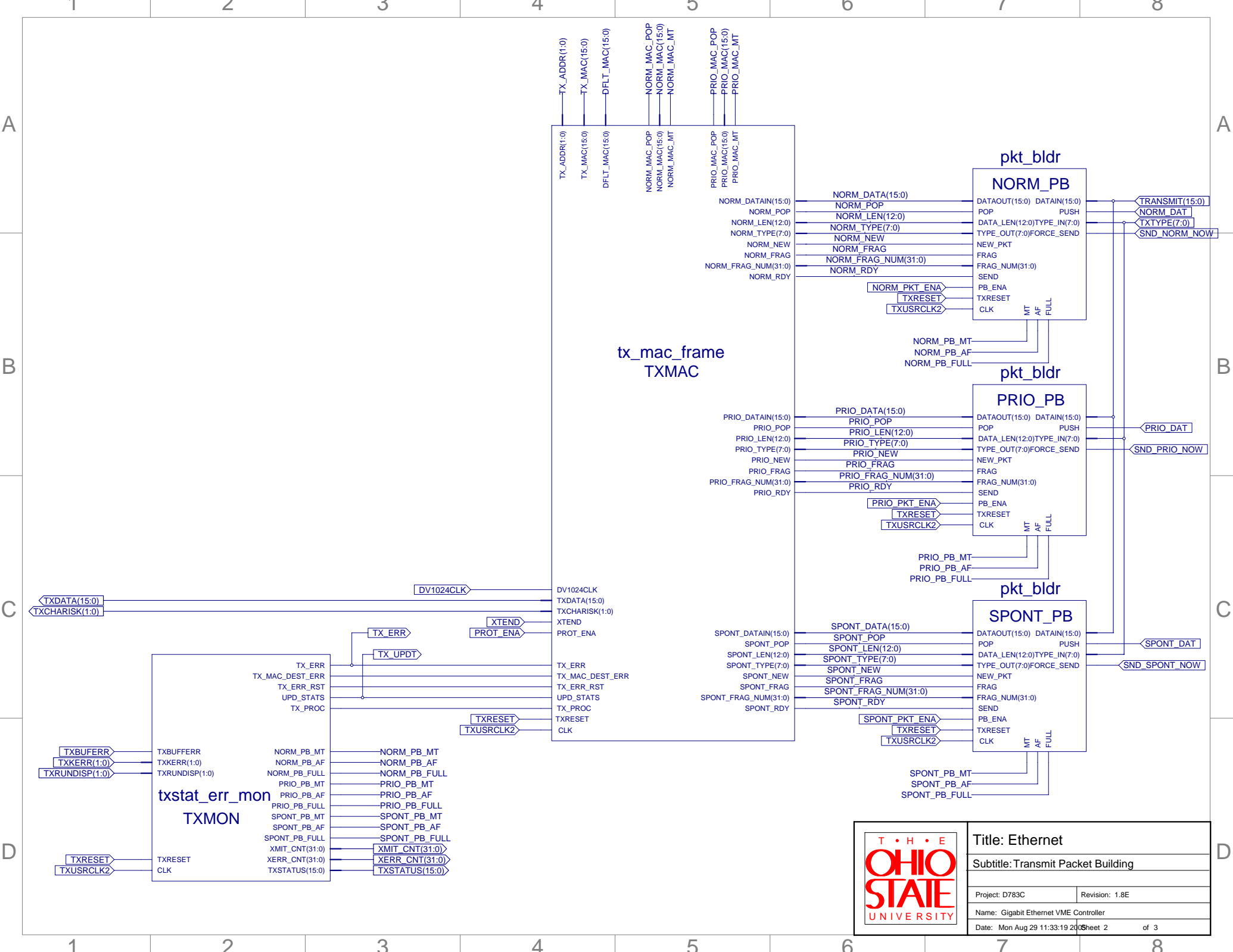
Revision: 2.1A

Name: Gigabit Ethernet VME Controller

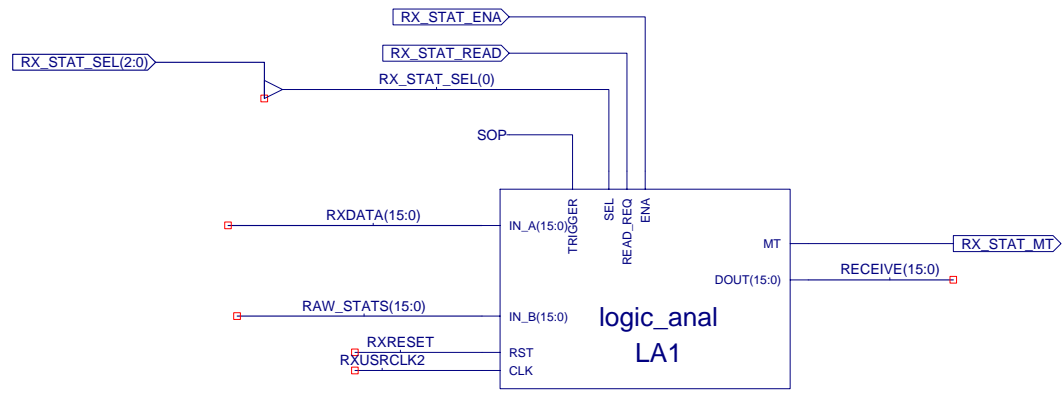
Date: Mon Aug 29 13:32:22 2006 Sheet 9 of 9



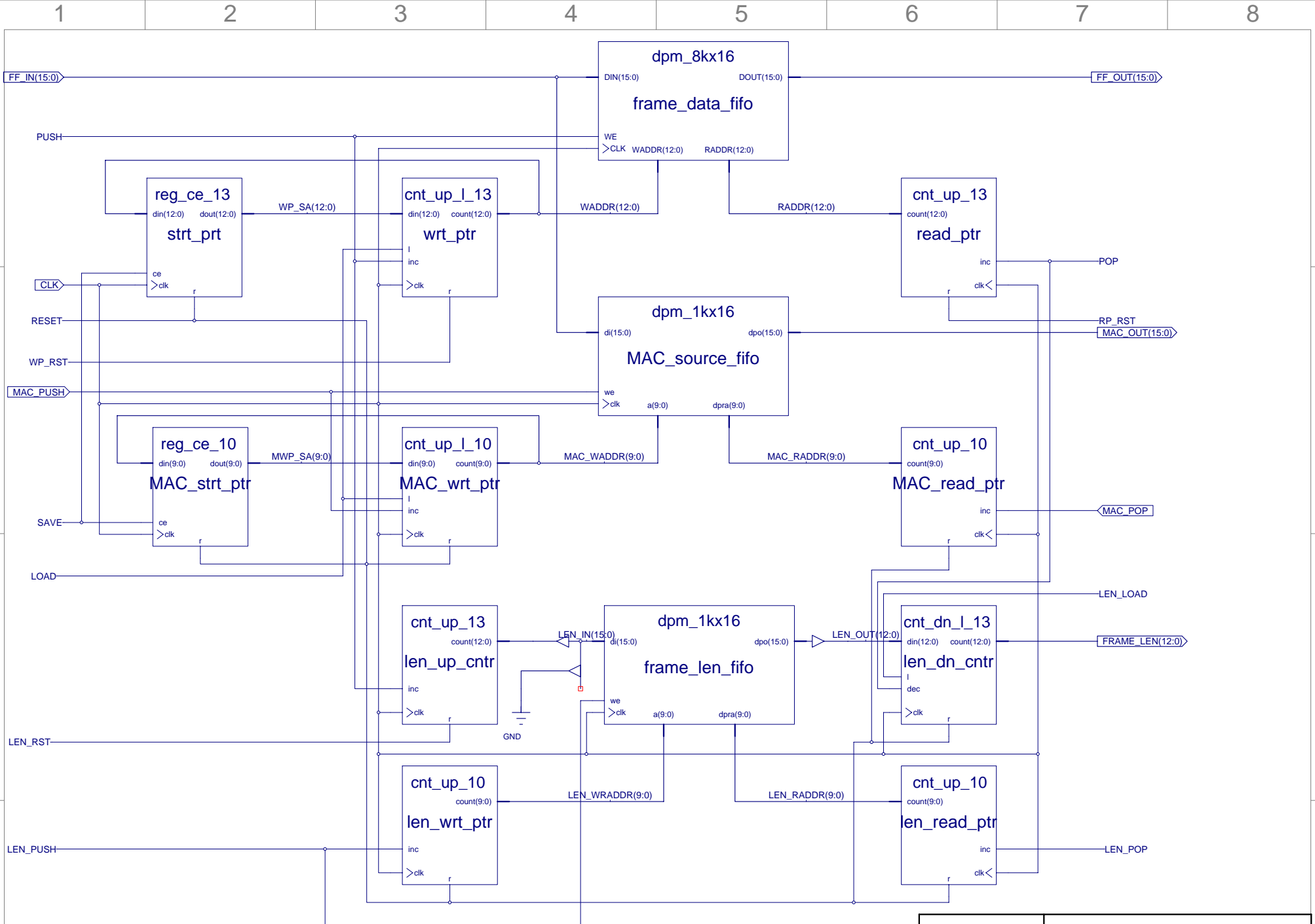
Title: Ethernet	
Subtitle: Receiv Packet Processing	
Project: D783C	Revision: 1.8E
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 11:33:19 2005	Sheet 1 of 3



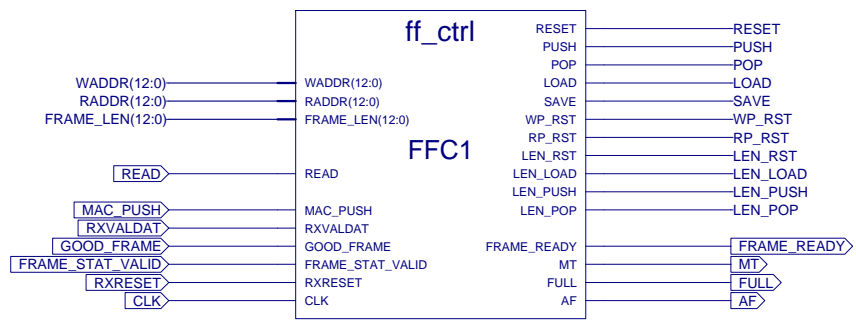
Title: Ethernet	
Subtitle: Transmit Packet Building	
Project: D783C	Revision: 1.8E
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 11:33:19 2005	
Sheet 2	of 3



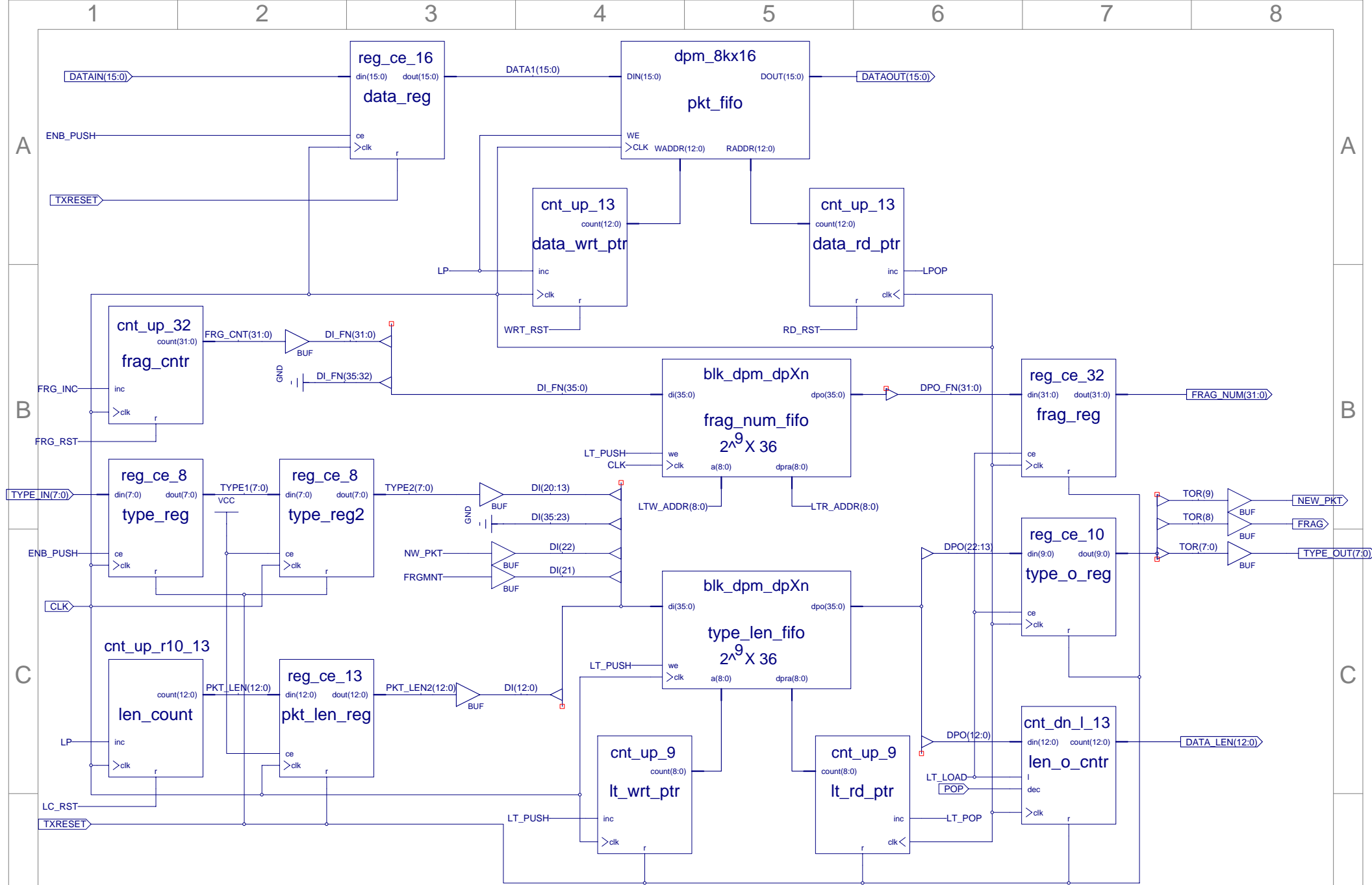
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	Subtitle: Logic Analyzer	
	Project: D783C	Revision: 1.8E
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 11:33:19 2005		Sheet 3 of 3



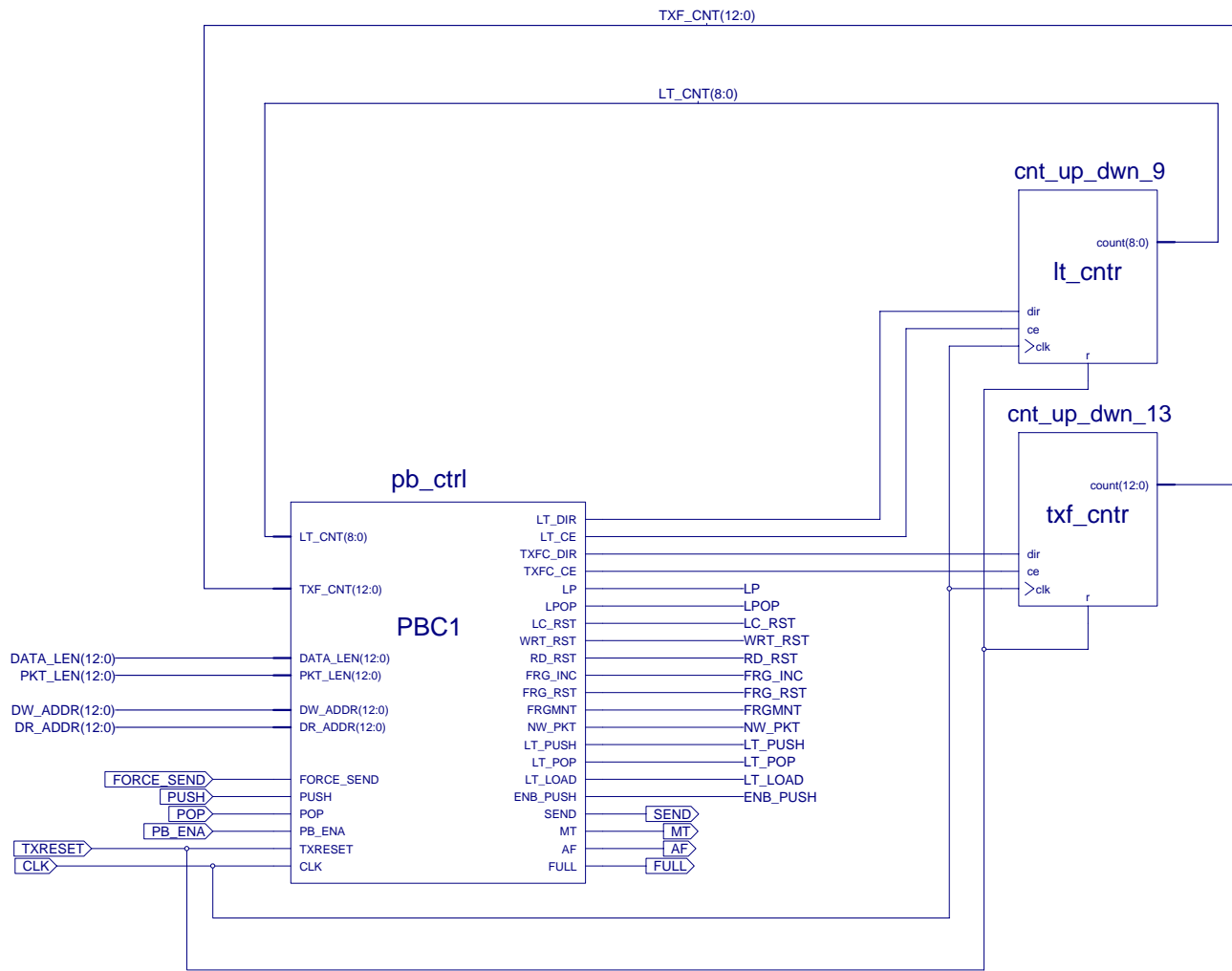
	Title: Packet Receiver FIFO	
	Subtitle: FIFOs and counters	
	Project: D783C	Revision: 1.8E
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 22 11:18:24 2005		Sheet 1 of 2




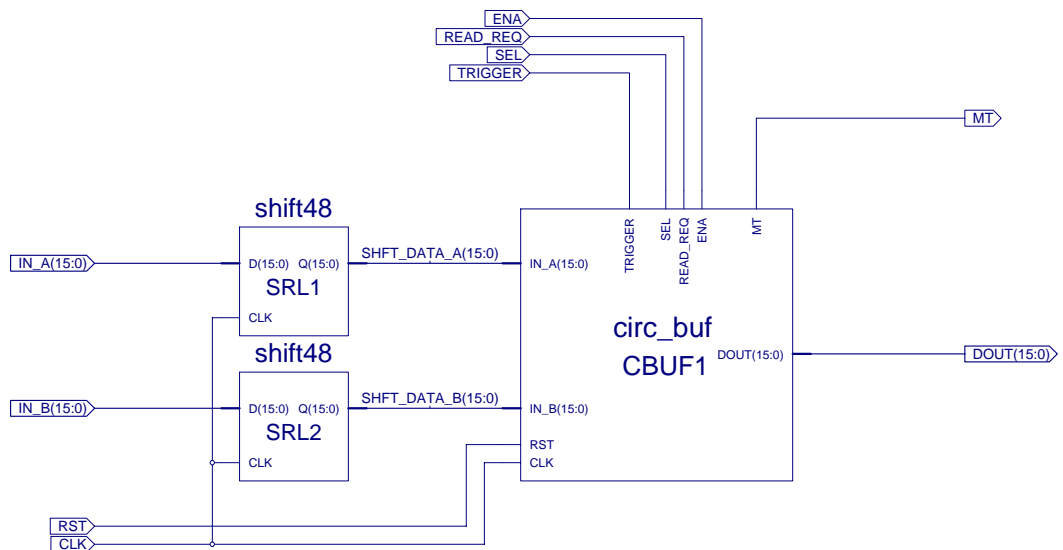
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	Subtitle: FIFO Controller	
	Project: D783C	Revision: 1.8E
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 22 11:18:24 2005		Sheet 2 of 2



Title: Packet Builder	
Subtitle: FIFOs and counters	
Project: D783C	Revision: 2.23
Name: Giagbit Ethernet Controller	
Date: Mon Aug 22 11:11:56 2005 Sheet 1 of 2	



	Title: Packet Builder	
	Subtitle: FIFO controller	
	Project: D783C	Revision: 2.23
	Name: Gigabit Ethernet Controller	
Date: Mon Aug 22 11:11:56 2005 Sheet 2 of 2		



Title: Logic Analyzer

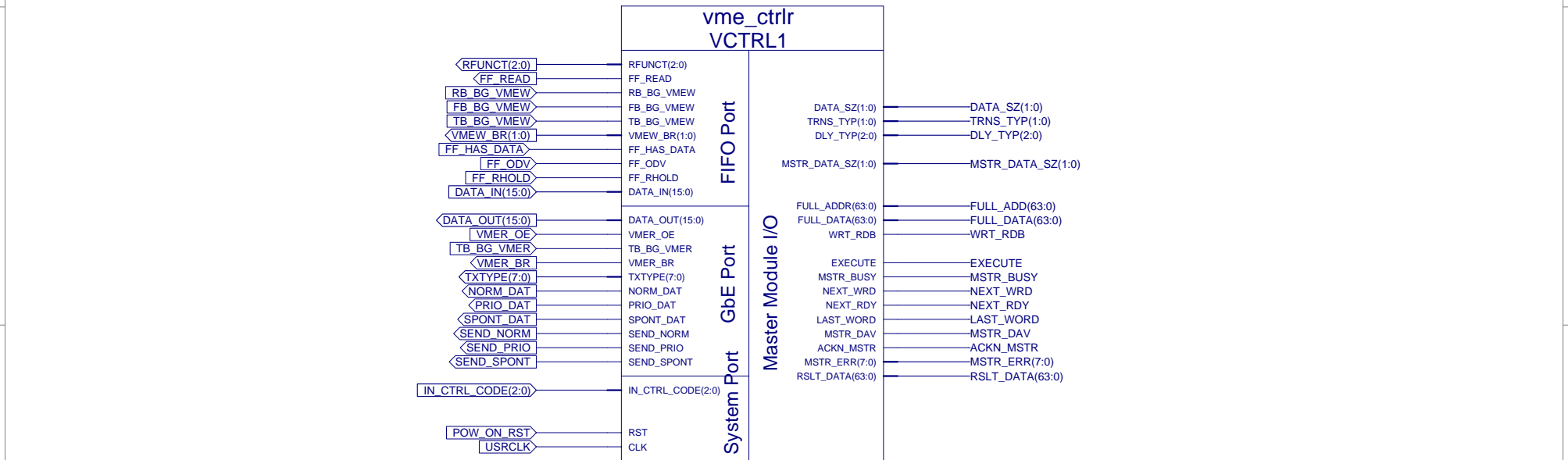
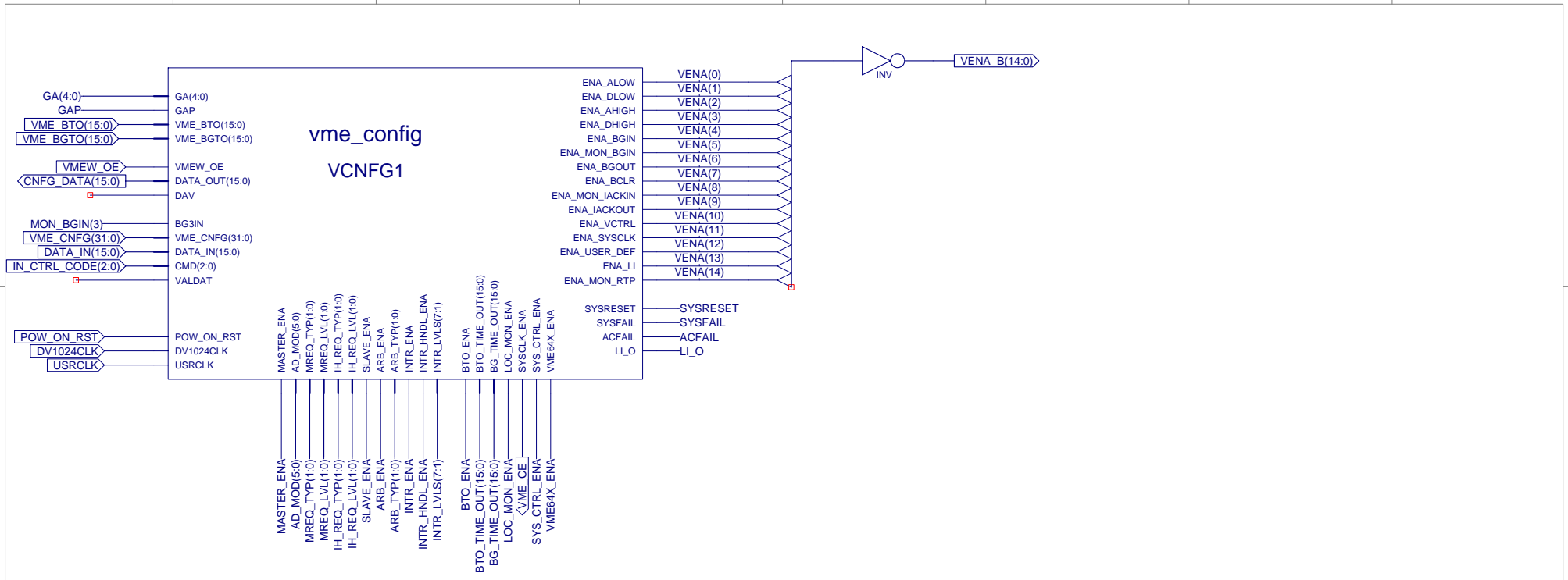
Subtitle: Circular Buffer

Project: D783C

Revision: 1.8E

Name: Gigabit Ethernet VME Controller

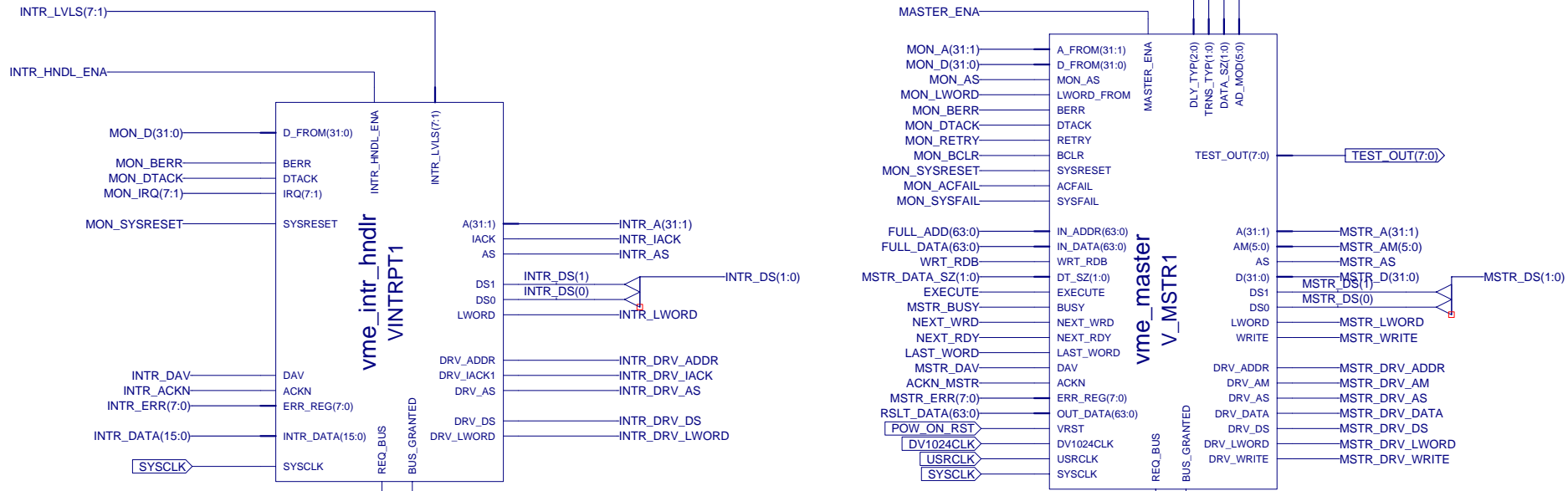
Date: Fri Aug 19 16:07:41 2005 Sheet 1 of 1



	Title: VME Interface	
	Subtitle: Controller	
	Project: D783C	Revision: 1.8E
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:09:59 2005		Sheet 1 of 4

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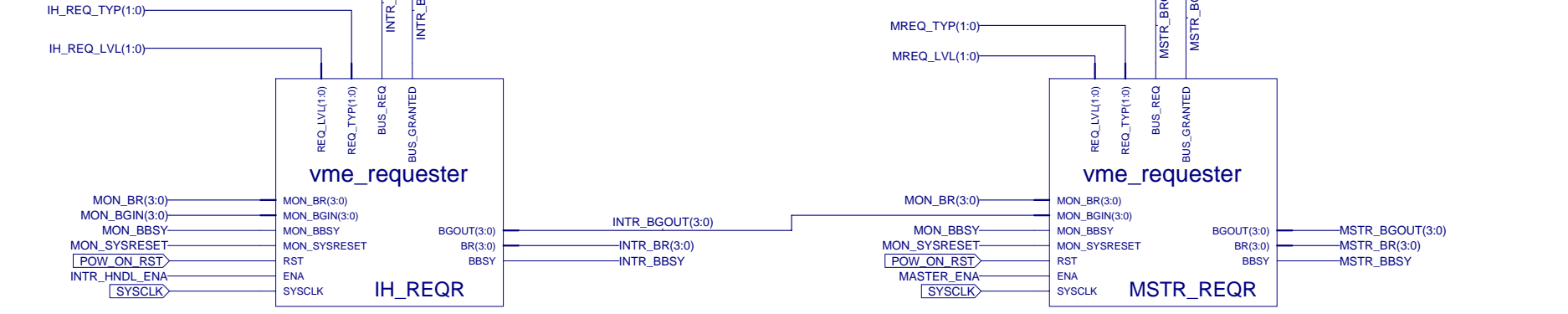


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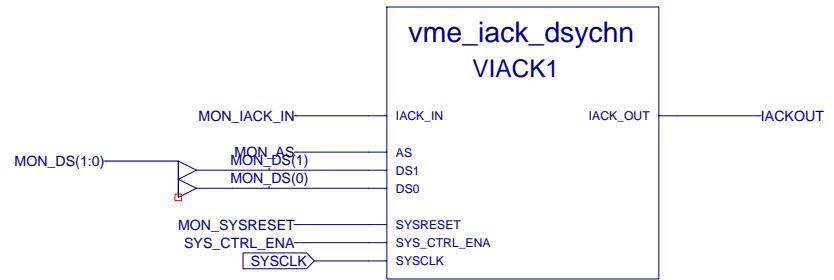
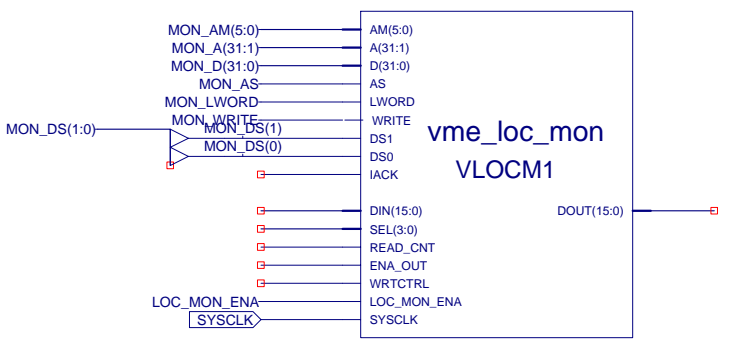
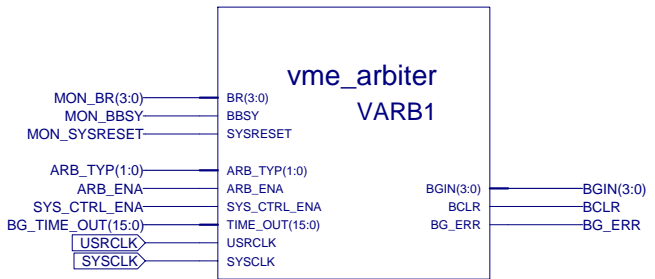
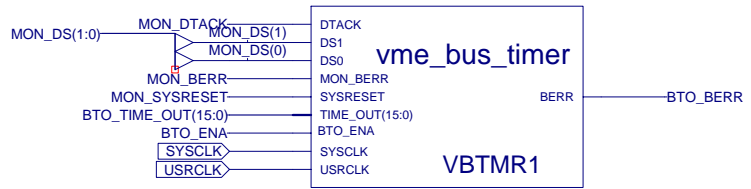
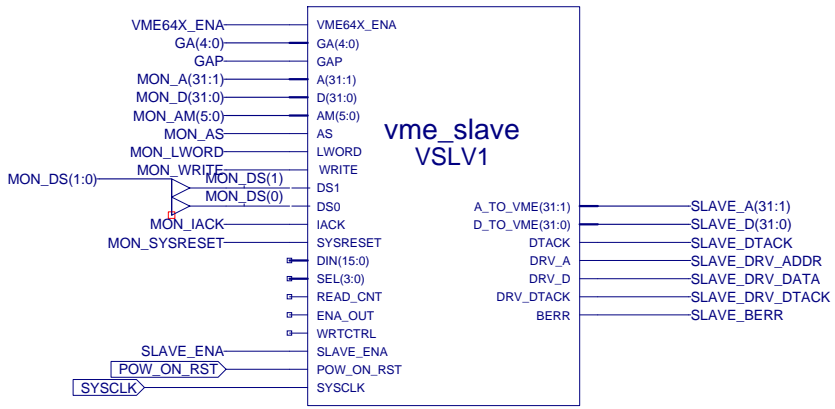
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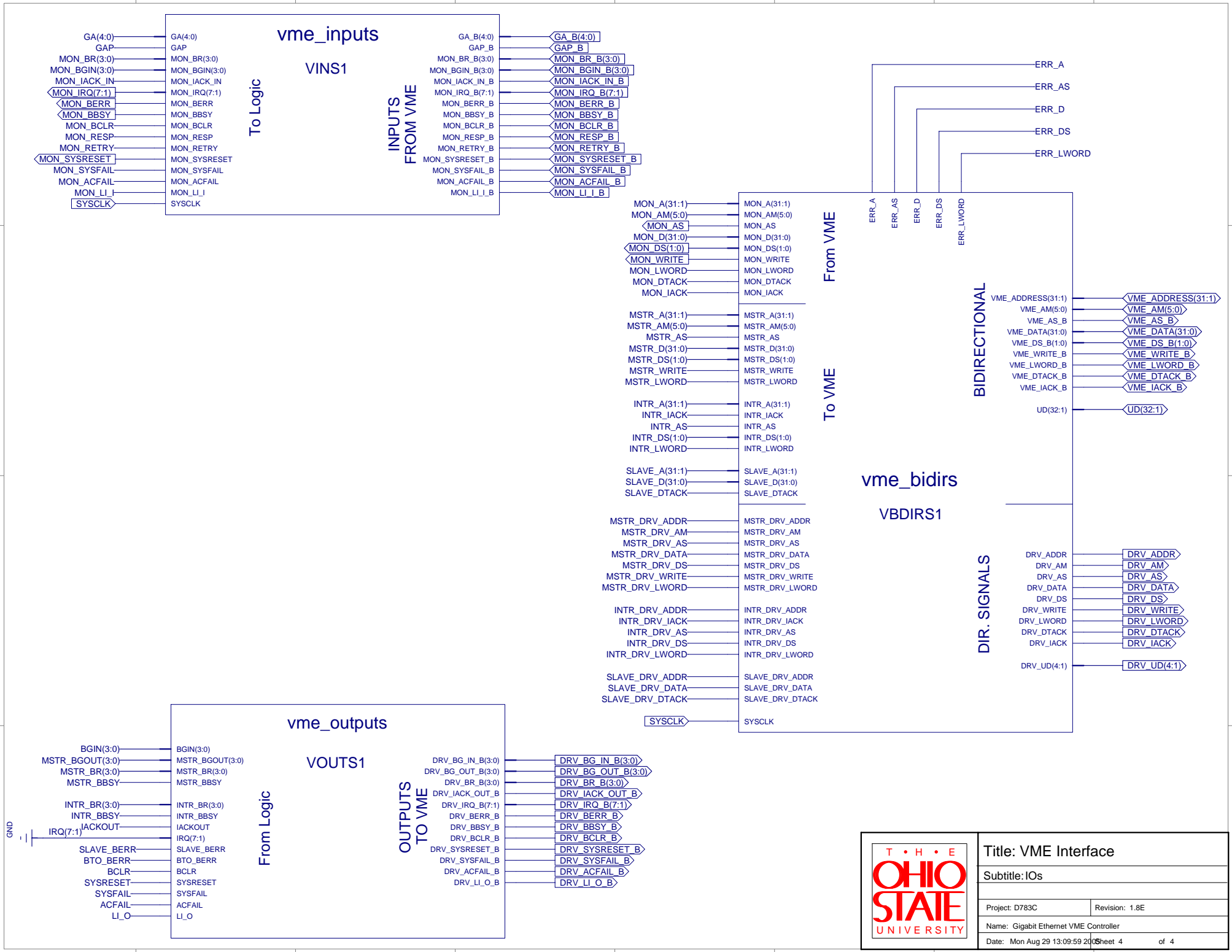
D

D

	Title: VME Interface	
	Subtitle: Master and Interrupt Handler	
	Project: D783C	Revision: 1.8E
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:09:59 2005		Sheet 2 of 4



	Title: VME Interface	
	Subtitle: Slave, Arbiter, Bus Timer, and Misc.	
	Project: D783C	Revision: 1.8E
	Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:09:59 2011		Sheet 3 of 4



Title: VME Interface	
Subtitle: IOs	
Project: D783C	Revision: 1.8E
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:09:59 2005	Sheet 4 of 4