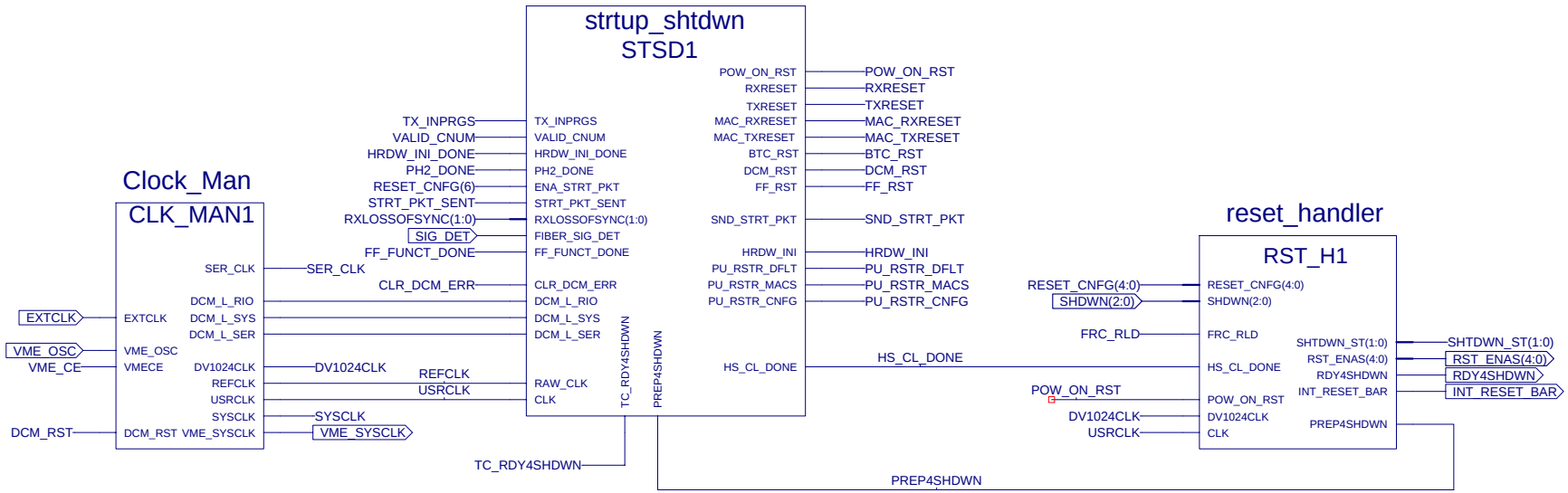

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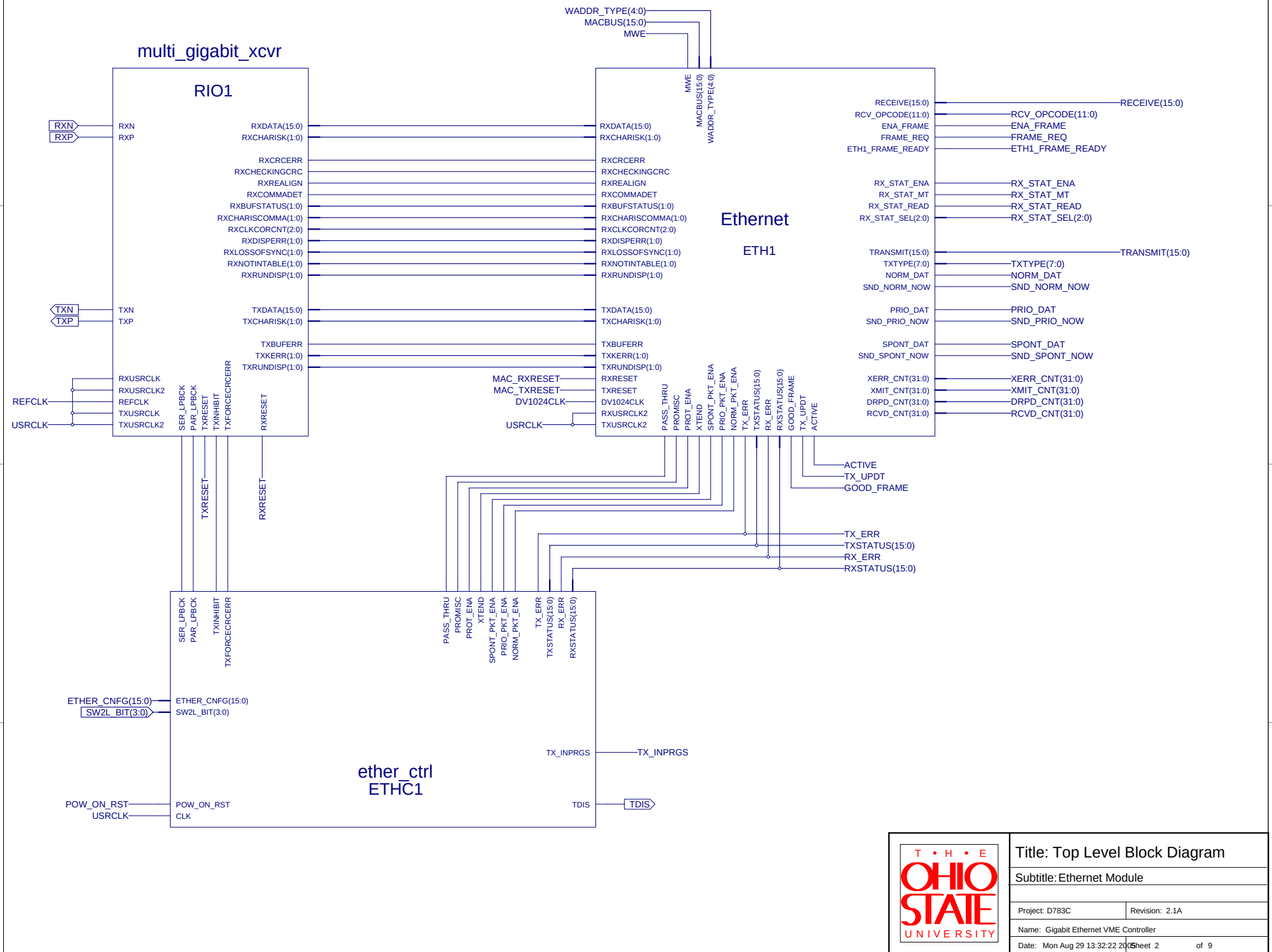
Title: Top Level Block Diagram

Subtitle: Start-up and Shutdown Sequencing

Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005	Sheet 1 of 9



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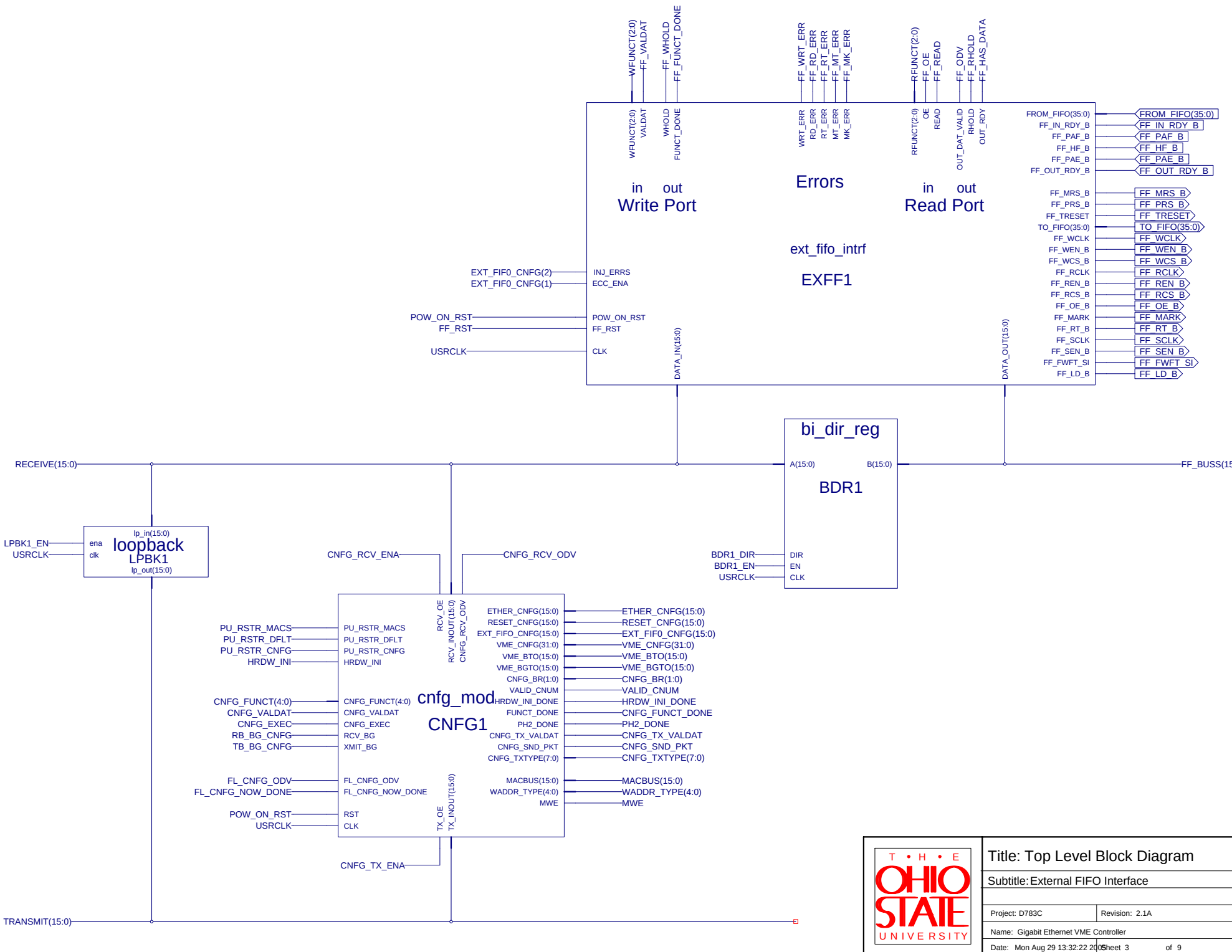
Title: Top Level Block Diagram

Subtitle: Ethernet Module

Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005	Sheet 2 of 9


WFUNCT(2:0)
FF_VALDAT
FF_WHOLD
FF_FUNCT_DONE
FF_WRT_ERR
FF_RD_ERR
FF_RT_ERR
FF_MT_ERR
FF_MK_ERR
RFUNCT(2:0)
FF_OE
FF_READ
FF_ODV
FF_RHOLD
FF_HAS_DATA
in out
Write Port
Errors
in out
Read Port
ext_fifo_intrf
EXFF1
EXT_FIF0_CNFG(2)
EXT_FIF0_CNFG(1)
INJ_ERRS
ECC_ENA
POW_ON_RST
FF_RST
USRCLK
CLK
DATA_IN(15:0)
DATA_OUT(15:0)
FROM_FIFO(35:0)
FF_IN_RDY_B
FF_PAF_B
FF_HF_B
FF_PAE_B
FF_OUT_RDY_B
FF_MRS_B
FF_PRS_B
FF_TRESET
TO_FIFO(35:0)
FF_WCLK
FF_WEN_B
FF_WCS_B
FF_RCLK
FF_REN_B
FF_RCS_B
FF_OE_B
FF_MARK
FF_RT_B
FF_SCLK
FF_SEN_B
FF_FWFT_SI
FF_LD_B
bi_dir_reg
A(15:0)
B(15:0)
BDR1
RECEIVE(15:0)
FF_BUSS(15:0)
BDR1_DIR
BDR1_EN
DIR
EN
lp_in(15:0)
LPBK1_EN
ena
loopback
LPBK1
clk
lp_out(15:0)
CNFG_RCV_ENA
CNFG_RCV_ODV
RCV_OE
RCV_INOUT(15:0)
CNFG_RCV_ODV
PU_RSTR_MACS
PU_RSTR_DFLT
PU_RSTR_CNFG
HRDW_INI
CNFG_FUNCT(4:0)
CNFG_VALDAT
CNFG_EXEC
RB_BG_CNFG
TB_BG_CNFG
cnfg_mod
CNFG1
RCV_BG
XMIT_BG
FL_CNFG_ODV
FL_CNFG_NOW_DONE
RST
TX_OE
TX_INOUT(15:0)
ETHER_CNFG(15:0)
RESET_CNFG(15:0)
EXT_FIFO_CNFG(15:0)
VME_CNFG(31:0)
VME_BTO(15:0)
VME_BGTO(15:0)
CNFG_BR(1:0)
VALID_CNUM
HRDW_INI_DONE
FUNCT_DONE
PH2_DONE
CNFG_TX_VALDAT
CNFG_SND_PKT
CNFG_TXTYPE(7:0)
MACBUS(15:0)
WADDR_TYPE(4:0)
MWE
CNFG_TX_ENA
TRANSMIT(15:0)
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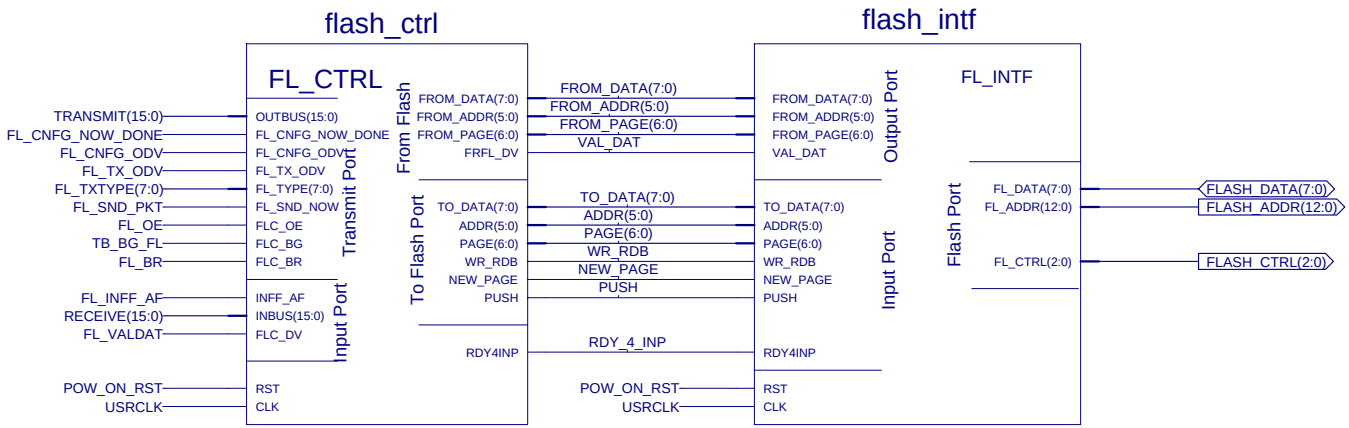
Title: Top Level Block Diagram
Subtitle: External FIFO Interface
Project: D783C
Revision: 2.1A
Name: Gigabit Ethernet VME Controller
Date: Mon Aug 29 13:32:22 2005
Sheet 3 of 9



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Title: Top Level Block Diagram

Subtitle: Flash Memory Interface

Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005	Sheet 4 of 9

1 2 3 4 5 6 7 8

A B C D

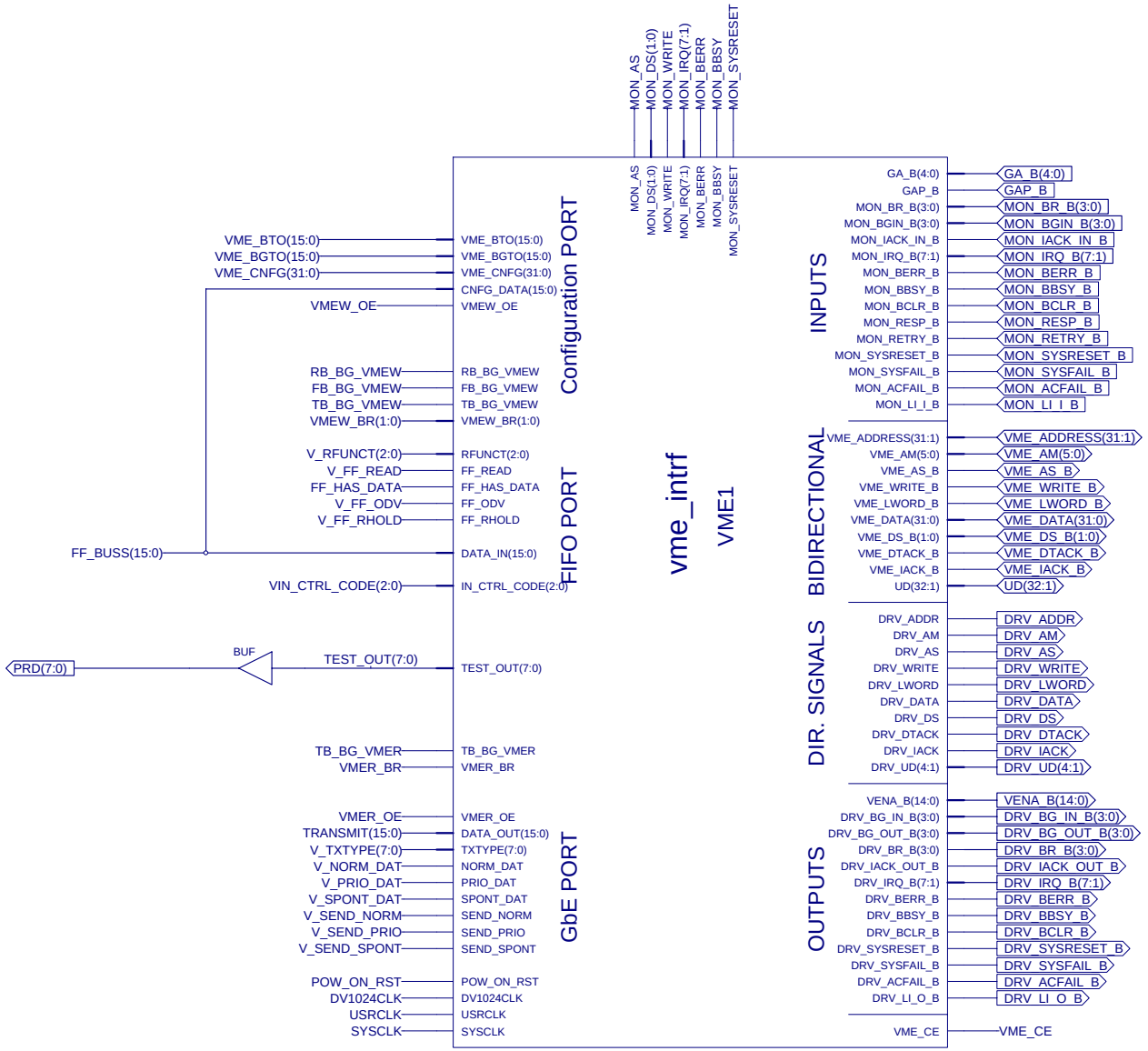
Title: Top Level Block Diagram

Subtitle: JTAG Interface

Project: D783C
Revision: 2.1A

Name: Gigabit Ethernet VME Controller

Date: Mon Aug 29 13:32:22 2005
Sheet 5 of 9



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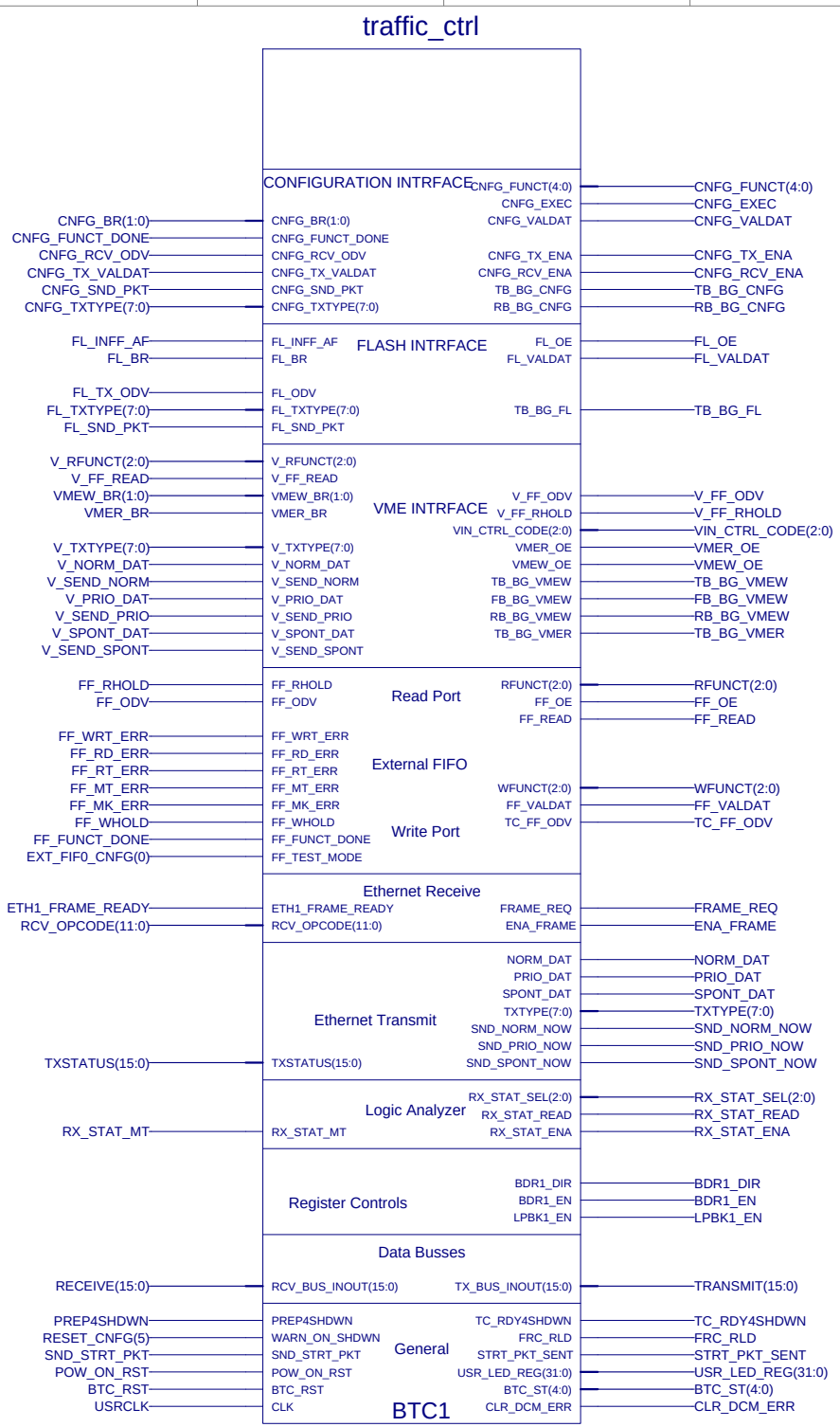
Title: Top Level Block Diagram

Subtitle: VME Interface

Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005	Sheet 6 of 9



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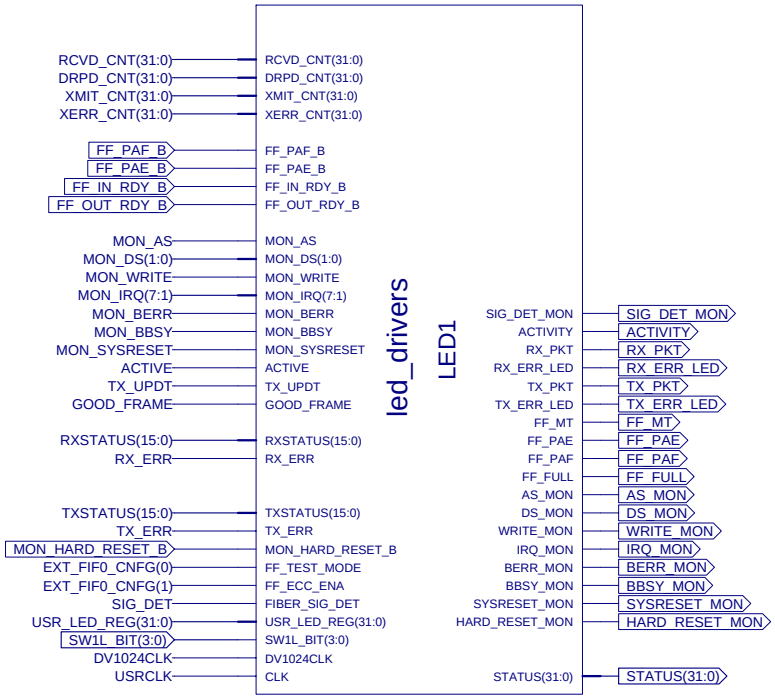
Title: Top Level Block Diagram

Subtitle: Bus Traffic Controller

Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005	Sheet 7 of 9



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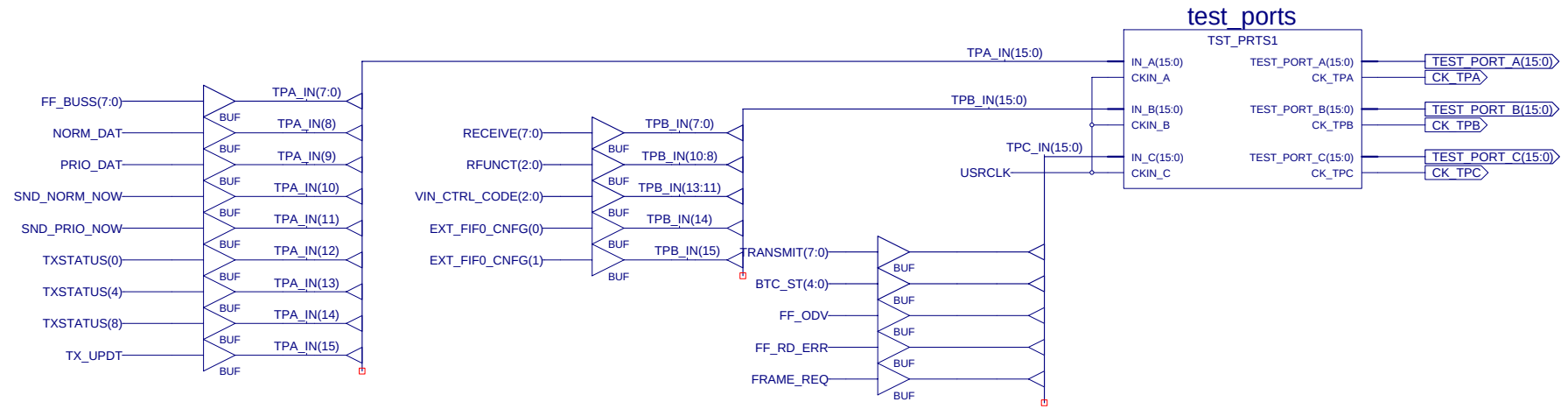
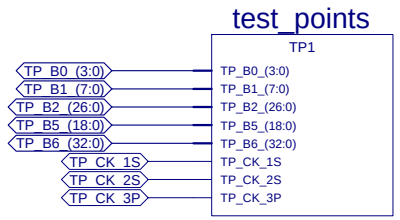
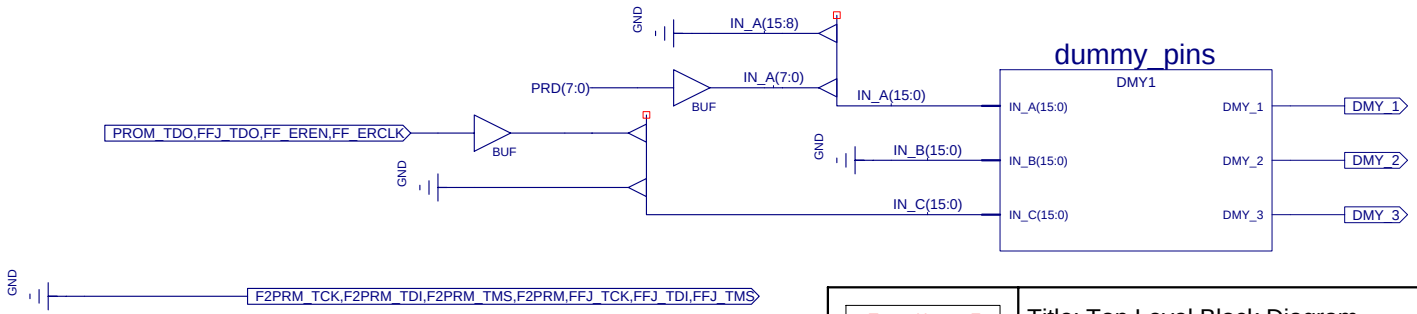
Title: Top Level Block Diagram

Subtitle: Status and Monitoring (LEDs)

Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005	Sheet 8 of 9







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Title: Top Level Block Diagram

Subtitle: Test Ports and Test Points

Project: D783C	Revision: 2.1A
Name: Gigabit Ethernet VME Controller	
Date: Mon Aug 29 13:32:22 2005	Sheet 9 of 9