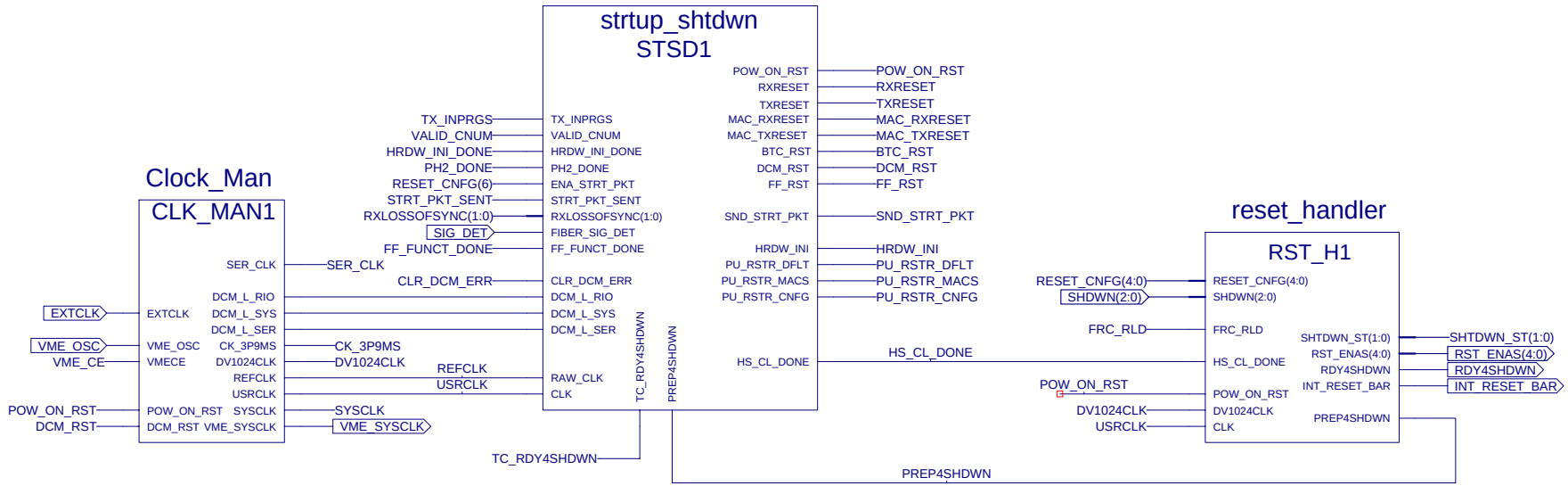

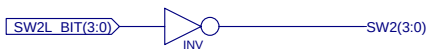

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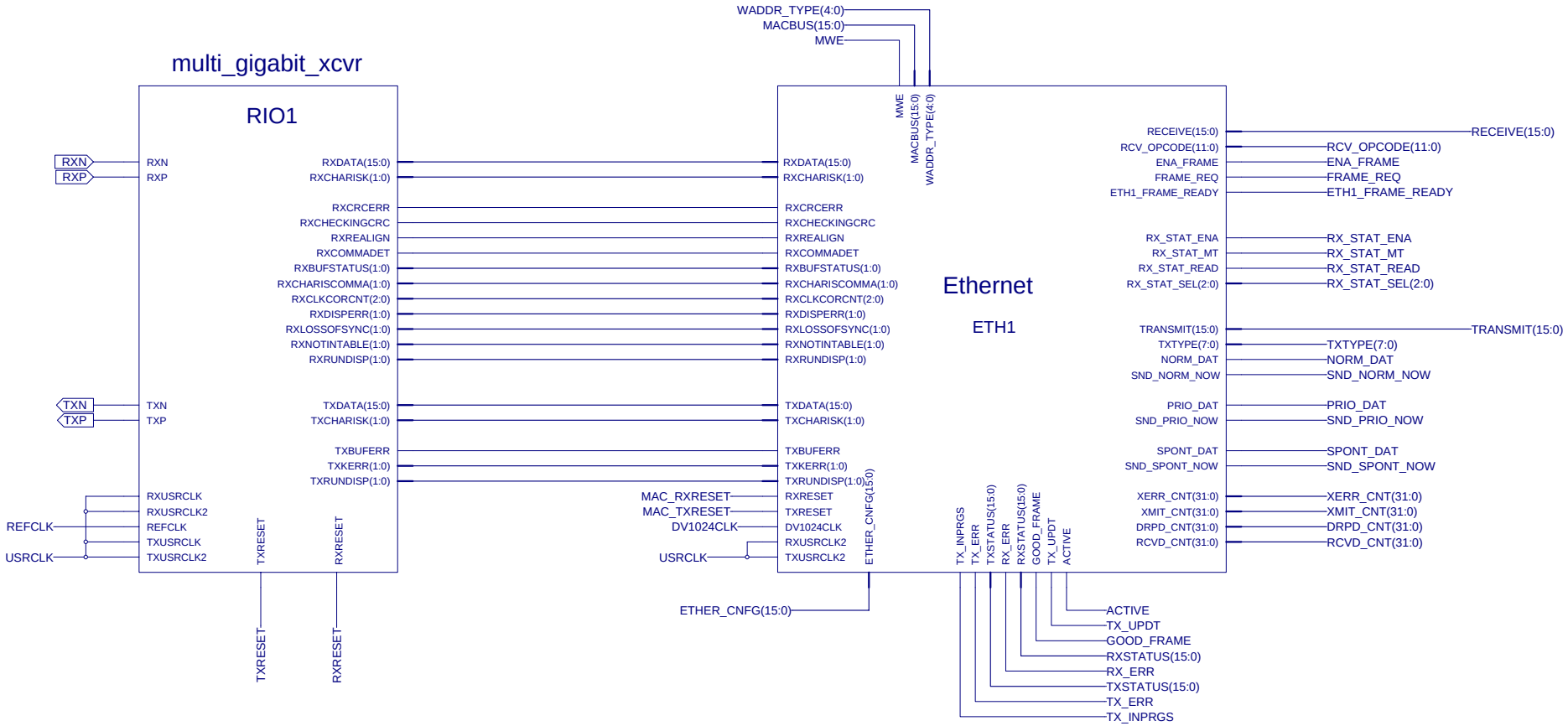
Title: VME Master and System Controller

Subtitle: Start-up and Shutdown Sequencing

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:53:56 2006	Sheet 1 of 9



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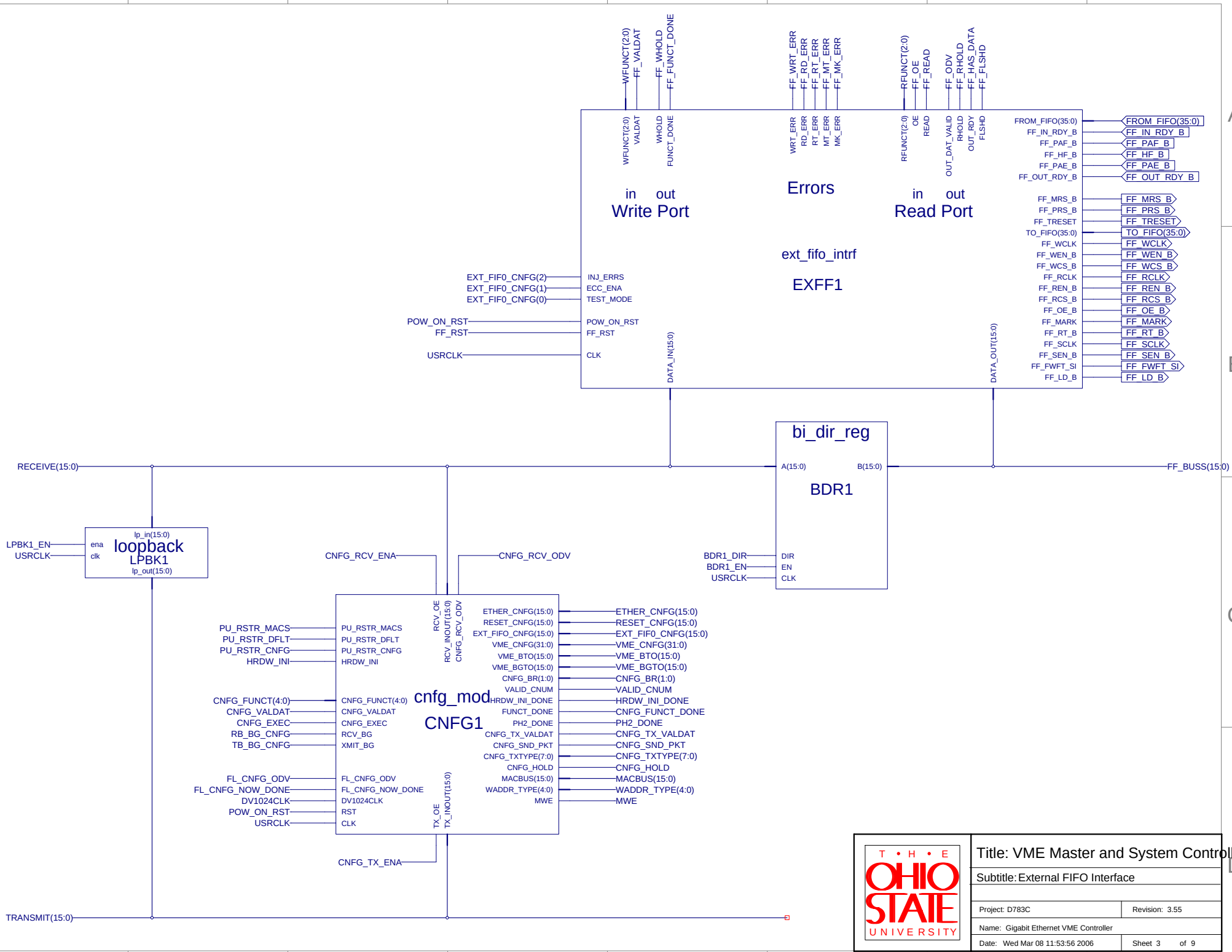
Title: VME Master and System Controller

Subtitle: Ethernet Module

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:53:56 2006	Sheet 2 of 9


WFUNCT(2:0)
FF_VALDAT
FF_WHOLD
FF_FUNCT_DONE
FF_WRT_ERR
FF_RD_ERR
FF_RT_ERR
FF_MT_ERR
FF_MK_ERR
RFUNCT(2:0)
FF_OE
FF_READ
FF_ODV
FF_RHOLD
FF_HAS_DATA
FF_FLSHD
in out
Write Port
Errors
in out
Read Port
ext_fifo_intrf
EXFF1
EXT_FIF0_CNFG(2)
EXT_FIF0_CNFG(1)
EXT_FIF0_CNFG(0)
INJ_ERRS
ECC_ENA
TEST_MODE
POW_ON_RST
FF_RST
USRCLK
CLK
DATA_IN(15:0)
DATA_OUT(15:0)
FROM_FIFO(35:0)
FF_IN_RDY_B
FF_PAF_B
FF_HF_B
FF_PAE_B
FF_OUT_RDY_B
FF_MRS_B
FF_PRS_B
FF_TRESET
TO_FIFO(35:0)
FF_WCLK
FF_WEN_B
FF_WCS_B
FF_RCLK
FF_REN_B
FF_RCS_B
FF_OE_B
FF_MARK
FF_RT_B
FF_SCLK
FF_SEN_B
FF_FWFT_SI
FF_LD_B
RECEIVE(15:0)
bi_dir_reg
A(15:0)
B(15:0)
BDR1
FF_BUSS(15:0)
BDR1_DIR
BDR1_EN
DIR
EN
lp_in(15:0)
LPBK1_EN
ena
loopback
LPBK1
clk
lp_out(15:0)
CNFG_RCV_ENA
CNFG_RCV_ODV
PU_RSTR_MACS
PU_RSTR_DFLT
PU_RSTR_CNFG
HRDW_INI
RCV_OE
RCV_INOUT(15:0)
CNFG_RCV_ODV
ETHER_CNFG(15:0)
RESET_CNFG(15:0)
EXT_FIFO_CNFG(15:0)
VME_CNFG(31:0)
VME_BTO(15:0)
VME_BGTO(15:0)
CNFG_BR(1:0)
VALID_CNUM
HRDW_INI_DONE
FUNCT_DONE
PH2_DONE
CNFG_TX_VALDAT
CNFG_SND_PKT
CNFG_TXTYPE(7:0)
CNFG_HOLD
MACBUS(15:0)
WADDR_TYPE(4:0)
MWE
CNFG_FUNCT(4:0)
CNFG_VALDAT
CNFG_EXEC
RB_BG_CNFG
TB_BG_CNFG
cnfg_mod
CNFG1
RCV_BG
XMIT_BG
FL_CNFG_ODV
FL_CNFG_NOW_DONE
DV1024CLK
RST
TX_OE
TX_INOUT(15:0)
CNFG_TX_ENA
TRANSMIT(15:0)
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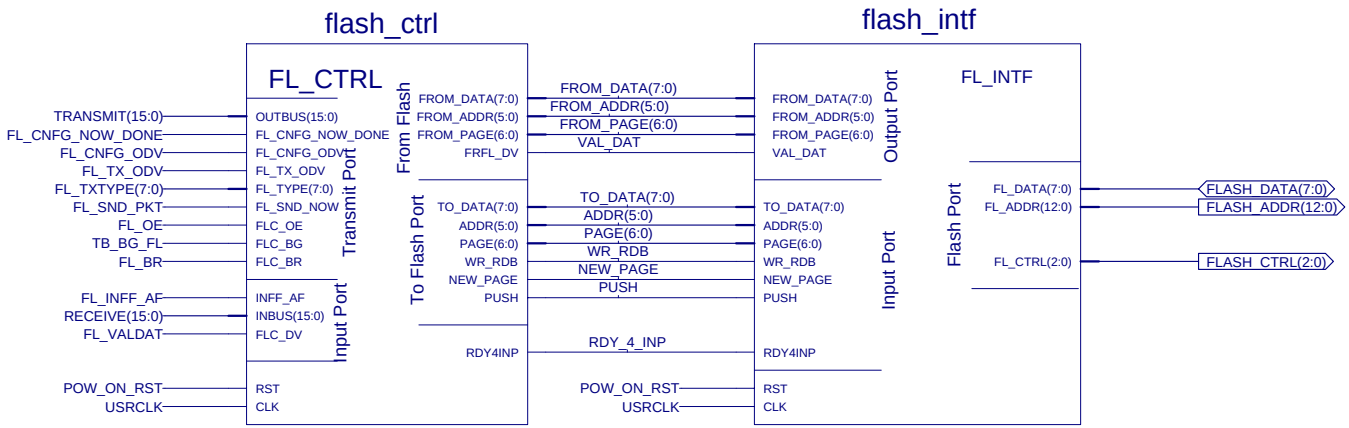
Title: VME Master and System Controller
Subtitle: External FIFO Interface
Project: D783C
Revision: 3.55
Name: Gigabit Ethernet VME Controller
Date: Wed Mar 08 11:53:56 2006
Sheet 3 of 9



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Title: VME Master and System Controller

Subtitle: Flash Memory Interface

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:53:56 2006	Sheet 4 of 9

1 2 3 4 5 6 7 8

A B C D

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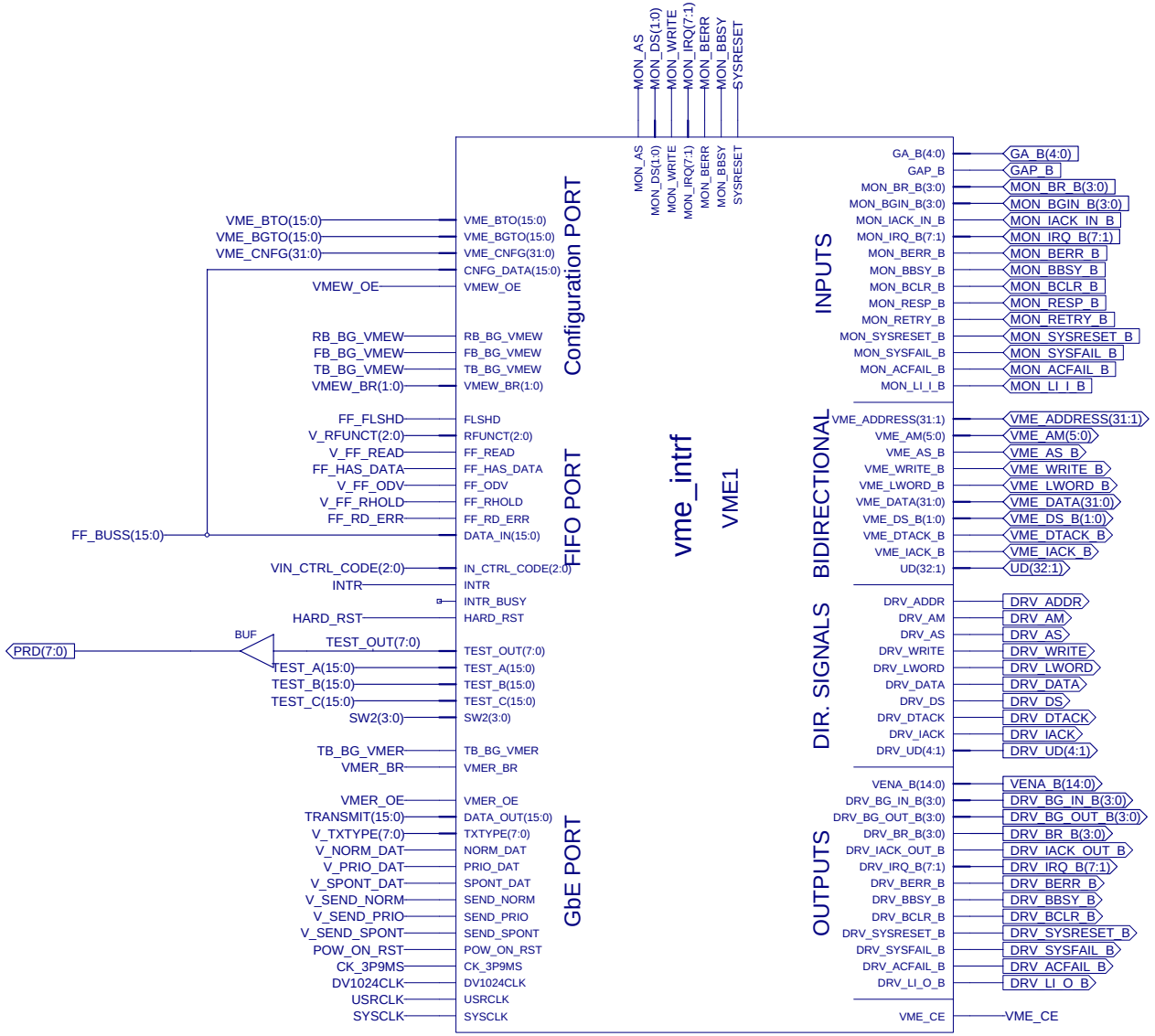
Title: VME Master and System Controller

Subtitle: JTAG Interface

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:53:56 2006	Sheet 5 of 9

1 2 3 4 5 6 7 8



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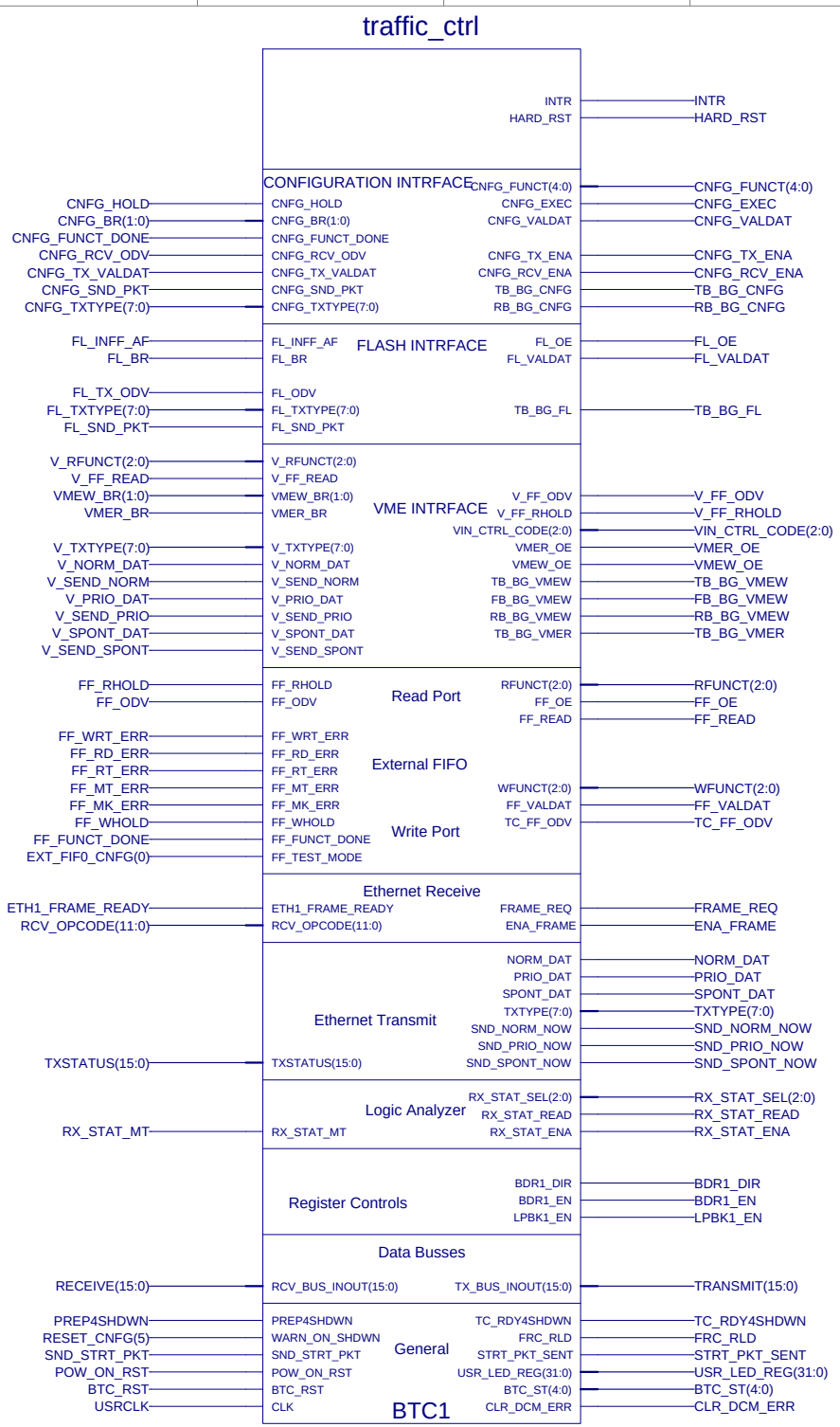
Title: VME Master and System Controller

Subtitle: VME Interface

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:53:56 2006	Sheet 6 of 9



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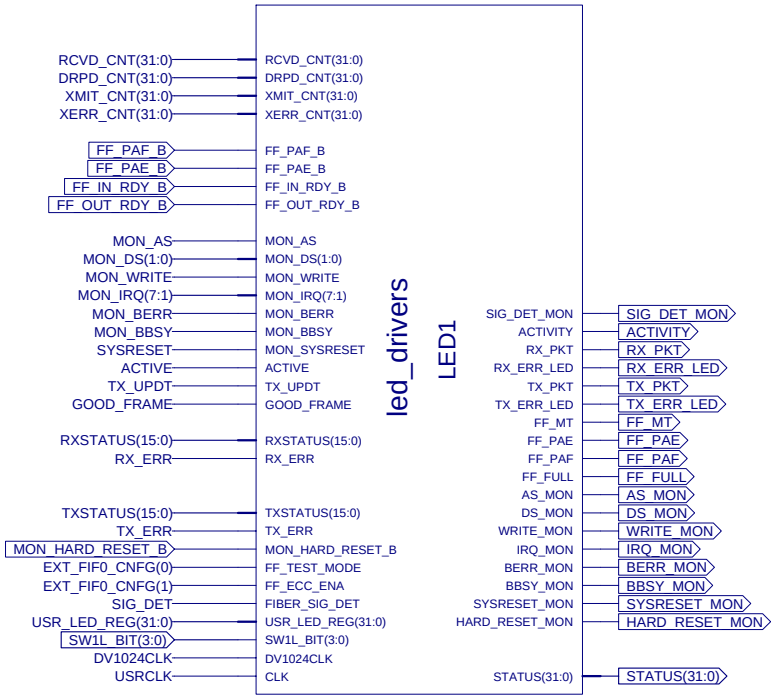
Title: VME Master and System Controller

Subtitle: Bus Traffic Controller

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:53:56 2006	Sheet 7 of 9



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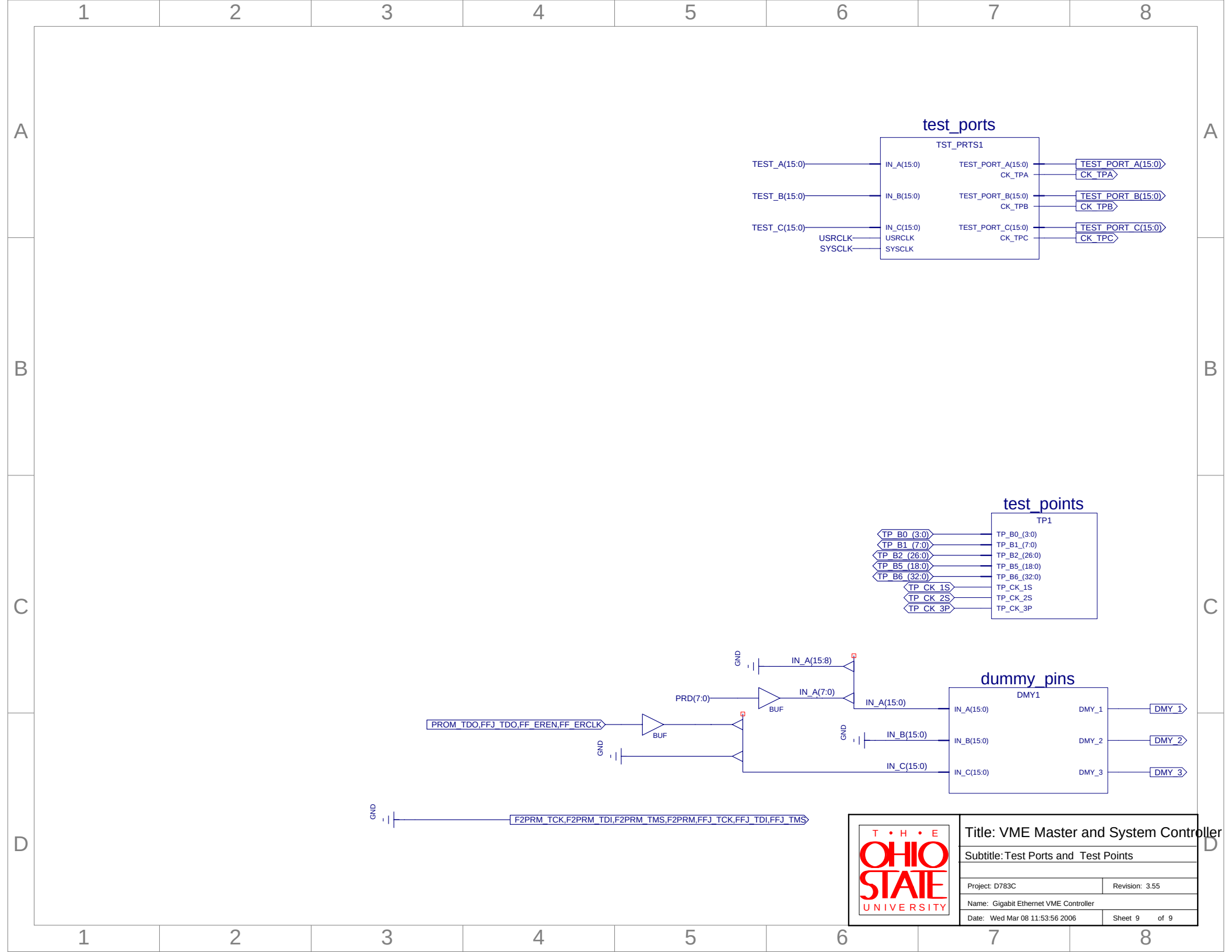
Title: VME Master and System Controller

Subtitle: Status and Monitoring (LEDs)

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:53:56 2006	Sheet 8 of 9


test_ports
TST_PRTS1
TEST_A(15:0)
IN_A(15:0)
TEST_PORT_A(15:0)
CK_TPA
TEST_PORT_A(15:0)
CK_TPA
TEST_B(15:0)
IN_B(15:0)
TEST_PORT_B(15:0)
CK_TPB
TEST_PORT_B(15:0)
CK_TPB
TEST_C(15:0)
IN_C(15:0)
TEST_PORT_C(15:0)
CK_TPC
TEST_PORT_C(15:0)
CK_TPC
USRCLK
USRCLK
SYSCLK
SYSCLK
test_points
TP1
TP_B0_(3:0)
TP_B1_(7:0)
TP_B2_(26:0)
TP_B5_(18:0)
TP_B6_(32:0)
TP_CK_1S
TP_CK_2S
TP_CK_3P
TP_B0_(3:0)
TP_B1_(7:0)
TP_B2_(26:0)
TP_B5_(18:0)
TP_B6_(32:0)
TP_CK_1S
TP_CK_2S
TP_CK_3P
dummy_pins
DMY1
GND
IN_A(15:8)
PRD(7:0)
IN_A(7:0)
BUF
IN_A(15:0)
IN_A(15:0)
DMY_1
DMY_1
PROM_TDO,FFJ_TDO,FF_EREN,FF_ERCLK
BUF
GND
IN_B(15:0)
IN_B(15:0)
DMY_2
DMY_2
GND
IN_C(15:0)
IN_C(15:0)
DMY_3
DMY_3
GND
F2PRM_TCK,F2PRM_TDI,F2PRM_TMS,F2PRM,FFJ_TCK,FFJ_TDI,FFJ_TMS
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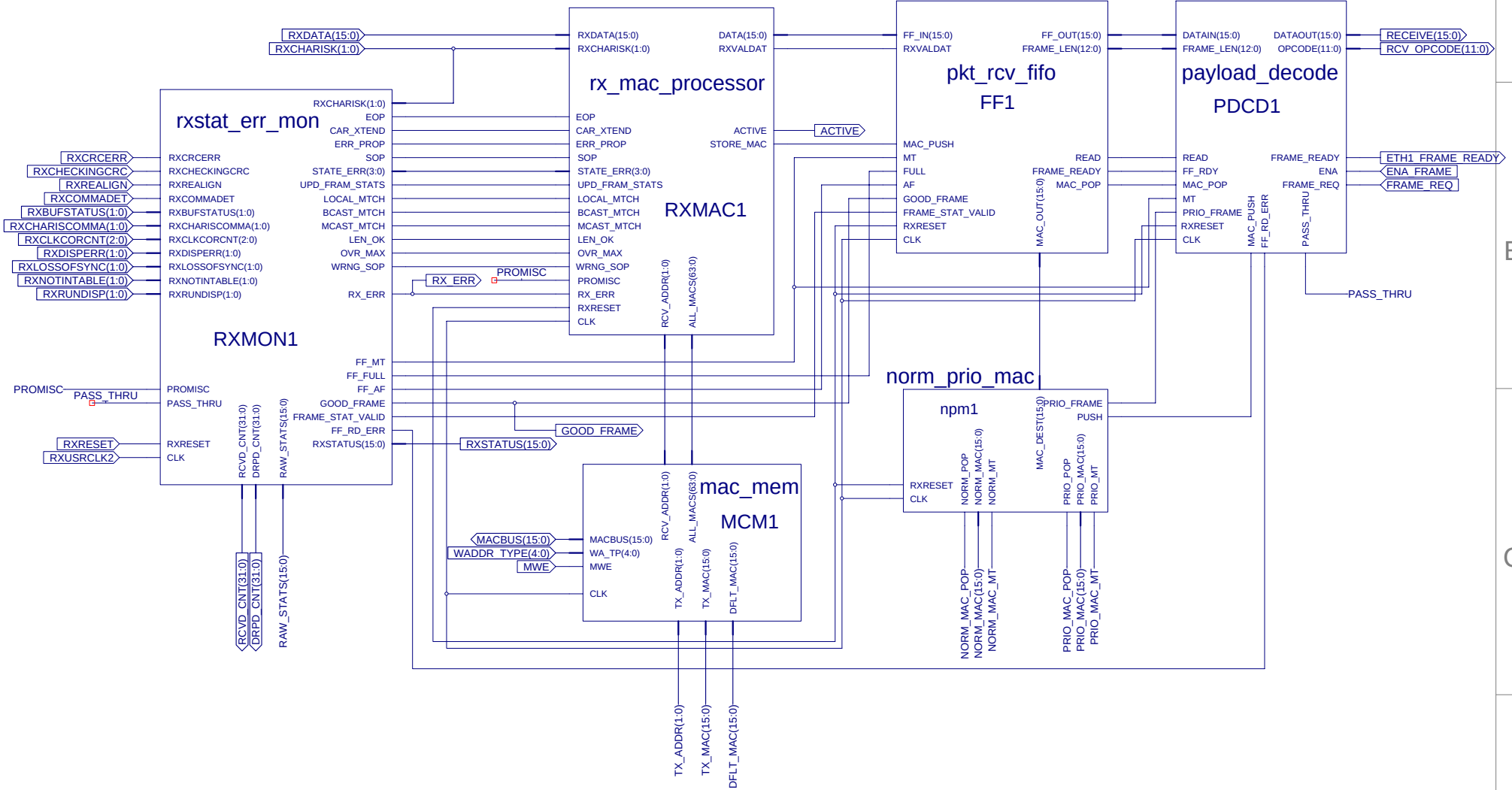
Title: VME Master and System Controller
Subtitle: Test Ports and Test Points
Project: D783C
Revision: 3.55
Name: Gigabit Ethernet VME Controller
Date: Wed Mar 08 11:53:56 2006
Sheet 9 of 9



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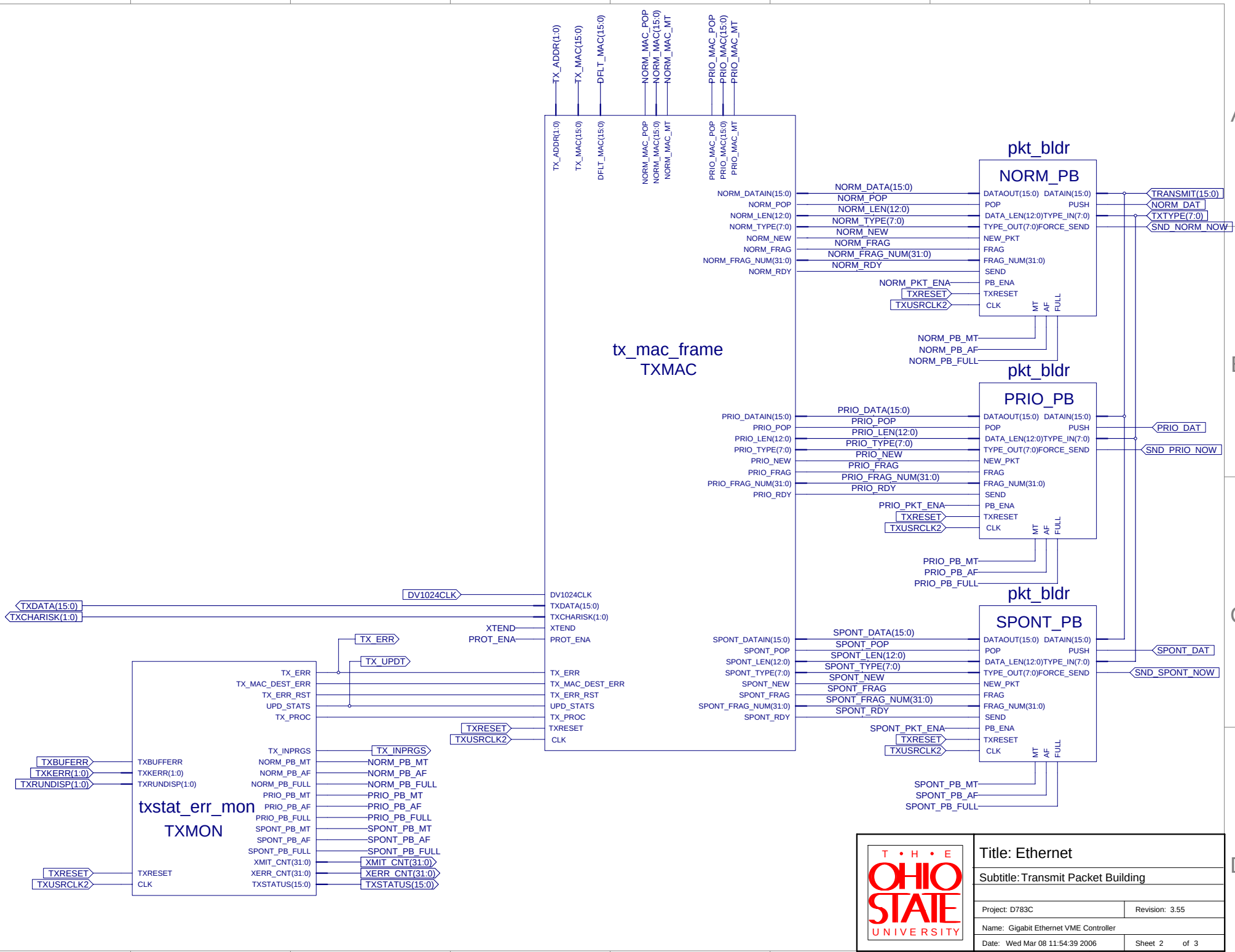
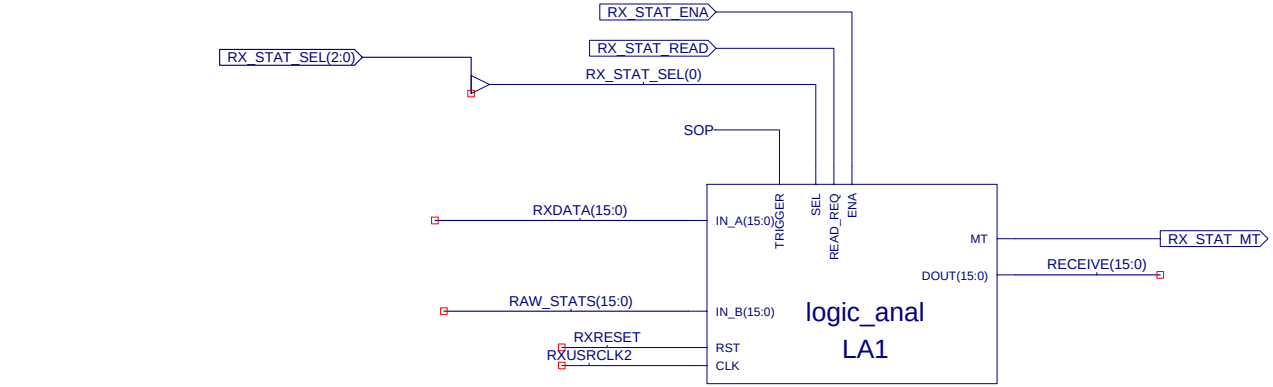
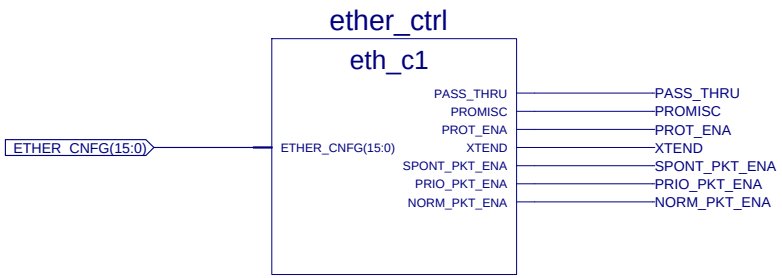
Title: Ethernet

Subtitle: Receiv Packet Processing

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:54:39 2006	Sheet 1 of 3


TX_ADDR(1:0)
TX_MAC(15:0)
DFLT_MAC(15:0)
NORM_MAC_POP
NORM_MAC(15:0)
NORM_MAC_MT
PRIO_MAC_POP
PRIO_MAC(15:0)
PRIO_MAC_MT
pkt_bldr
NORM_PB
NORM_DATA(15:0)
NORM_POP
NORM_LEN(12:0)
NORM_TYPE(7:0)
NORM_NEW
NORM_FRAG
NORM_FRAG_NUM(31:0)
NORM_RDY
NORM_PKT_ENA
TXRESET
TXUSRCLK2
DATAOUT(15:0)
DATAIN(15:0)
POP
PUSH
DATA_LEN(12:0)
TYPE_IN(7:0)
TYPE_OUT(7:0)
FORCE_SEND
NEW_PKT
FRAG
FRAG_NUM(31:0)
SEND
PB_ENA
TXRESET
CLK
MT
AF
FULL
TRANSMIT(15:0)
NORM_DAT
TXTYPE(7:0)
SND_NORM_NOW
NORM_PB_MT
NORM_PB_AF
NORM_PB_FULL
tx_mac_frame
TXMAC
pkt_bldr
PRIO_PB
PRIO_DATA(15:0)
PRIO_POP
PRIO_LEN(12:0)
PRIO_TYPE(7:0)
PRIO_NEW
PRIO_FRAG
PRIO_FRAG_NUM(31:0)
PRIO_RDY
PRIO_PKT_ENA
PRIO_DAT
SND_PRIO_NOW
PRIO_PB_MT
PRIO_PB_AF
PRIO_PB_FULL
pkt_bldr
SPONT_PB
SPONT_DATA(15:0)
SPONT_POP
SPONT_LEN(12:0)
SPONT_TYPE(7:0)
SPONT_NEW
SPONT_FRAG
SPONT_FRAG_NUM(31:0)
SPONT_RDY
SPONT_PKT_ENA
SPONT_DAT
SND_SPONT_NOW
SPONT_PB_MT
SPONT_PB_AF
SPONT_PB_FULL
DV1024CLK
TXDATA(15:0)
TXCHARISK(1:0)
XTEND
PROT_ENA
TX_ERR
TX_UPDT
TX_MAC_DEST_ERR
TX_ERR_RST
UPD_STATS
TX_PROC
TXRESET
TXUSRCLK2
CLK
TX_INPRGS
NORM_PB_MT
NORM_PB_AF
NORM_PB_FULL
PRIO_PB_MT
PRIO_PB_AF
PRIO_PB_FULL
SPONT_PB_MT
SPONT_PB_AF
SPONT_PB_FULL
XMIT_CNT(31:0)
XERR_CNT(31:0)
TXSTATUS(15:0)
TXBUFERR
TXKERR(1:0)
TXRUNDISP(1:0)
txstat_err_mon
TXMON
THE OHIO STATE UNIVERSITY
Title: Ethernet
Subtitle: Transmit Packet Building
Project: D783C
Revision: 3.55
Name: Gigabit Ethernet VME Controller
Date: Wed Mar 08 11:54:39 2006
Sheet 2 of 3





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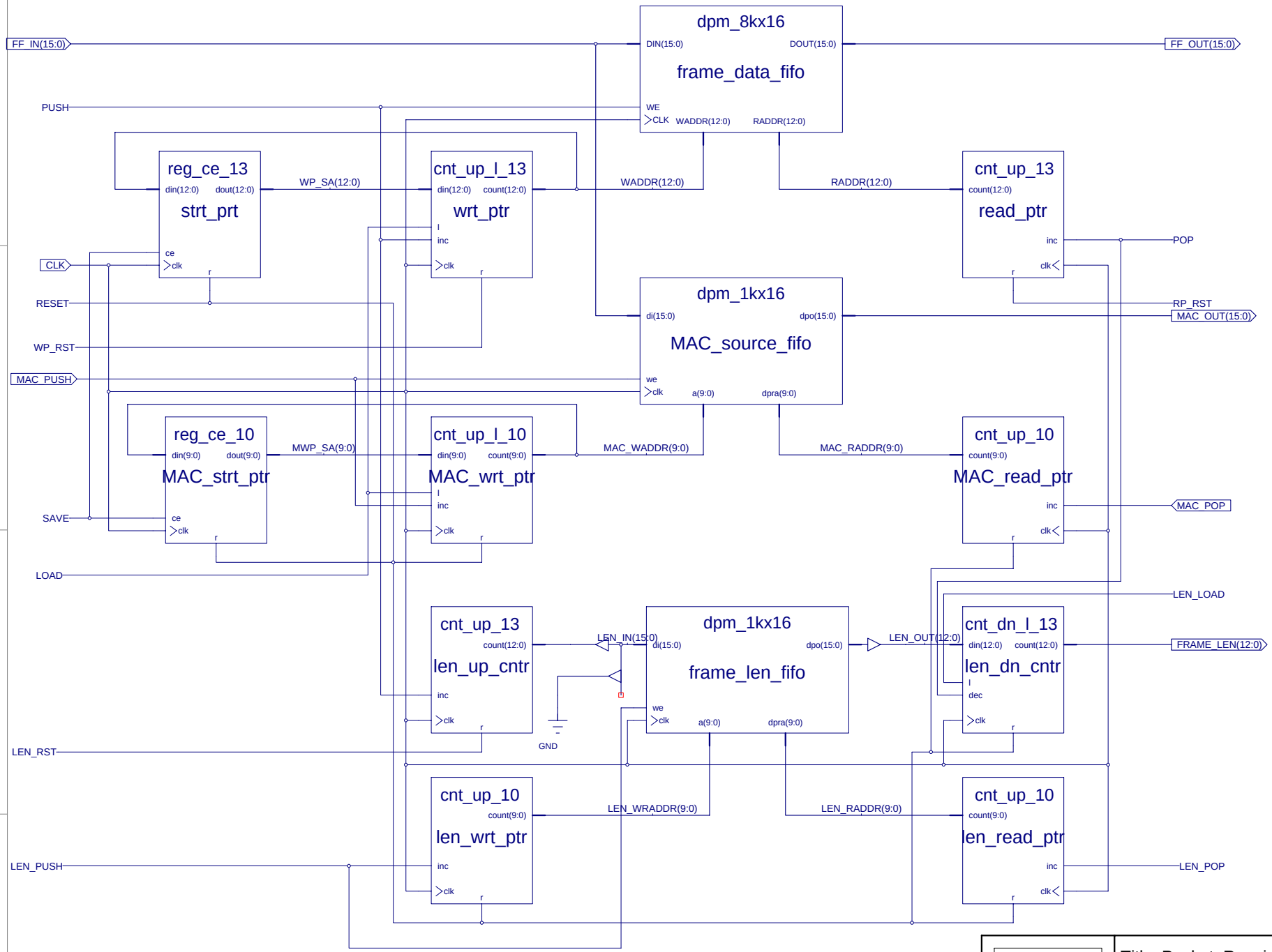
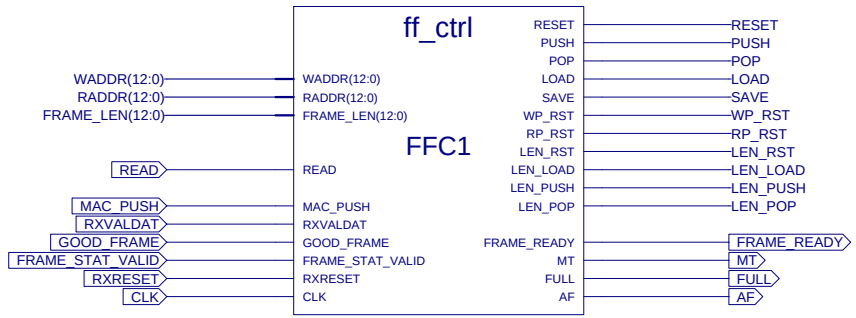
Title: Ethernet

Subtitle: Logic Analyzer

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:54:39 2006	Sheet 3 of 3


dpm_8kx16
DIN(15:0)
DOUT(15:0)
frame_data_fifo
WE
CLK
WADDR(12:0)
RADDR(12:0)
FF_IN(15:0)
FF_OUT(15:0)
PUSH
reg_ce_13
din(12:0)
dout(12:0)
strt_prt
ce
clk
r
WP_SA(12:0)
cnt_up_l_13
din(12:0)
count(12:0)
wrt_ptr
l
inc
WADDR(12:0)
RADDR(12:0)
cnt_up_13
count(12:0)
read_ptr
inc
POP
CLK
RESET
WP_RST
dpm_1kx16
di(15:0)
dpo(15:0)
MAC_source_fifo
we
a(9:0)
dpra(9:0)
RP_RST
MAC_OUT(15:0)
MAC_PUSH
reg_ce_10
din(9:0)
dout(9:0)
MAC_strt_ptr
MWP_SA(9:0)
cnt_up_l_10
din(9:0)
count(9:0)
MAC_wrt_ptr
MAC_WADDR(9:0)
MAC_RADDR(9:0)
cnt_up_10
count(9:0)
MAC_read_ptr
MAC_POP
SAVE
LOAD
LEN_LOAD
cnt_up_13
count(12:0)
len_up_cntr
LEN_IN(15:0)
dpm_1kx16
di(15:0)
dpo(15:0)
frame_len_fifo
we
a(9:0)
dpra(9:0)
LEN_OUT(12:0)
cnt_dn_l_13
din(12:0)
count(12:0)
len_dn_cntr
l
dec
clk
r
FRAME_LEN(12:0)
GND
LEN_RST
cnt_up_10
count(9:0)
len_wrt_ptr
LEN_WRADDR(9:0)
LEN_RADDR(9:0)
cnt_up_10
count(9:0)
len_read_ptr
LEN_PUSH
LEN_POP
THE OHIO STATE UNIVERSITY
Title: Packet Receiver FIFO
Subtitle: FIFOs and counters
Project: D783C
Revision: 3.55
Name: Gigabit Ethernet VME Contoller
Date: Wed Mar 08 11:55:49 2006
Sheet 1 of 2



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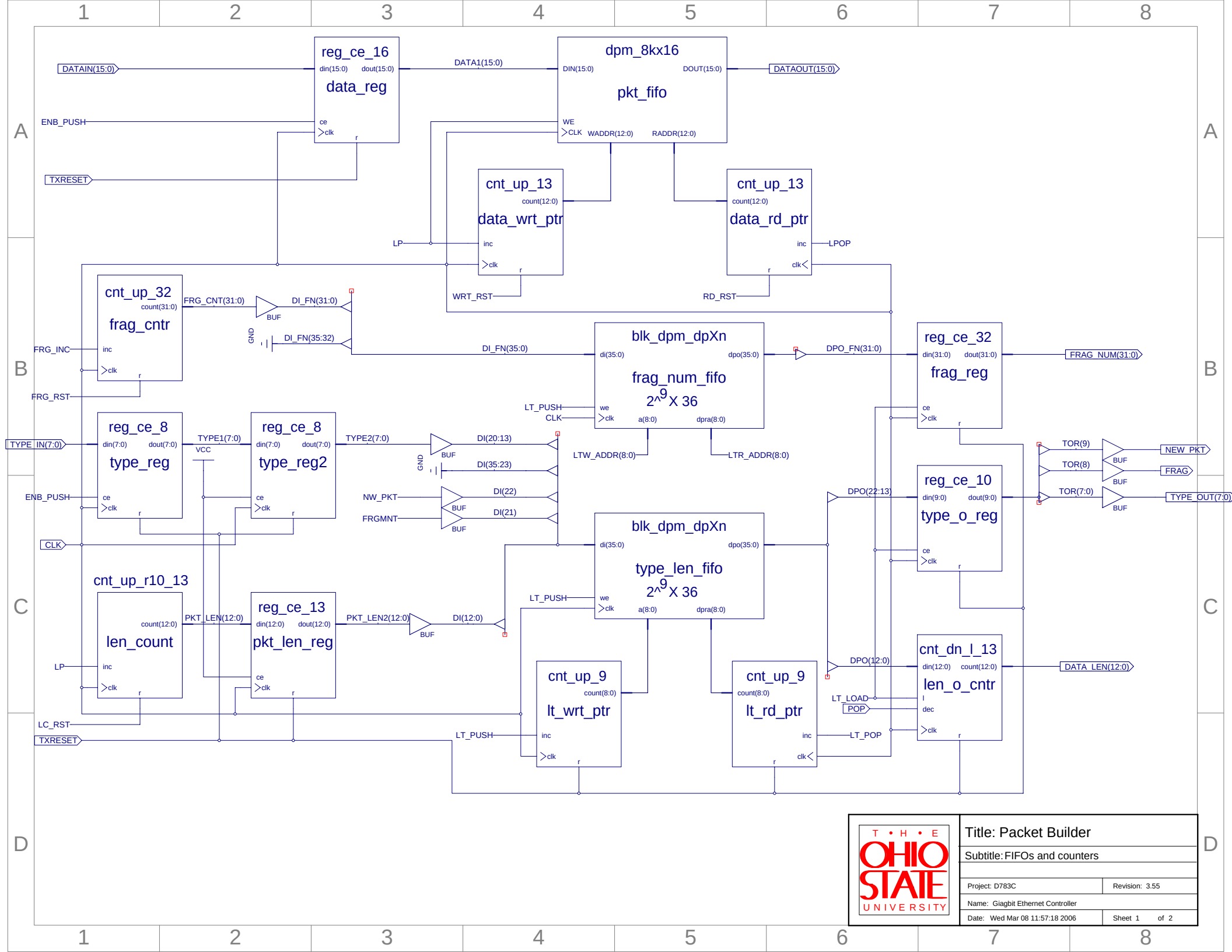
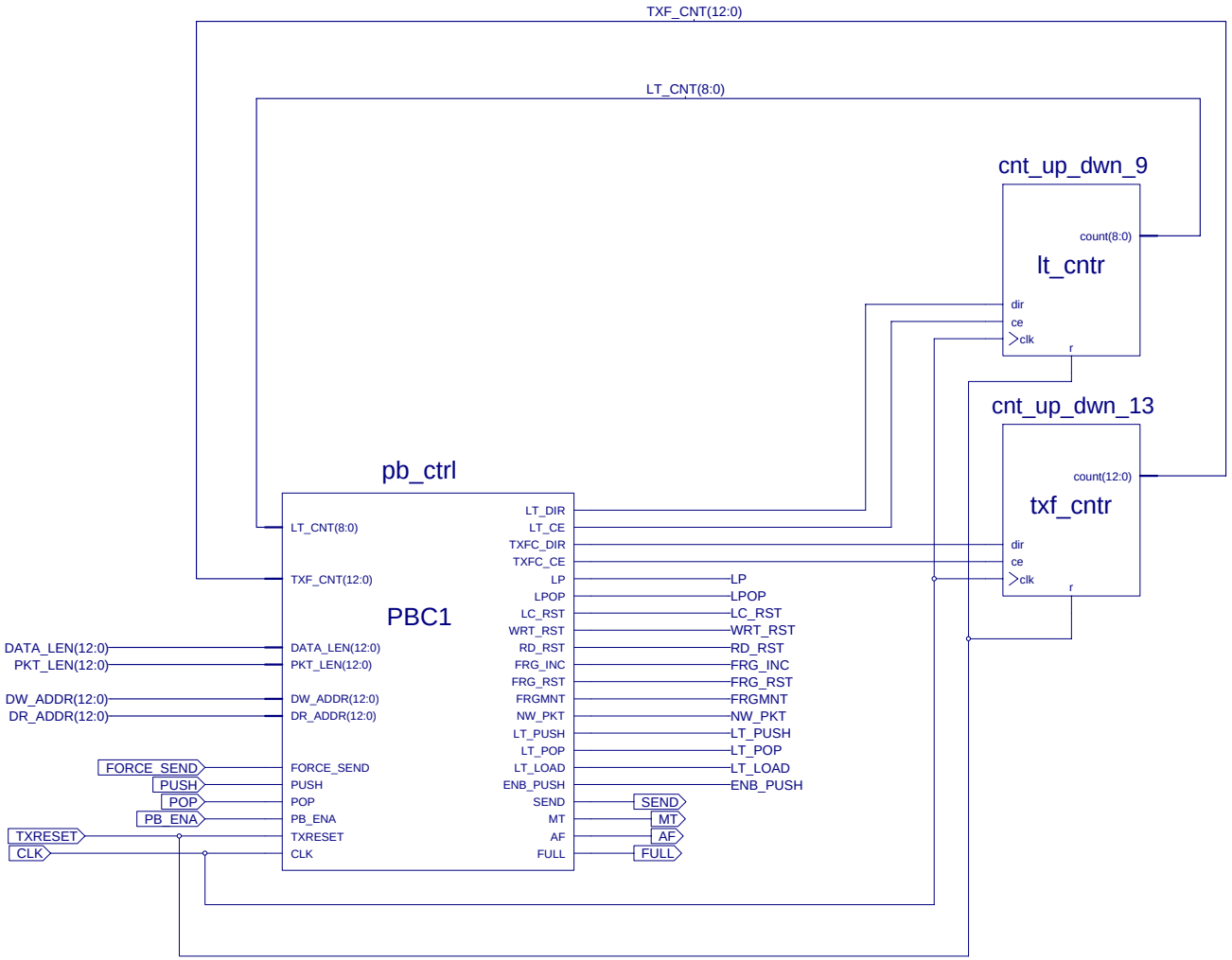
Title: Packet Receiver FIFO

Subtitle: FIFO Controller

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:55:49 2006	Sheet 2 of 2


reg_ce_16
din(15:0) dout(15:0)
data_reg
DATAIN(15:0)
DATA1(15:0)
dpm_8kx16
DIN(15:0) DOUT(15:0)
pkt_fifo
WE CLK WADDR(12:0) RADDR(12:0)
DATAOUT(15:0)
ENB_PUSH
TXRESET
cnt_up_13
count(12:0)
data_wrt_ptr
inc clk
cnt_up_13
count(12:0)
data_rd_ptr
inc clk
LP
LPOP
WRT_RST
RD_RST
cnt_up_32
count(31:0)
frag_cntr
inc clk
FRG_CNT(31:0)
BUF
DI_FN(31:0)
GND
DI_FN(35:32)
DI_FN(35:0)
blk_dpm_dpXn
di(35:0) dpo(35:0)
frag_num_fifo
2^9 X 36
we clk a(8:0) dpra(8:0)
DPO_FN(31:0)
reg_ce_32
din(31:0) dout(31:0)
frag_reg
ce clk
FRAG_NUM(31:0)
FRG_INC
FRG_RST
LT_PUSH
CLK
LTW_ADDR(8:0)
LTR_ADDR(8:0)
reg_ce_8
din(7:0) dout(7:0)
type_reg
ce clk
TYPE_IN(7:0)
TYPE1(7:0)
VCC
reg_ce_8
din(7:0) dout(7:0)
type_reg2
ce clk
TYPE2(7:0)
BUF
GND
DI(20:13)
DI(35:23)
NW_PKT
FRGMNT
DI(22)
DI(21)
TOR(9)
TOR(8)
TOR(7:0)
NEW_PKT
FRAG
TYPE_OUT(7:0)
ENB_PUSH
CLK
DPO(22:13)
reg_ce_10
din(9:0) dout(9:0)
type_o_reg
ce clk
blk_dpm_dpXn
di(35:0) dpo(35:0)
type_len_fifo
2^9 X 36
we clk a(8:0) dpra(8:0)
LT_PUSH
cnt_up_r10_13
count(12:0)
len_count
inc clk
PKT_LEN(12:0)
reg_ce_13
din(12:0) dout(12:0)
pkt_len_reg
ce clk
PKT_LEN2(12:0)
BUF
DI(12:0)
LP
LC_RST
TXRESET
cnt_up_9
count(8:0)
lt_wrt_ptr
inc clk
LT_PUSH
cnt_up_9
count(8:0)
lt_rd_ptr
inc clk
LT_POP
DPO(12:0)
LT_LOAD
POP
cnt_dn_l_13
din(12:0) count(12:0)
len_o_cntr
l
dec
clk
DATA_LEN(12:0)
THE OHIO STATE UNIVERSITY
Title: Packet Builder
Subtitle: FIFOs and counters
Project: D783C
Revision: 3.55
Name: Giagbit Ethernet Controller
Date: Wed Mar 08 11:57:18 2006
Sheet 1 of 2



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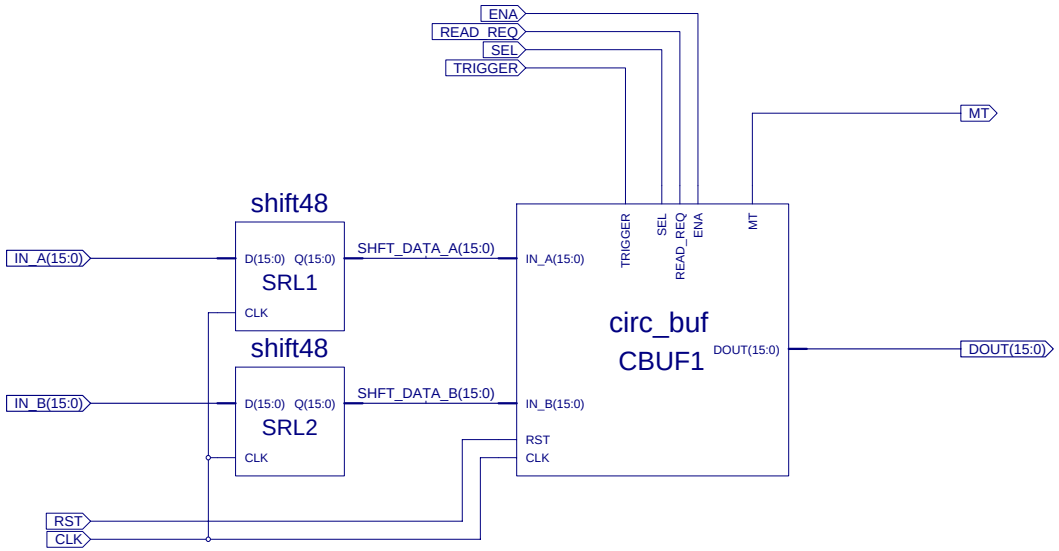
Title: Packet Builder

Subtitle: FIFO controller

Project: D783C	Revision: 3.55
Name: Giagbit Ethernet Controller	
Date: Wed Mar 08 11:57:18 2006	Sheet 2 of 2



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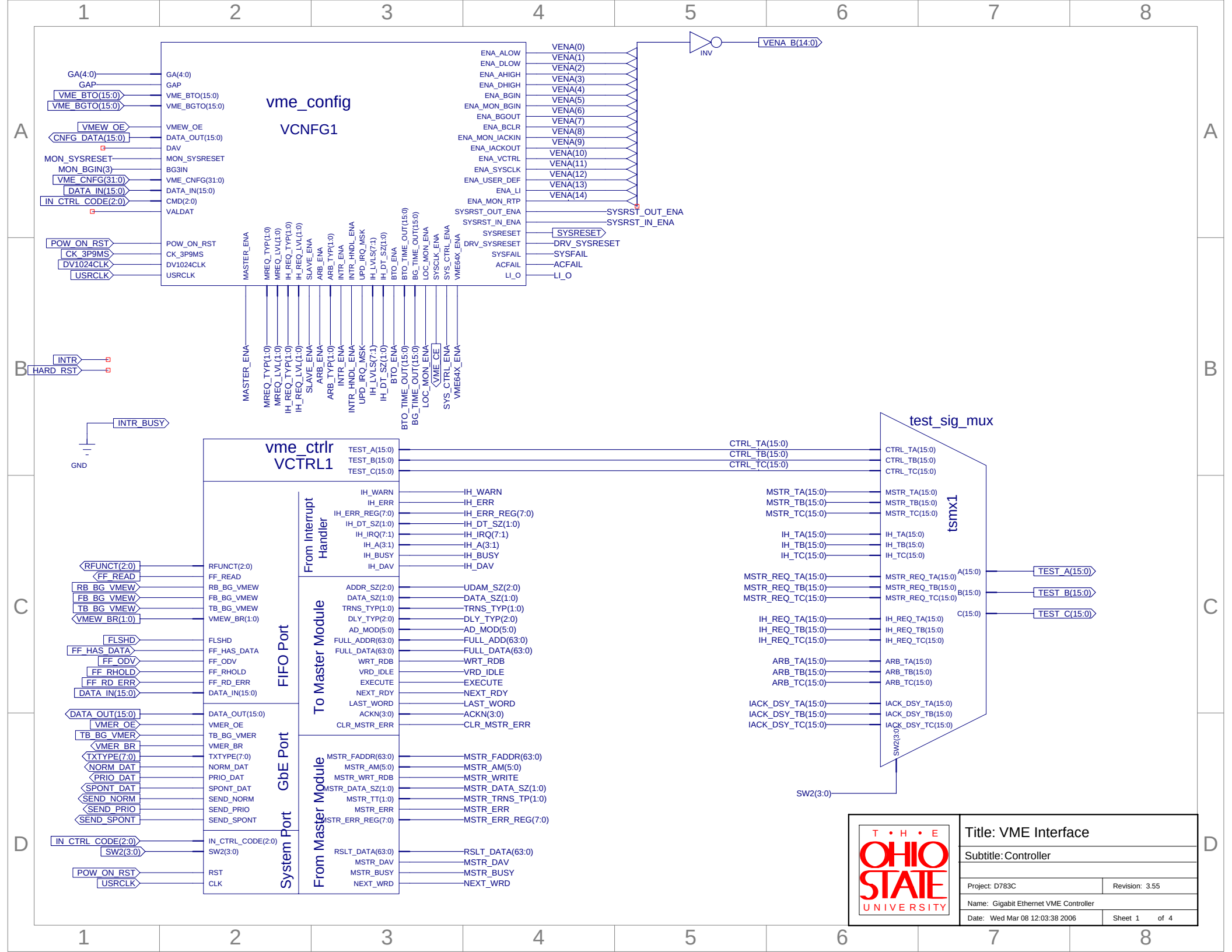
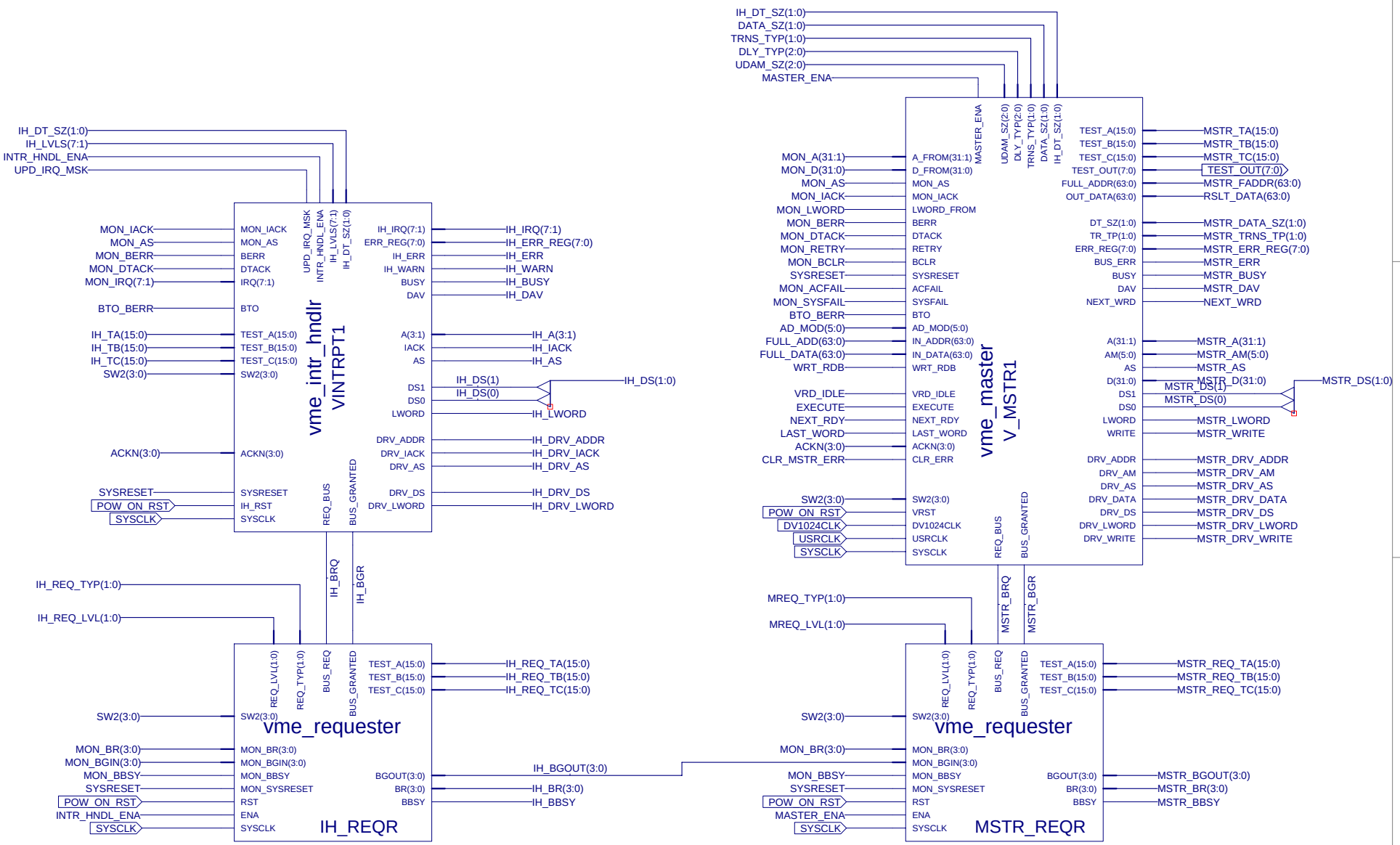
Title: Logic Analyzer

Subtitle: Circular Buffer

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 11:59:44 2006	Sheet 1 of 1


vme_config
VCNFG1
GA(4:0)
GAP
VME_BTO(15:0)
VME_BGTO(15:0)
VMEW_OE
CNFG_DATA(15:0)
DAV
MON_SYSRESET
MON_BGIN(3)
VME_CNFG(31:0)
DATA_IN(15:0)
IN_CTRL_CODE(2:0)
VALDAT
POW_ON_RST
CK_3P9MS
DV1024CLK
USRCLK
ENA_ALOW
ENA_DLOW
ENA_AHIGH
ENA_DHIGH
ENA_BGIN
ENA_MON_BGIN
ENA_BGOUT
ENA_BCLR
ENA_MON_IACKIN
ENA_IACKOUT
ENA_VCTRL
ENA_SYSCLK
ENA_USER_DEF
ENA_LI
ENA_MON_RTP
SYSRST_OUT_ENA
SYSRST_IN_ENA
SYSRESET
DRV_SYSRESET
SYSFAIL
ACFAIL
LI_O
VENA(0)
VENA(1)
VENA(2)
VENA(3)
VENA(4)
VENA(5)
VENA(6)
VENA(7)
VENA(8)
VENA(9)
VENA(10)
VENA(11)
VENA(12)
VENA(13)
VENA(14)
INV
VENA_B(14:0)
SYSRST_OUT_ENA
SYSRST_IN_ENA
SYSRESET
DRV_SYSRESET
SYSFAIL
ACFAIL
LI_O
MASTER_ENA
MREQ_TYP(1:0)
MREQ_LVL(1:0)
IH_REQ_TYP(1:0)
IH_REQ_LVL(1:0)
SLAVE_ENA
ARB_ENA
ARB_TYP(1:0)
INTR_ENA
INTR_HNDL_ENA
UPD_IRQ_MSK
IH_LVLS(7:1)
IH_DT_SZ(1:0)
BTO_ENA
BTO_TIME_OUT(15:0)
BG_TIME_OUT(15:0)
LOC_MON_ENA
VME_CE
SYS_CTRL_ENA
VME64X_ENA
INTR
HARD_RST
INTR_BUSY
GND
vme_ctrlr
VCTRL1
TEST_A(15:0)
TEST_B(15:0)
TEST_C(15:0)
From Interrupt Handler
IH_WARN
IH_ERR
IH_ERR_REG(7:0)
IH_DT_SZ(1:0)
IH_IRQ(7:1)
IH_A(3:1)
IH_BUSY
IH_DAV
FIFO Port
RFUNCT(2:0)
FF_READ
RB_BG_VMEW
FB_BG_VMEW
TB_BG_VMEW
VMEW_BR(1:0)
FLSHD
FF_HAS_DATA
FF_ODV
FF_RHOLD
FF_RD_ERR
DATA_IN(15:0)
To Master Module
ADDR_SZ(2:0)
DATA_SZ(1:0)
TRNS_TYP(1:0)
DLY_TYP(2:0)
AD_MOD(5:0)
FULL_ADDR(63:0)
FULL_DATA(63:0)
WRT_RDB
VRD_IDLE
EXECUTE
NEXT_RDY
LAST_WORD
ACKN(3:0)
CLR_MSTR_ERR
UDAM_SZ(2:0)
DATA_SZ(1:0)
TRNS_TYP(1:0)
DLY_TYP(2:0)
AD_MOD(5:0)
FULL_ADD(63:0)
FULL_DATA(63:0)
WRT_RDB
VRD_IDLE
EXECUTE
NEXT_RDY
LAST_WORD
ACKN(3:0)
CLR_MSTR_ERR
GbE Port
DATA_OUT(15:0)
VMER_OE
TB_BG_VMER
VMER_BR
TXTYPE(7:0)
NORM_DAT
PRIO_DAT
SPONT_DAT
SEND_NORM
SEND_PRIO
SEND_SPONT
From Master Module
MSTR_FADDR(63:0)
MSTR_AM(5:0)
MSTR_WRT_RDB
MSTR_DATA_SZ(1:0)
MSTR_TT(1:0)
MSTR_ERR
MSTR_ERR_REG(7:0)
RSLT_DATA(63:0)
MSTR_DAV
MSTR_BUSY
NEXT_WRD
MSTR_FADDR(63:0)
MSTR_AM(5:0)
MSTR_WRITE
MSTR_DATA_SZ(1:0)
MSTR_TRNS_TP(1:0)
MSTR_ERR
MSTR_ERR_REG(7:0)
RSLT_DATA(63:0)
MSTR_DAV
MSTR_BUSY
NEXT_WRD
System Port
IN_CTRL_CODE(2:0)
SW2(3:0)
RST
CLK
test_sig_mux
tsmx1
CTRL_TA(15:0)
CTRL_TB(15:0)
CTRL_TC(15:0)
MSTR_TA(15:0)
MSTR_TB(15:0)
MSTR_TC(15:0)
IH_TA(15:0)
IH_TB(15:0)
IH_TC(15:0)
MSTR_REQ_TA(15:0)
MSTR_REQ_TB(15:0)
MSTR_REQ_TC(15:0)
IH_REQ_TA(15:0)
IH_REQ_TB(15:0)
IH_REQ_TC(15:0)
ARB_TA(15:0)
ARB_TB(15:0)
ARB_TC(15:0)
IACK_DSY_TA(15:0)
IACK_DSY_TB(15:0)
IACK_DSY_TC(15:0)
A(15:0)
B(15:0)
C(15:0)
SW2(3:0)
SW2(3:0)
THE OHIO STATE UNIVERSITY
Title: VME Interface
Subtitle: Controller
Project: D783C
Revision: 3.55
Name: Gigabit Ethernet VME Controller
Date: Wed Mar 08 12:03:38 2006
Sheet 1 of 4



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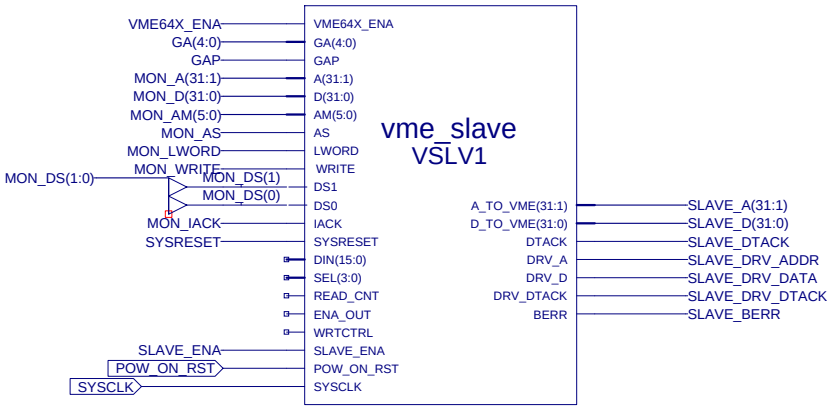
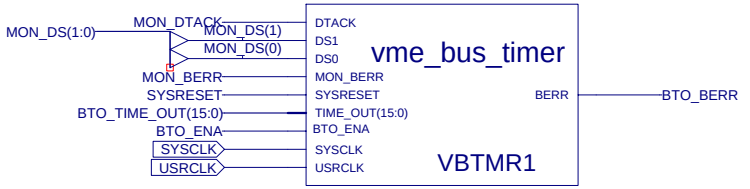
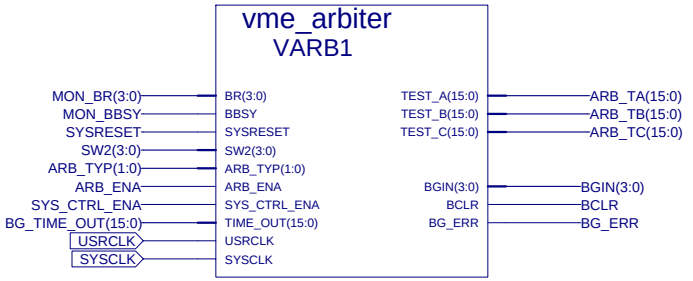
Title: VME Interface

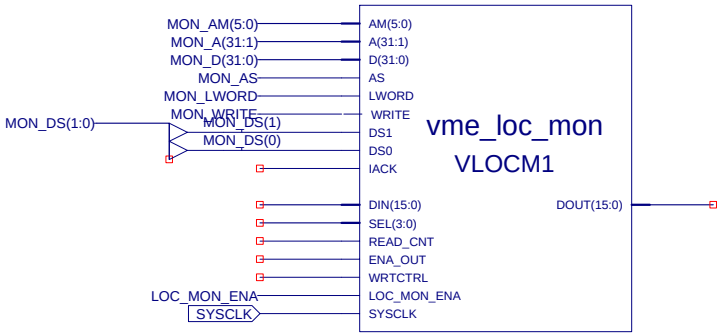
Subtitle: Master and Interrupt Handler

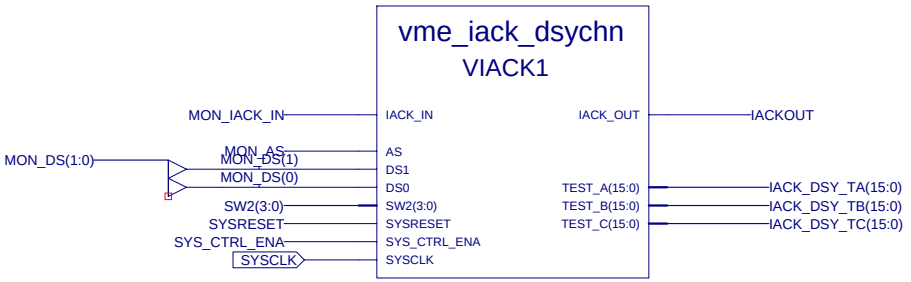
Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 12:03:38 2006	Sheet 2 of 4











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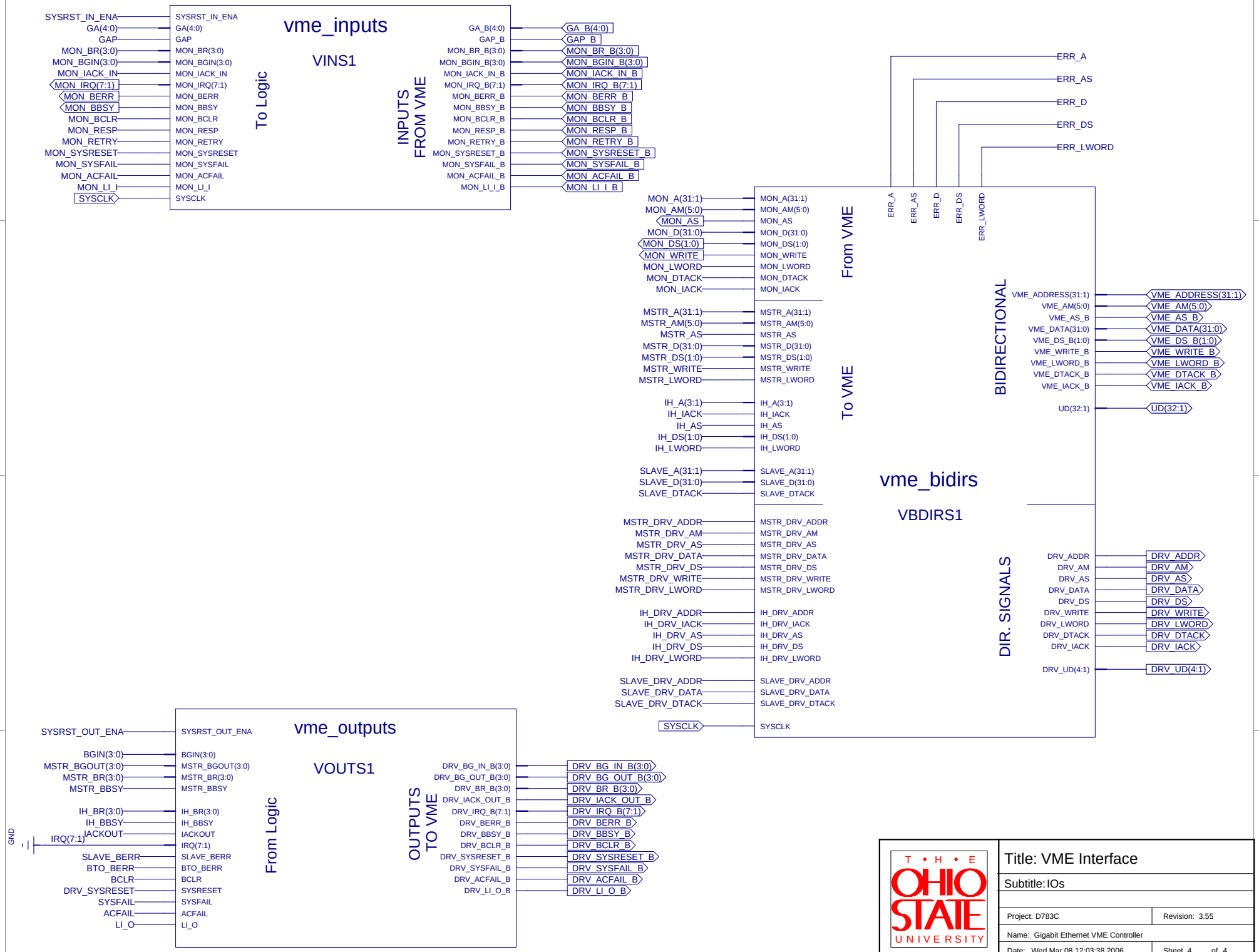
Title: VME Interface

Subtitle: Slave, Arbiter, Bus Timer, and Misc.

Project: D783C	Revision: 3.55
Name: Gigabit Ethernet VME Controller	
Date: Wed Mar 08 12:03:38 2006	Sheet 3 of 4


vme_inputs
VINS1
To Logic
INPUTS FROM VME
SYSRST_IN_ENA
GA(4:0)
GAP
MON_BR(3:0)
MON_BGIN(3:0)
MON_IACK_IN
MON_IRQ(7:1)
MON_BERR
MON_BBSY
MON_BCLR
MON_RESP
MON_RETRY
MON_SYSRESET
MON_SYSFAIL
MON_ACFAIL
MON_LI_I
SYSCLK
GA_B(4:0)
GAP_B
MON_BR_B(3:0)
MON_BGIN_B(3:0)
MON_IACK_IN_B
MON_IRQ_B(7:1)
MON_BERR_B
MON_BBSY_B
MON_BCLR_B
MON_RESP_B
MON_RETRY_B
MON_SYSRESET_B
MON_SYSFAIL_B
MON_ACFAIL_B
MON_LI_I_B
vme_bidirs
VBDIRS1
From VME
To VME
BIDIRECTIONAL
DIR. SIGNALS
ERR_A
ERR_AS
ERR_D
ERR_DS
ERR_LWORD
MON_A(31:1)
MON_AM(5:0)
MON_AS
MON_D(31:0)
MON_DS(1:0)
MON_WRITE
MON_LWORD
MON_DTACK
MON_IACK
MSTR_A(31:1)
MSTR_AM(5:0)
MSTR_AS
MSTR_D(31:0)
MSTR_DS(1:0)
MSTR_WRITE
MSTR_LWORD
IH_A(3:1)
IH_IACK
IH_AS
IH_DS(1:0)
IH_LWORD
SLAVE_A(31:1)
SLAVE_D(31:0)
SLAVE_DTACK
MSTR_DRV_ADDR
MSTR_DRV_AM
MSTR_DRV_AS
MSTR_DRV_DATA
MSTR_DRV_DS
MSTR_DRV_WRITE
MSTR_DRV_LWORD
IH_DRV_ADDR
IH_DRV_IACK
IH_DRV_AS
IH_DRV_DS
IH_DRV_LWORD
SLAVE_DRV_ADDR
SLAVE_DRV_DATA
SLAVE_DRV_DTACK
SYSCLK
VME_ADDRESS(31:1)
VME_AM(5:0)
VME_AS_B
VME_DATA(31:0)
VME_DS_B(1:0)
VME_WRITE_B
VME_LWORD_B
VME_DTACK_B
VME_IACK_B
UD(32:1)
DRV_ADDR
DRV_AM
DRV_AS
DRV_DATA
DRV_DS
DRV_WRITE
DRV_LWORD
DRV_DTACK
DRV_IACK
DRV_UD(4:1)
vme_outputs
VOUTS1
From Logic
OUTPUTS TO VME
SYSRST_OUT_ENA
BGIN(3:0)
MSTR_BGOUT(3:0)
MSTR_BR(3:0)
MSTR_BBSY
IH_BR(3:0)
IH_BBSY
IACKOUT
IRQ(7:1)
SLAVE_BERR
BTO_BERR
BCLR
DRV_SYSRESET
SYSFAIL
ACFAIL
LI_O
GND
DRV_BG_IN_B(3:0)
DRV_BG_OUT_B(3:0)
DRV_BR_B(3:0)
DRV_IACK_OUT_B
DRV_IRQ_B(7:1)
DRV_BERR_B
DRV_BBSY_B
DRV_BCLR_B
DRV_SYSRESET_B
DRV_SYSFAIL_B
DRV_ACFAIL_B
DRV_LI_O_B
THE OHIO STATE UNIVERSITY
Title: VME Interface
Subtitle: IOs
Project: D783C
Revision: 3.55
Name: Gigabit Ethernet VME Controller
Date: Wed Mar 08 12:03:38 2006
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