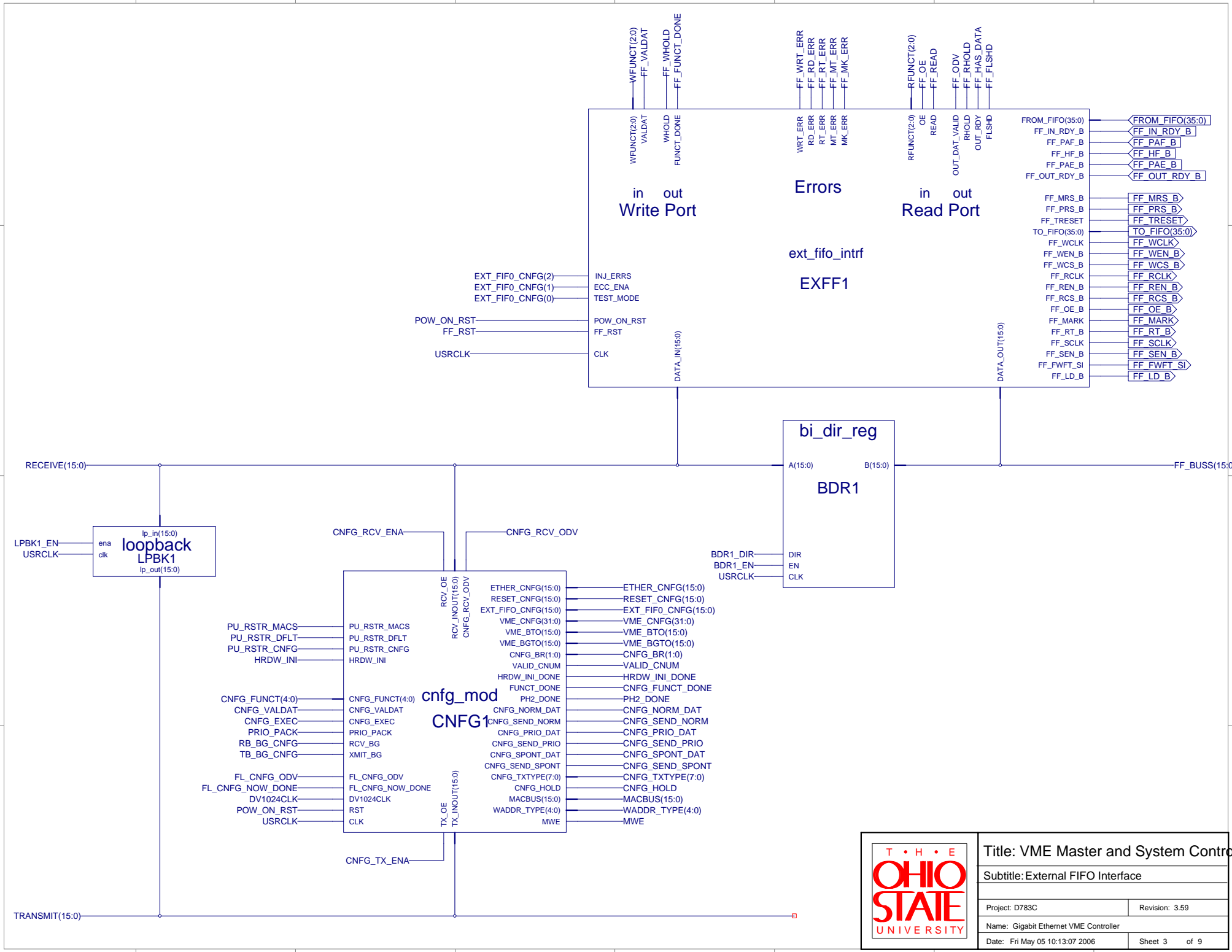
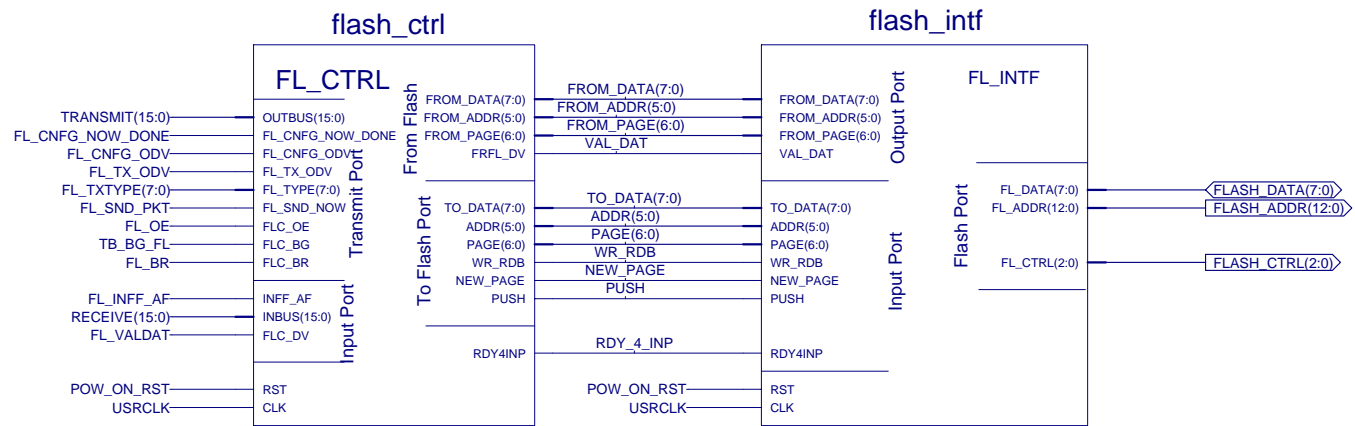


	<b>Title:</b> VME Master and System Controller	
	<b>Subtitle:</b> Start-up and Shutdown Sequencing	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:13:07 2006	Sheet 1	of 9





<b>Title: VME Master and System Controller</b>	
Subtitle: External FIFO Interface	
Project: D783C	Revision: 3.59
Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:13:07 2006	Sheet 3 of 9



1

2

3

4

5

6

7

8

A

A

B

B

C

C

D

D

1

2

3


4

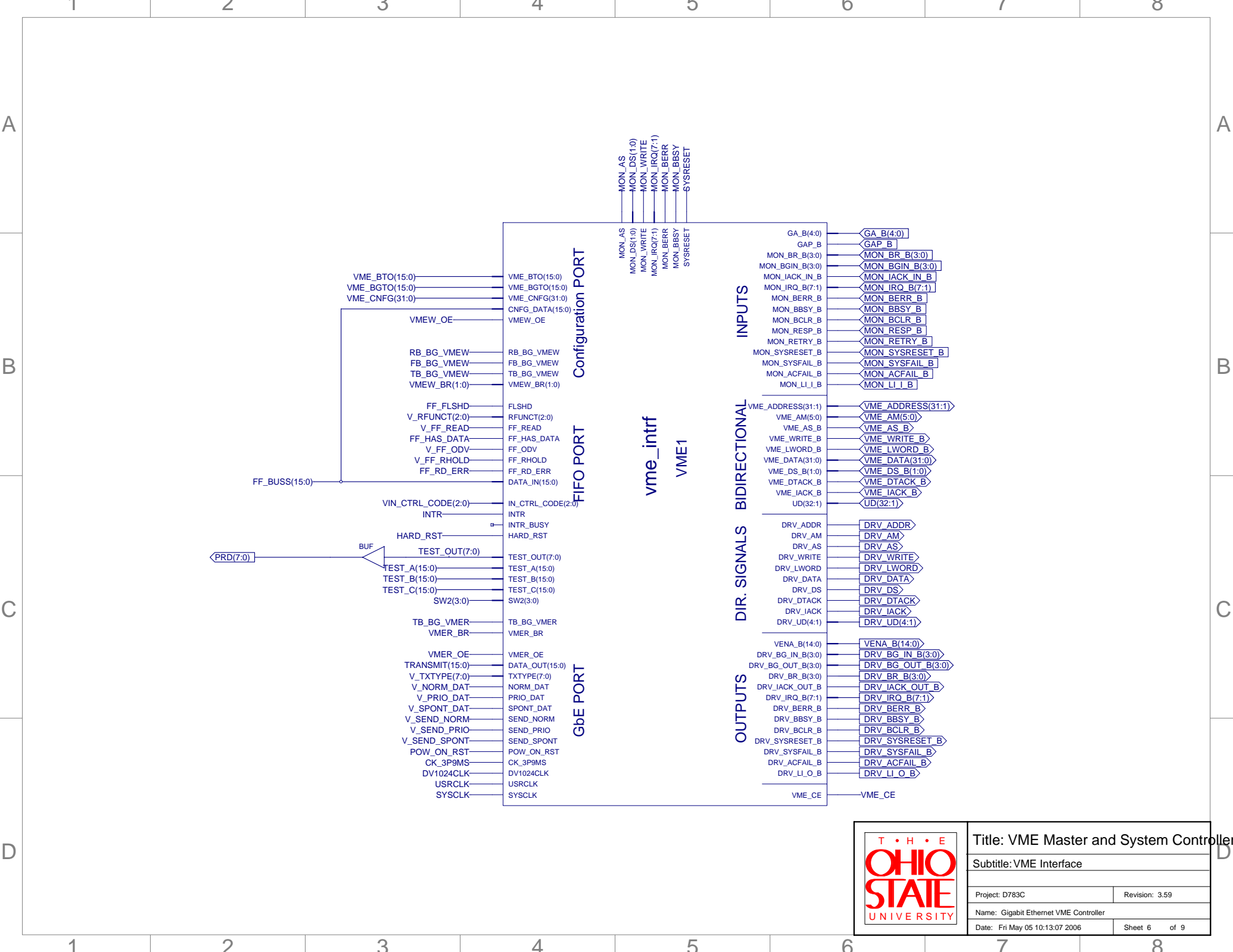
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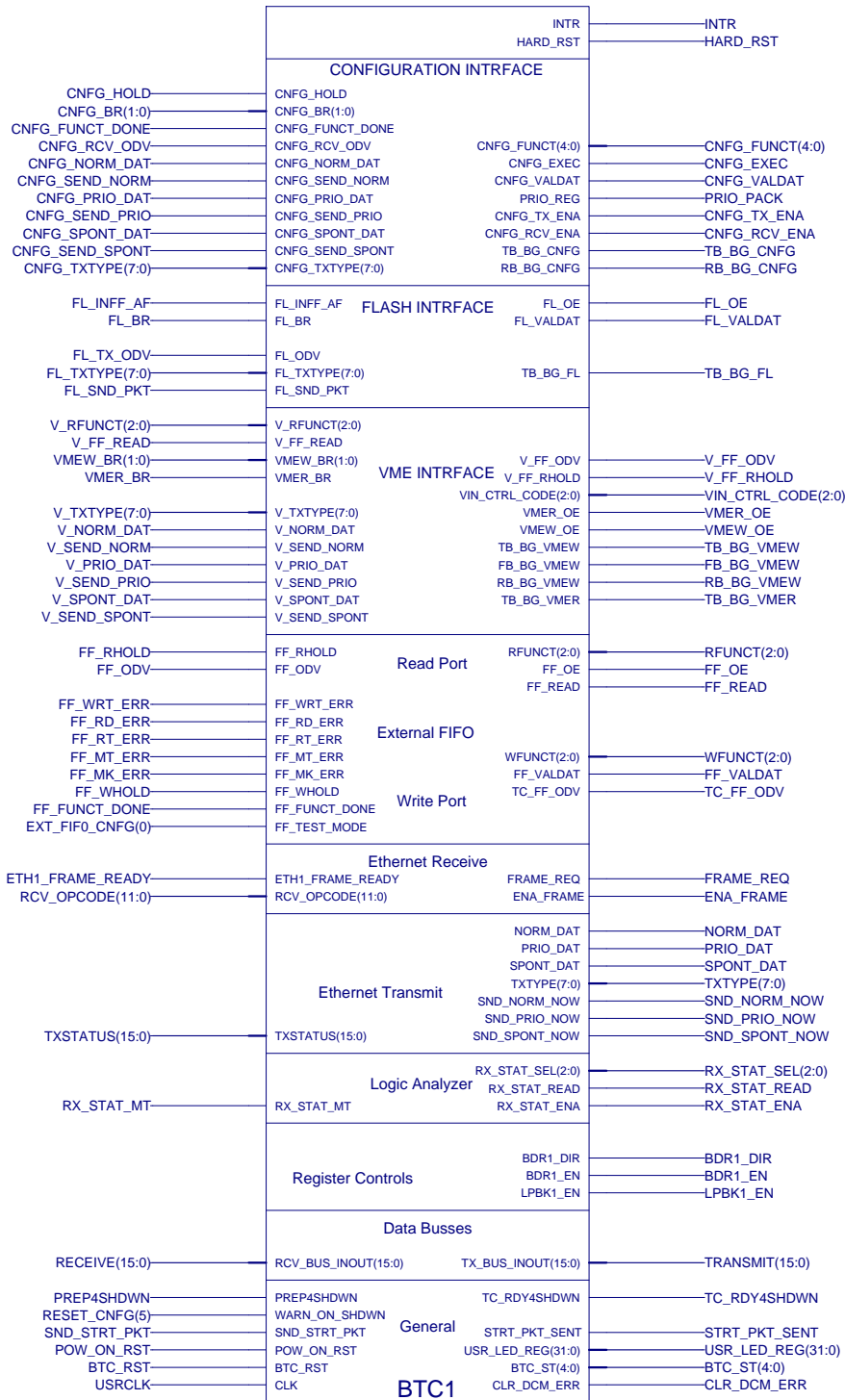
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	<b>Title:</b> VME Master and System Controller	
	Subtitle: JTAG Interface	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:13:07 2006	Sheet 5 of 9	

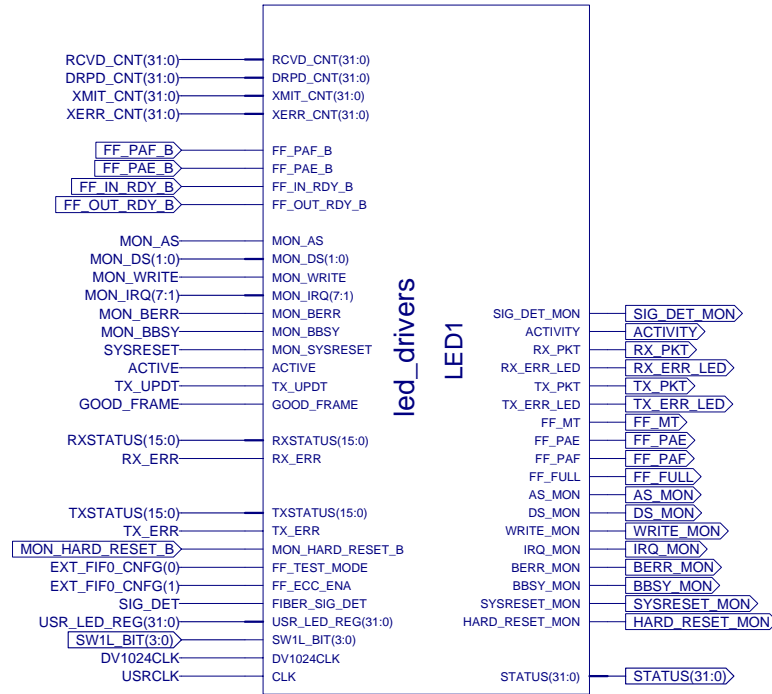


<b>Title:</b> VME Master and System Controller	
<b>Subtitle:</b> VME Interface	
<b>Project:</b> D783C	<b>Revision:</b> 3.59
<b>Name:</b> Gigabit Ethernet VME Controller	
<b>Date:</b> Fri May 05 10:13:07 2006	<b>Sheet</b> 6 <b>of</b> 9

# traffic\_ctrl



	<b>Title: VME Master and System Controller</b>	
	Subtitle: Bus Traffic Controller	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:13:07 2006		Sheet 7 of 9

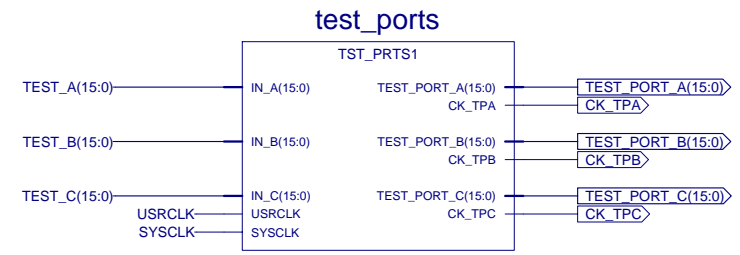




1 2 3 4 5 6 7 8

A

A

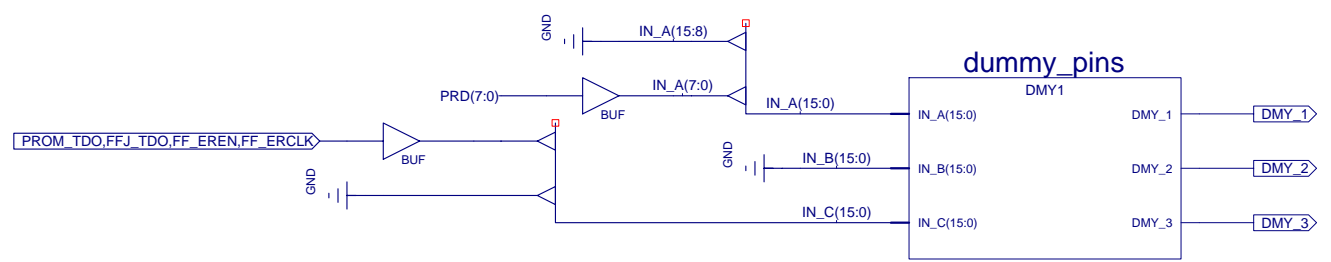
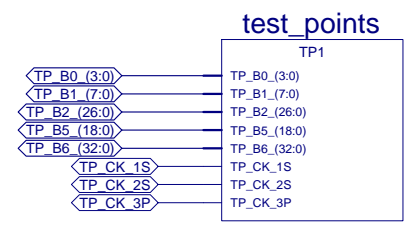


B

B

C

C

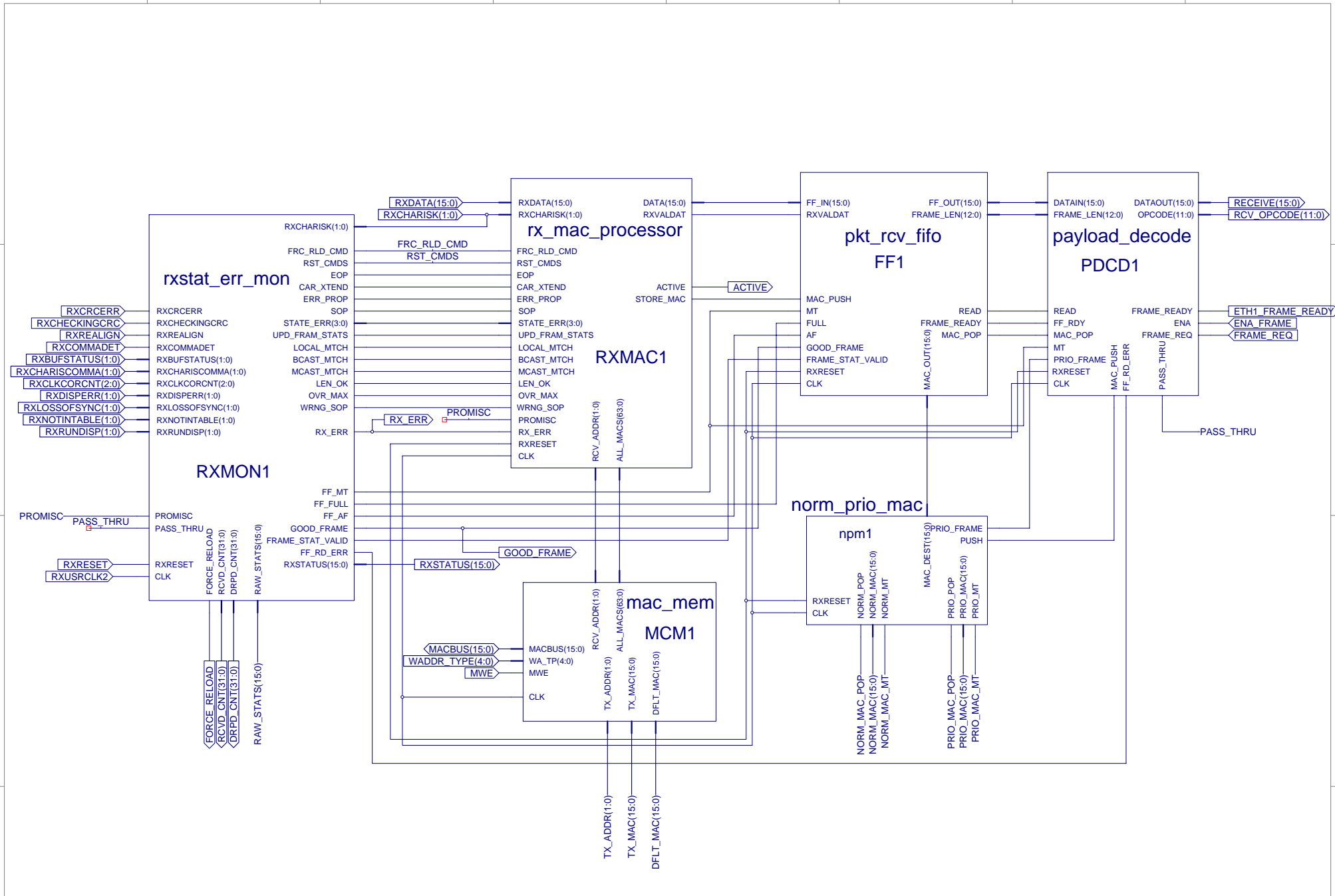



D

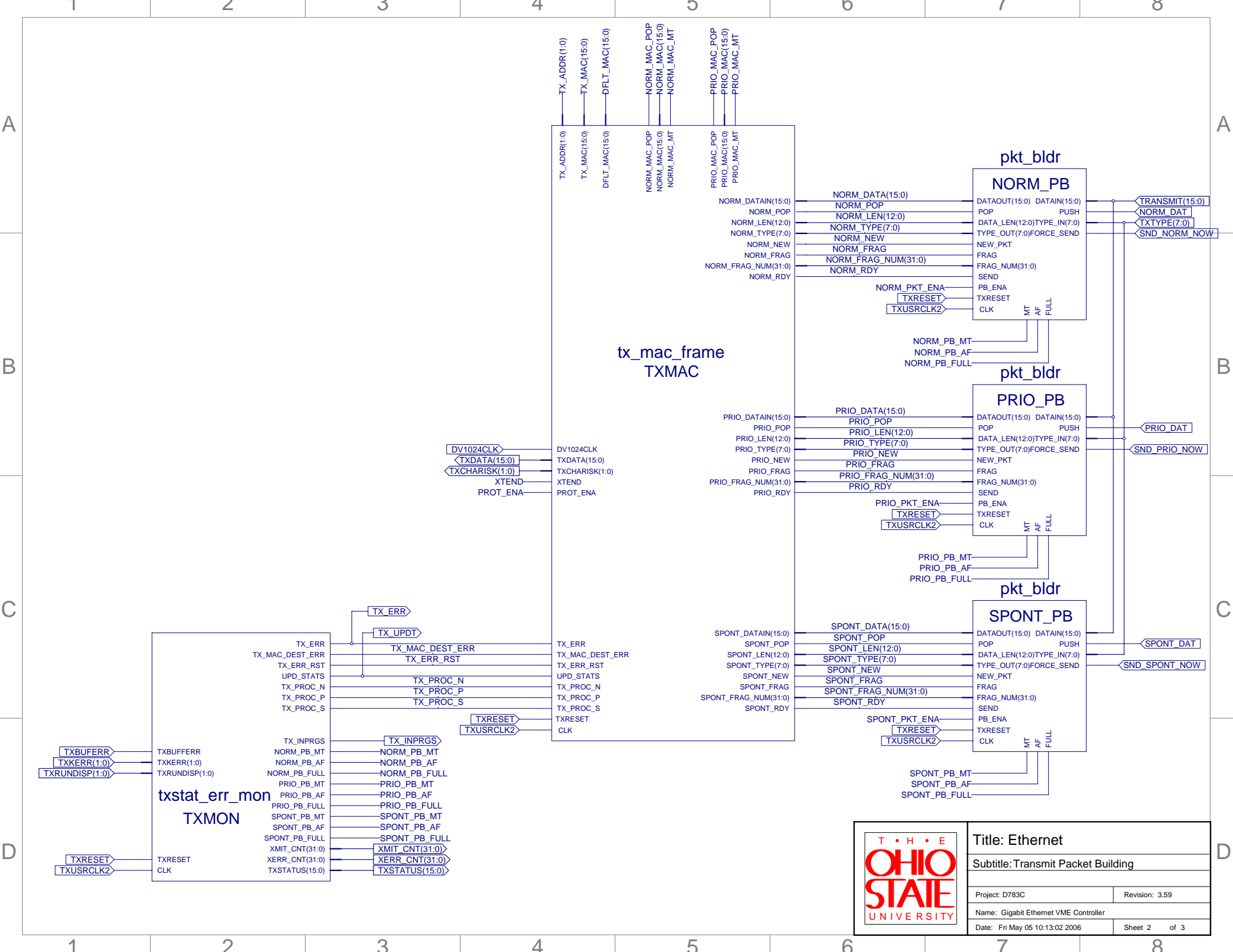
D

1 2 3 4 5 6 7 8

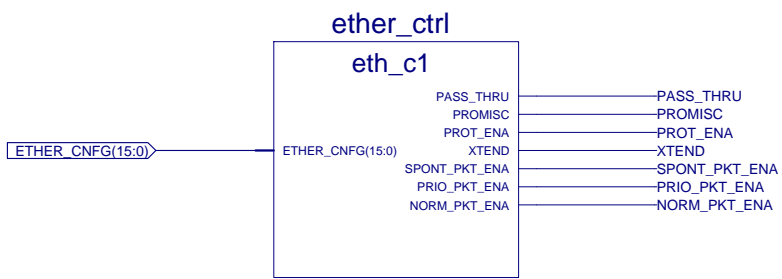
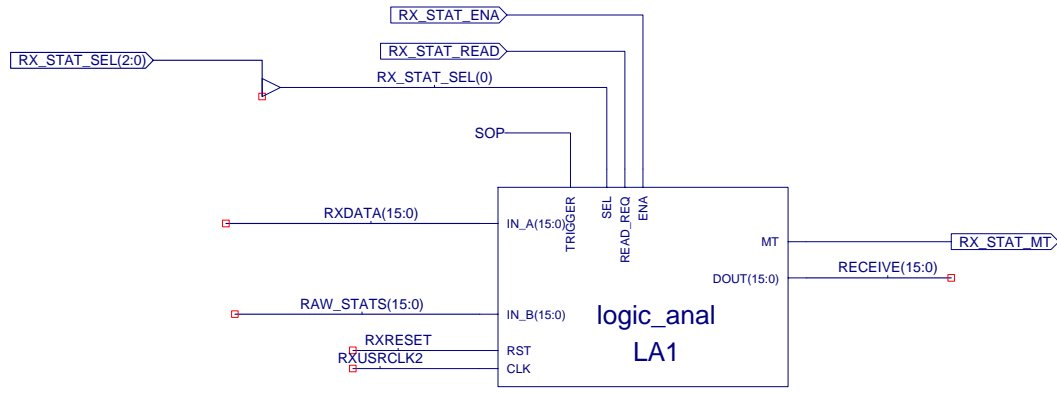
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	Subtitle: Test Ports and Test Points	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:13:07 2006	Sheet 9	of 9



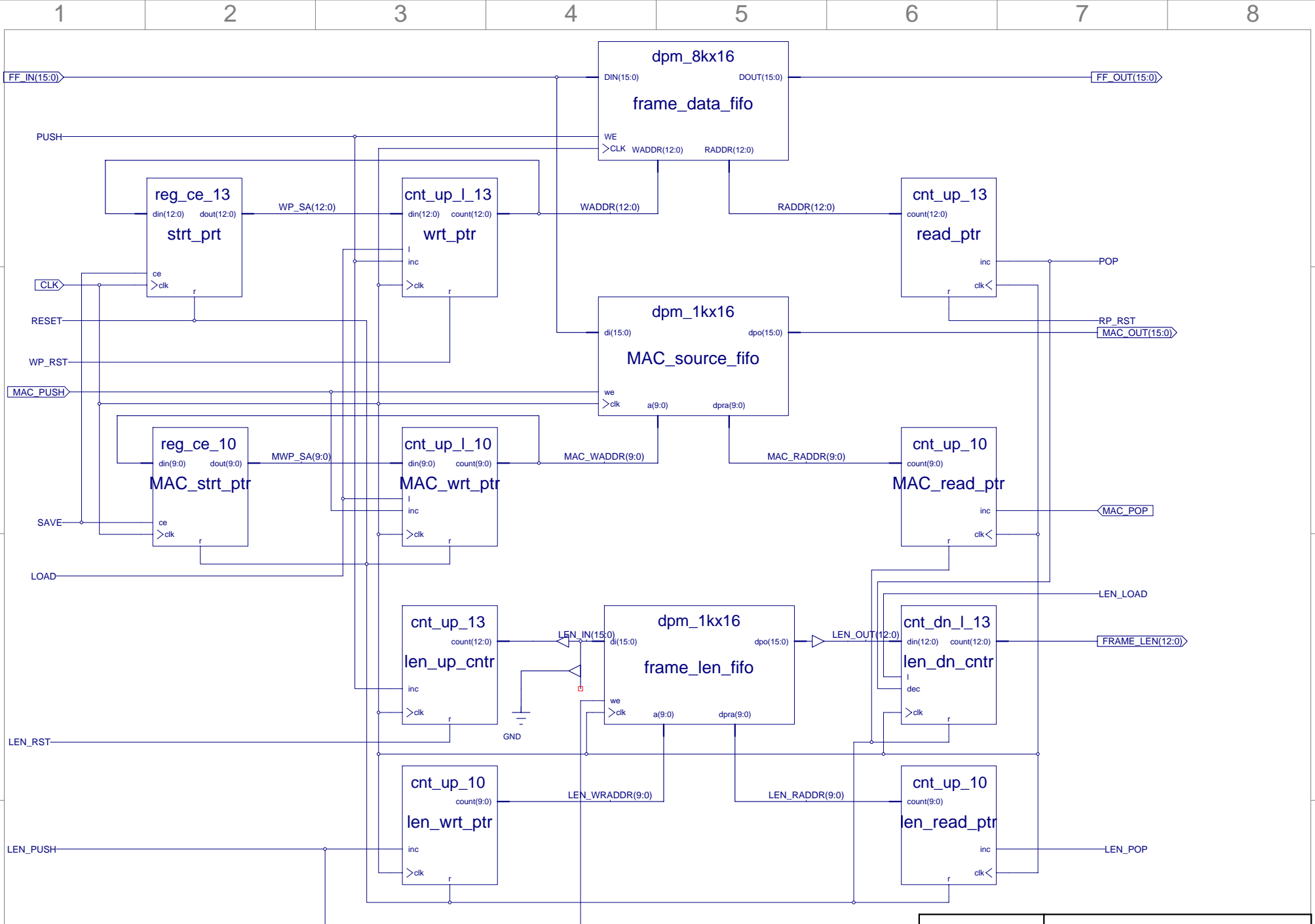
	<b>Title: Ethernet</b>	
	Subtitle: Receiv Packet Processing	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:13:02 2006		Sheet 1 of 3



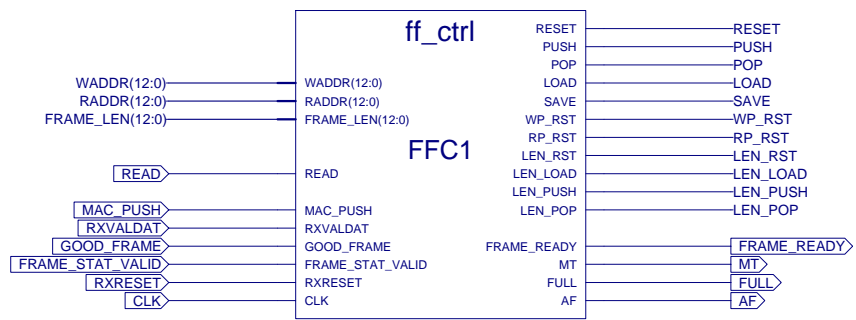
<b>Title:</b> Ethernet	
<b>Subtitle:</b> Transmit Packet Building	
<b>Project:</b> D783C	<b>Revision:</b> 3.59
<b>Name:</b> Gigabit Ethernet VME Controller	
<b>Date:</b> Fri May 05 10:13:02 2006	<b>Sheet 2</b> of 3



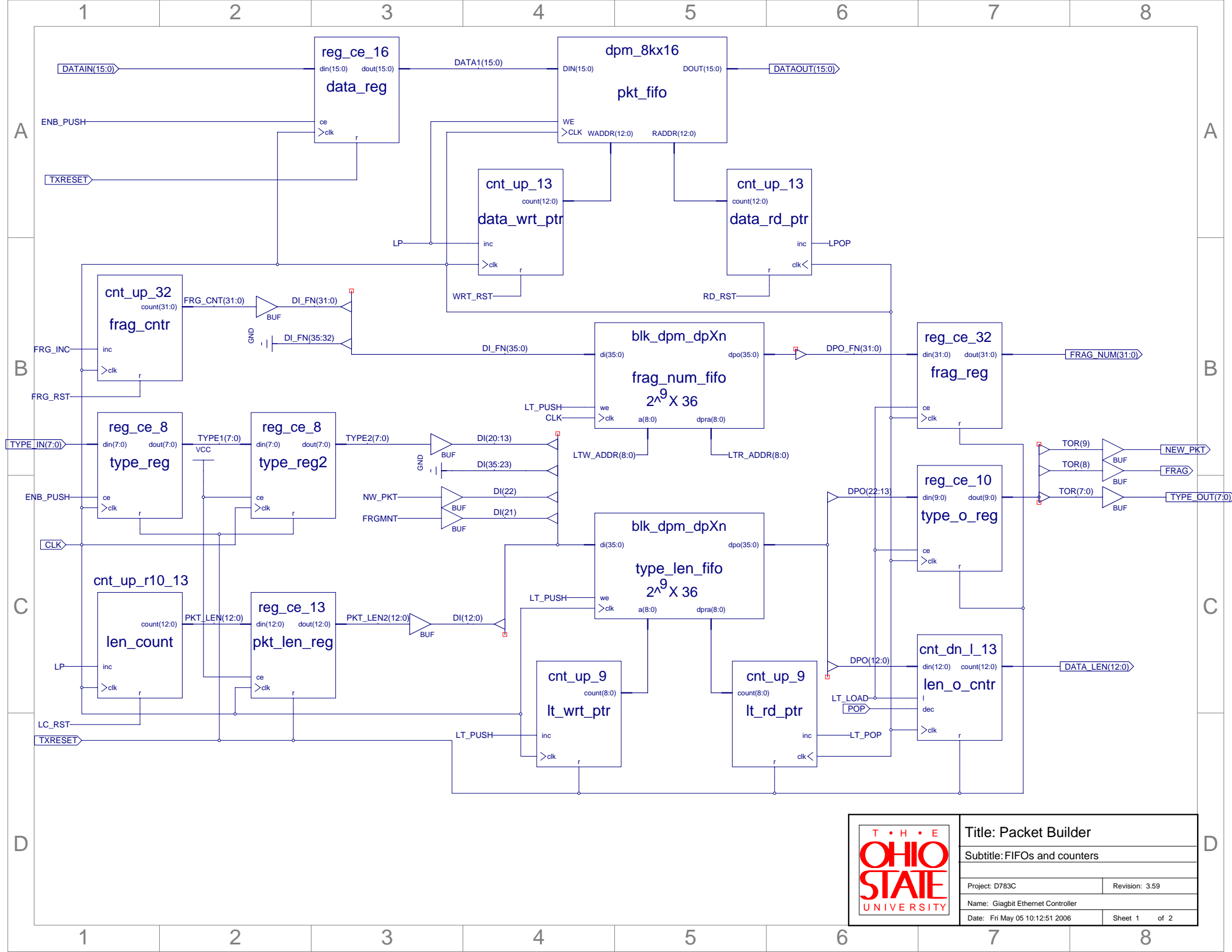
	<b>Title: Ethernet</b>	
	Subtitle: Logic Analyzer	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:13:02 2006	Sheet 3 of 3	



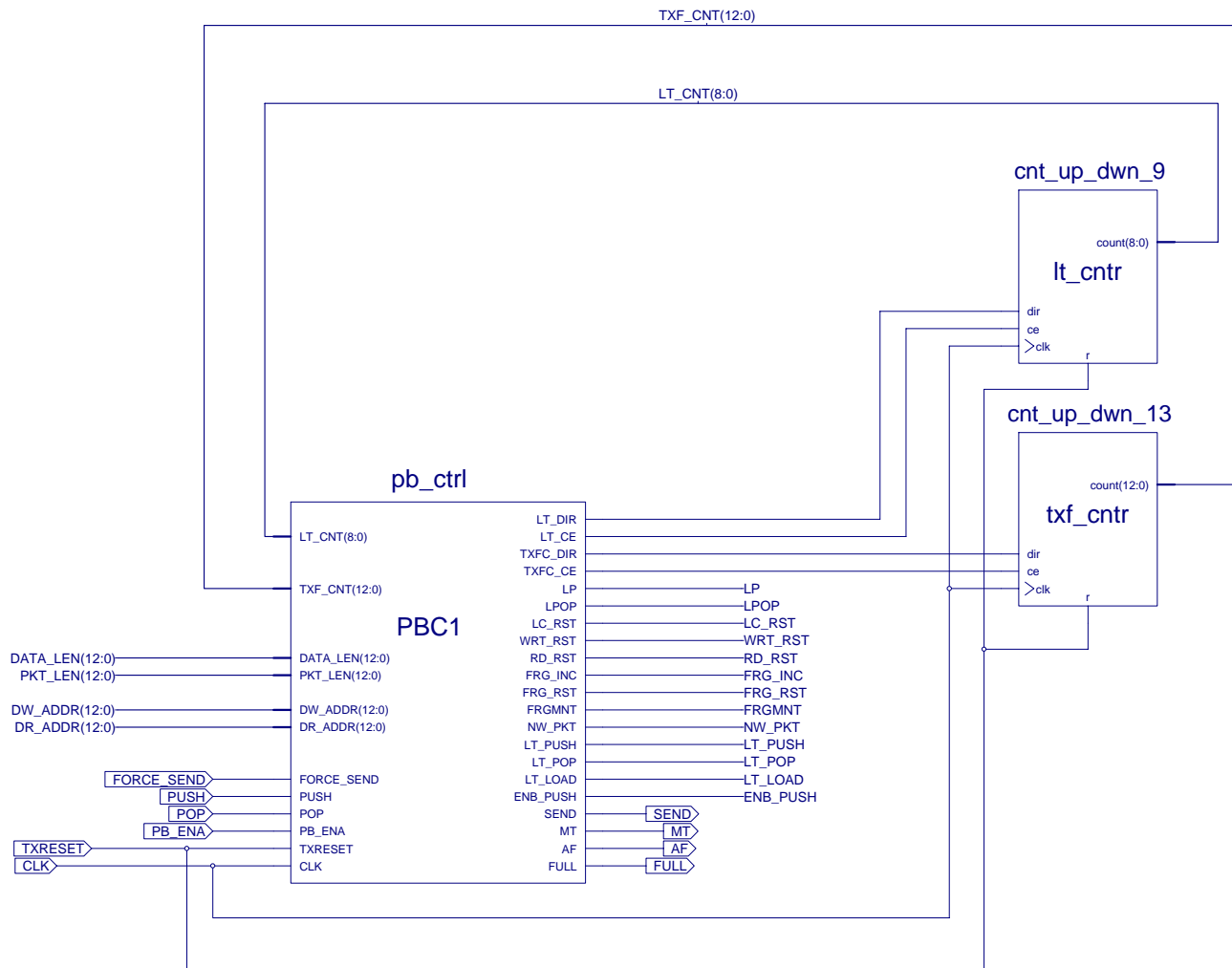
	<b>Title: Packet Receiver FIFO</b>	
	Subtitle: FIFOs and counters	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:12:15 2006	Sheet 1	of 2



<b>Title: Packet Receiver FIFO</b>	
Subtitle: FIFO Controller	
Project: D783C	Revision: 3.59
Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:12:15 2006	Sheet 2 of 2

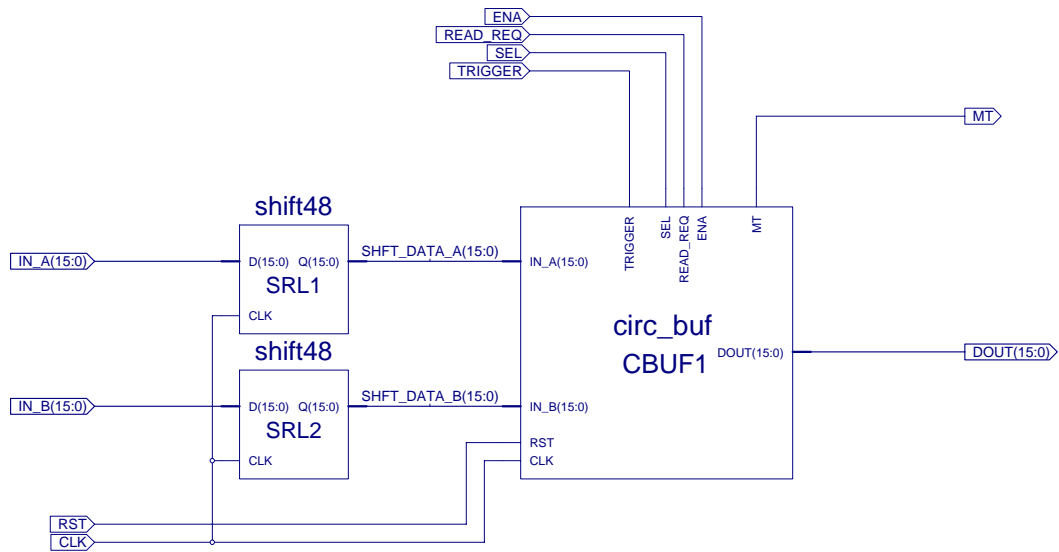



<b>Title: Packet Builder</b>	
Subtitle: FIFOs and counters	
Project: D783C	Revision: 3.59
Name: Giagbit Ethernet Controller	
Date: Fri May 05 10:12:51 2006	Sheet 1 of 2

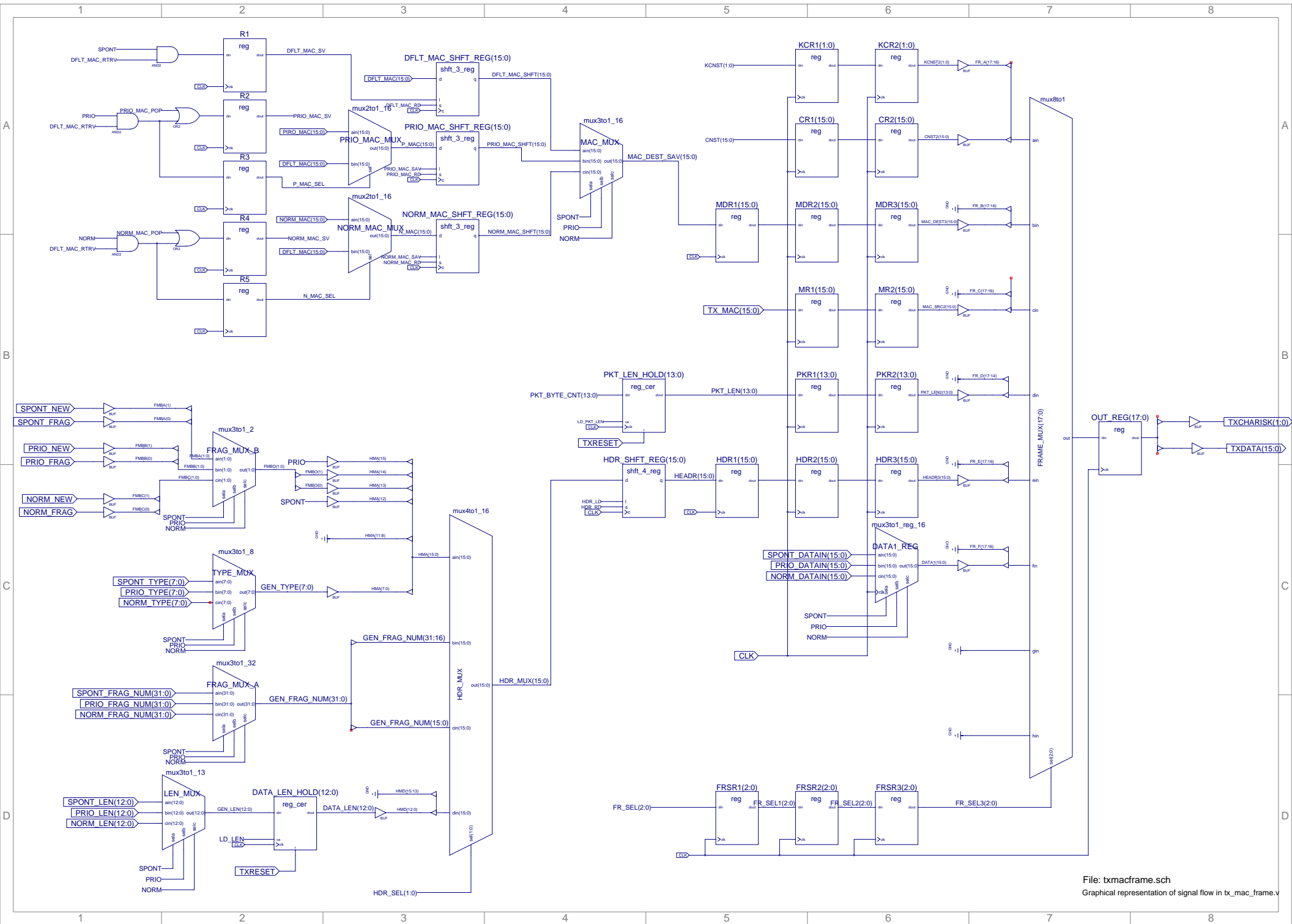


	<b>Title: Packet Builder</b>	
	Subtitle: FIFO controller	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet Controller	
	Date: Fri May 05 10:12:51 2006	Sheet 2 of 2

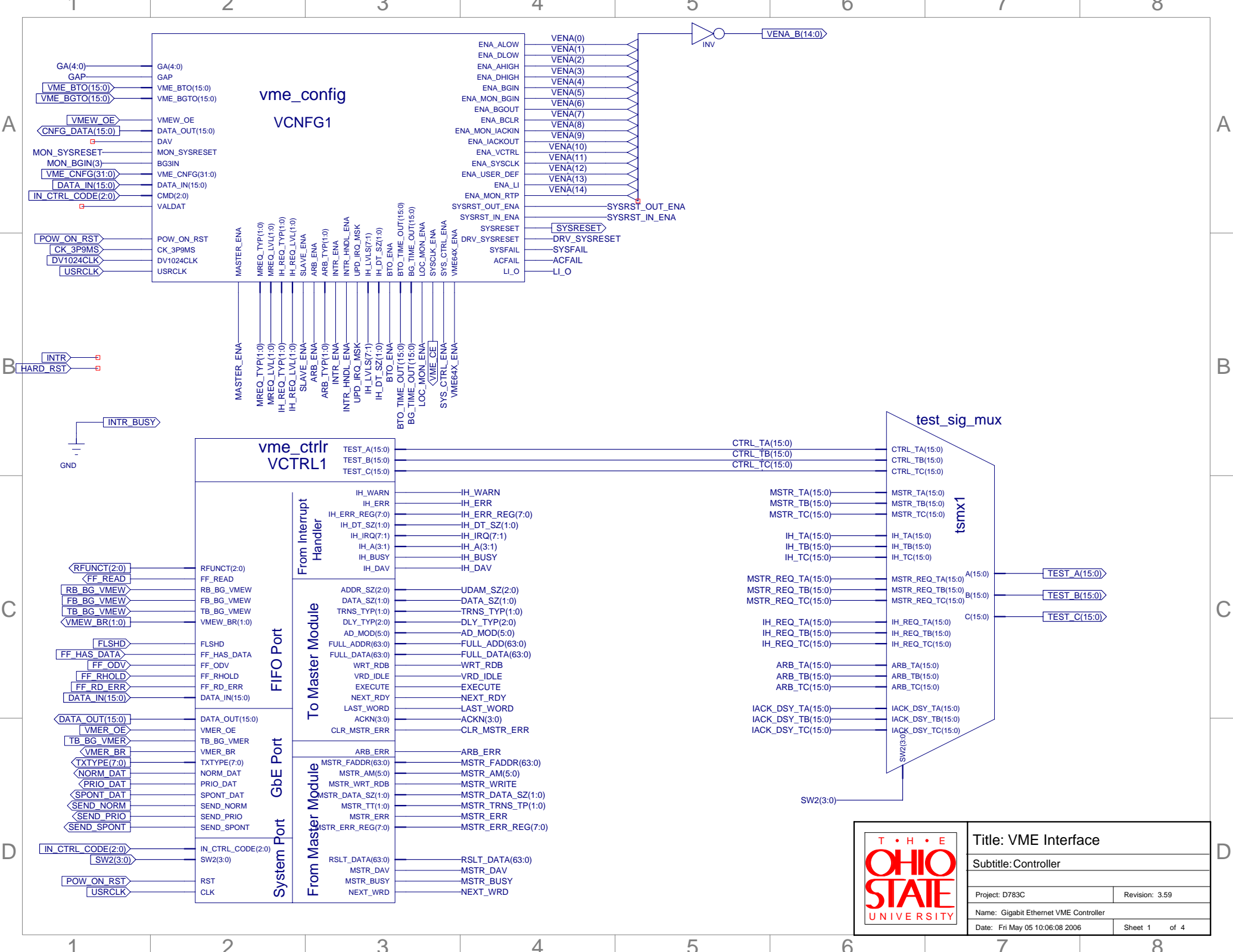




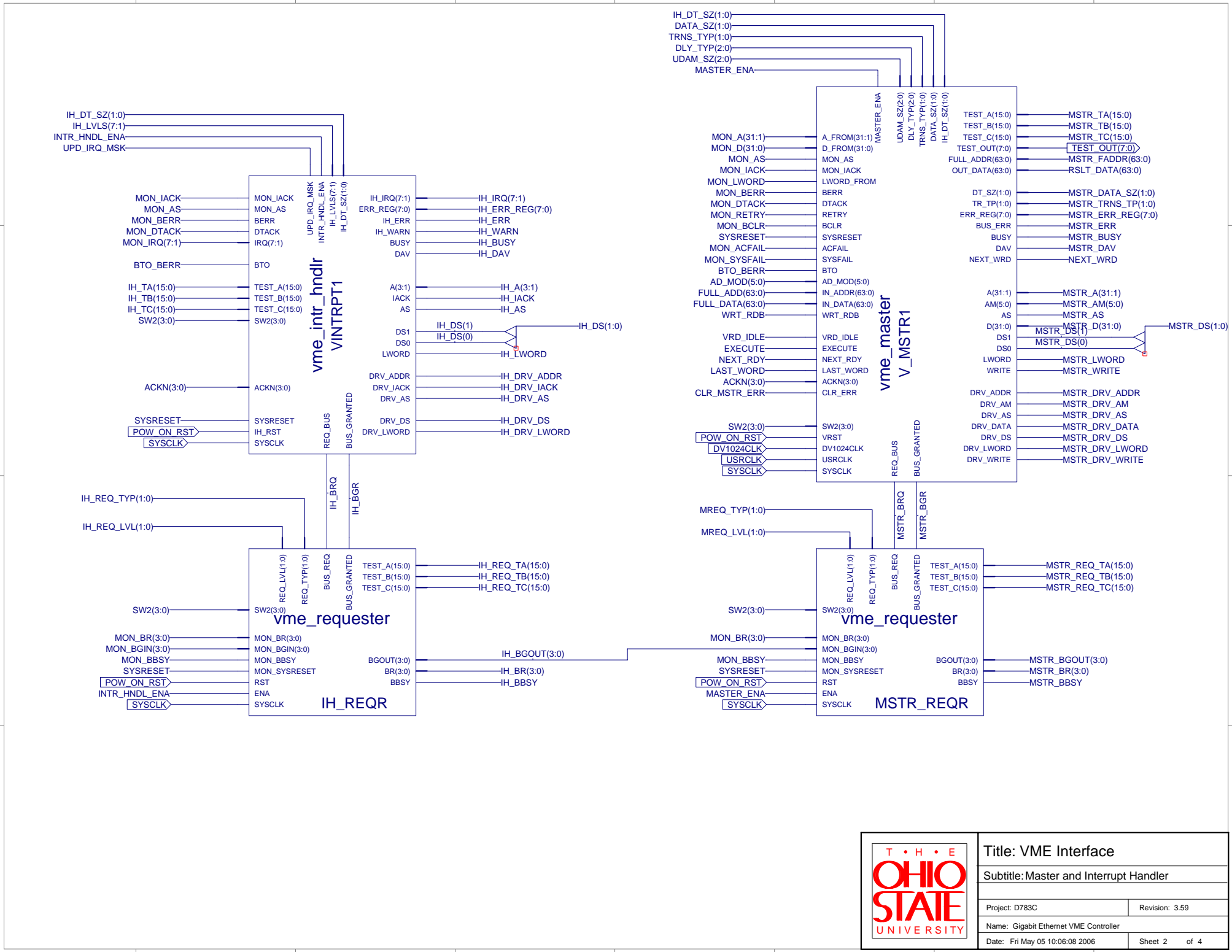
	<b>Title: Logic Analyzer</b>	
	Subtitle: Circular Buffer	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:12:56 2006	Sheet 1	of 1



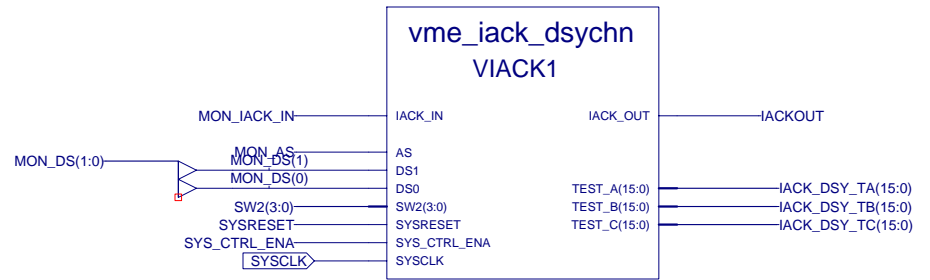
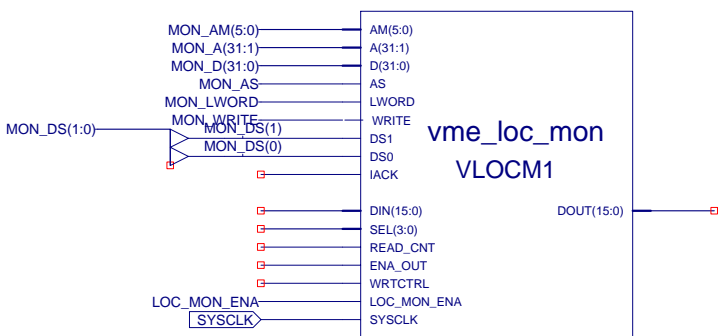
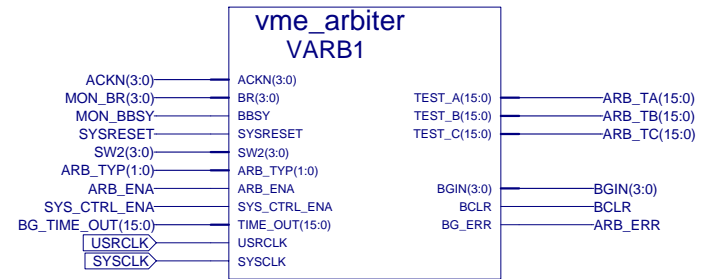
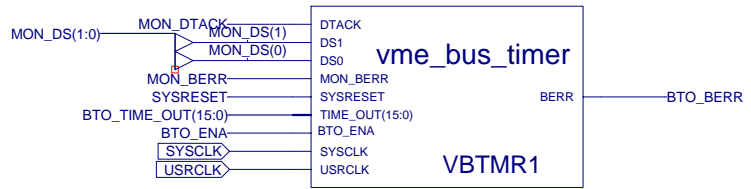
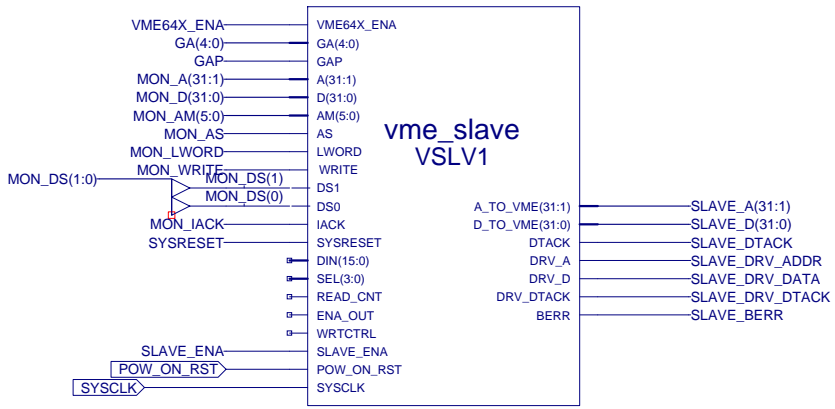
File: txmacframe.sch  
 Graphical representation of signal flow in tx\_mac\_frame.v



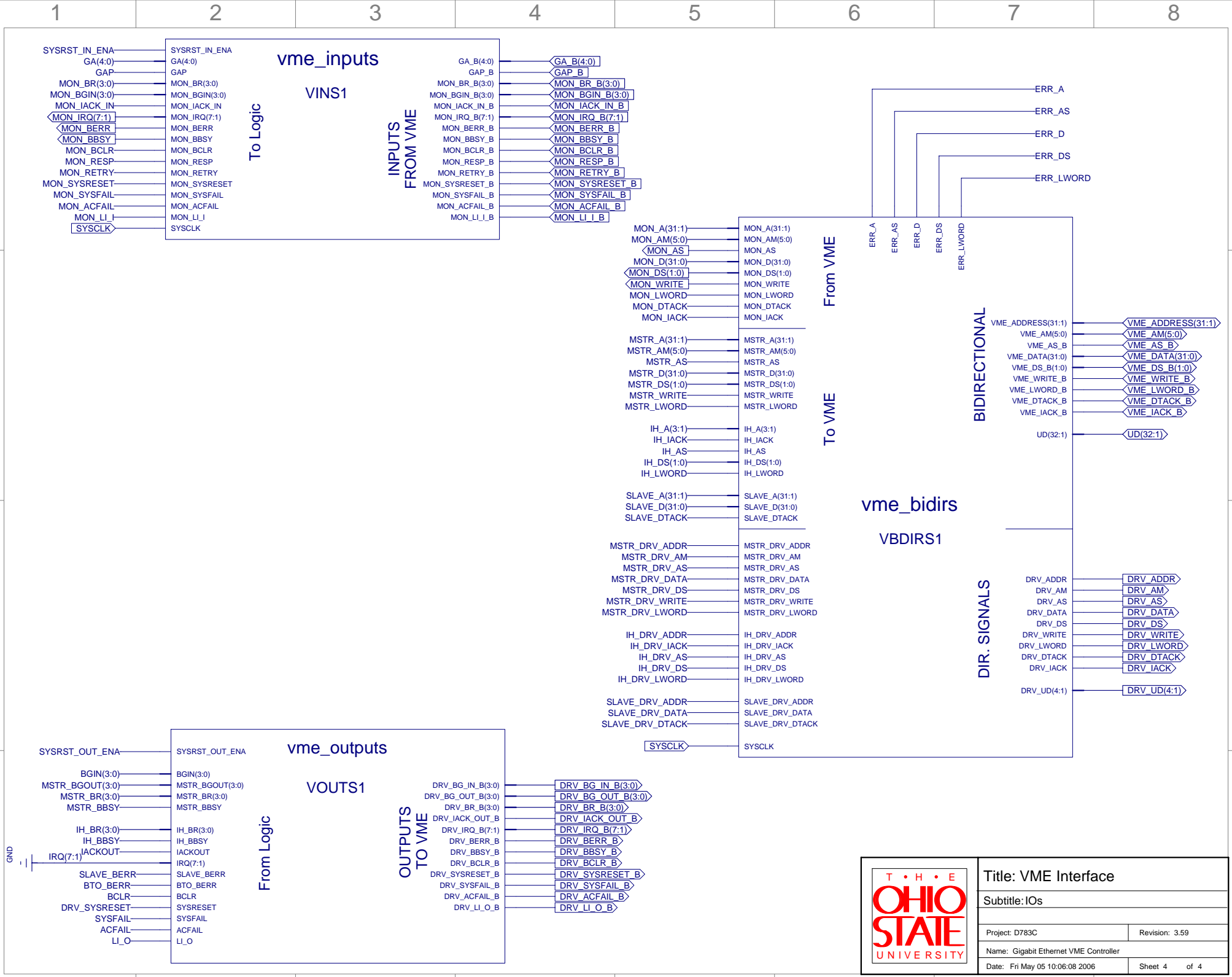
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	Subtitle: Controller	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:06:08 2006	Sheet 1	of 4



<b>Title: VME Interface</b>	
Subtitle: Master and Interrupt Handler	
Project: D783C	Revision: 3.59
Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:06:08 2006	Sheet 2 of 4



	<b>Title: VME Interface</b>	
	Subtitle: Slave, Arbiter, Bus Timer, and Misc.	
	Project: D783C	Revision: 3.59
	Name: Gigabit Ethernet VME Controller	
Date: Fri May 05 10:06:08 2006	Sheet 3	of 4



<b>Title:</b> VME Interface	
<b>Subtitle:</b> IOs	
<b>Project:</b> D783C	<b>Revision:</b> 3.59
<b>Name:</b> Gigabit Ethernet VME Controller	
<b>Date:</b> Fri May 05 10:06:08 2006	<b>Sheet 4</b> of 4