Cathode Preamp-Shaper (Buckeye) ASIC

Amplifier Noise Requirement

For the CMS endcap chambers, the cathode strips are in the radial direction and they provide the measurement of the bending (azimuthal) coordinate. This measurement relies on the interpolation of charges induced by the avalanche process on several (4-5) neighboring cathode strips (hereafter referred to as a cluster). The resulting position resolution is proportional to the percentage error of the cluster charge measurement. For chambers with strip width equal to the gas gap (twice the anode to cathode distance), this resolution is approximately equal to $w\Delta(Q)/Q$, where w is the strip width, Q and $\Delta(Q)$ are the total cluster charge and it's error. For a cluster with N strips, $\Delta(Q)= \delta(q)\sqrt{N}$, where $\delta(q)$ is the noise of each strip channel. In the absence of RF pickup noise, $\delta(q)$ is dominated by the electronics noise of the FET in the preamp.

To achieve the required per layer resolution of 150 μm for ME1/2 (<w>=0.5cm) and 300 μm for rest of the endcap chambers (<w>=1.0 cm), the total cathode charge must be measured with an accuracy of <3%. The design goal is to achieve 1% in $\delta(q)/Q$ for the entire endcap muon system. This calls for a state of the art low noise amplifier.

The input signal corresponding to a normally incident minimum ionizing particle (at the Landau peak) is about $7x10^6$ electrons, or 112 fC with the chamber operating with a gas gain of 10^5. The intrinsic noise for the preamp-shaper depends primarily on three parameters: the input (strip) capacitance, the size (width and length) of the preamp FET and the shaper peaking time. Anticipating the high rate environment at the LHC, the shaper peaking time is chosen to be 100 ns for fast recovery and for good two-pulse time resolution. These considerations together with practical choices for the FET size lead to the requirement that the rms equivalent input noise be on the order of 25 e/pF or less.

Design Specifications of Cathode Amplifier/Shaper ASIC

- Equivalent Input Noise (rms): <25 e/pF
- Shaper Peaking Time: 100 ns
- Peaking Time of Shaped Chamber Pulse: 170ns
- Shaped Waveform: 5 pole semi-Gaussian w/ tail cancellation
- Preamp-Shaper Gain: 0.9 mV/fC
- Non-Linearity: < 1% 0 - 1.5 volt
- Two Track Time Resolution: 125 ns

Description of ASIC Design

The Buckeye ASIC was designed using the AMI foundry 0.8 micron CMOS technology with linear capacitors. Shown below is a schematic diagram of the amplifier/shaper.

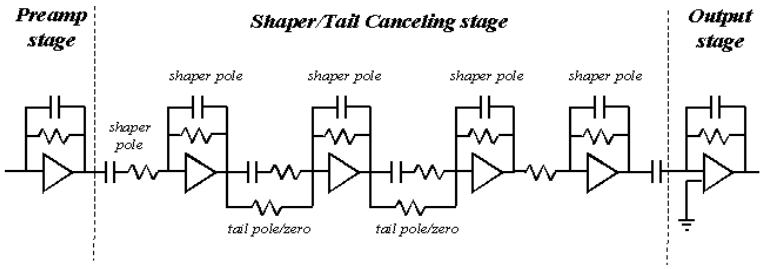


Figure 1. Schematics of Cathode Preamp/Shaper Amplifier

Paramount in the amplifier design was the consideration of the high background rates at the LHC. The major background is photons that deposit on average 2.5 times minimum ionizing charge in the chambers. Singles rates can be as high as ~100 KHz/strip at design luminosities. We thus chose the pole in the preamp (integration) stage to have a decay time of 1 μs. The first pole-zero in the shaper is used to cancel out this integration pole. The rest of the shaping consists of a 5 pole semi-gaussian shaper with a single pole-zero used to cancel the long tail (1/(t + 1.5 ns)) of the induced charge on the cathode strips. In addition the amplifier is AC-coupled to the cathode strips, further reducing the charge seen by the first preamp (integration) stage. The resulting amplifier can handle a continuous rate of 3 MHz photon background with no pulse distortion.

Built into the Cathode preamp shaper ASIC are various calibration functions. As shown in the figure below, an internal shift register attached to each of the 16 amplifiers controls connections to external calibration signals. External capacitors on the CFEB (10 pF, < 1% precision) allow precision calibration of each capacitor channel. Two internal capacitors (one with twice the capacitance of the other) can be selectively set to yield three separate pulse inputs. These capacitors allow testing of the trigger 1/2 strip primitives (the comparator ASIC). Lastly each of the amplifier channels can be selectively killed by appropriate choice of bits on the shift register input.

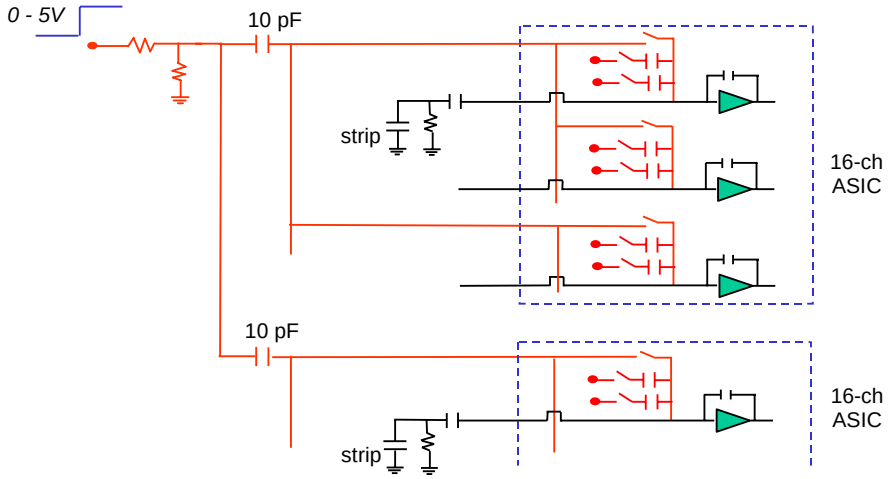
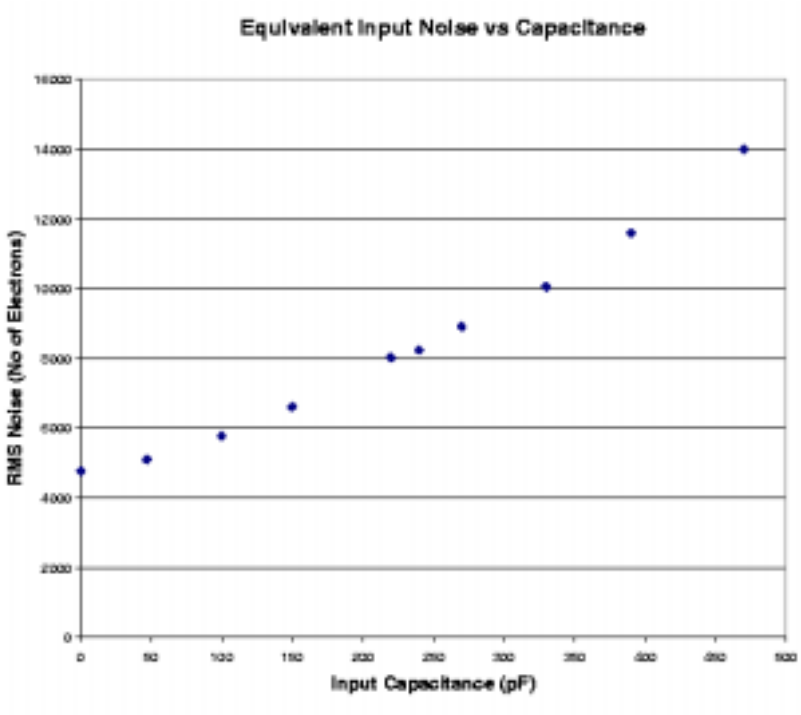


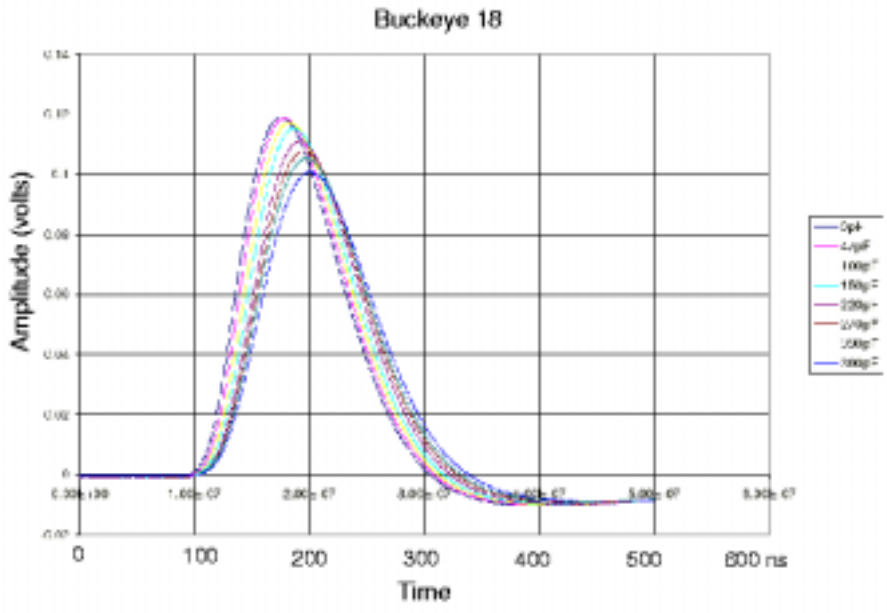
Figure 2. Schematic of Calibration Circuit

Performance Specifications:

- Preamp-Shaper Gain: 0.87 mV/fC
- Gain variation: 2%
- Calibration Precision: 1% over full range
- Equivalent Input Noise (rms): ~ C(inp) x 20 e/pF + 4770 e (see figure below)



- Pulse shape with impulse charge input (see figure below)



- Non-Linearity: < 0.6 %, 0 – 1.7 V (see figure below)