D785U

CMS CSC Data Concentrator Card (DCC) PCB Schematic

Version 4

MBRD_BLK

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

mojo

DCC: It Collects 9 DTB data, and sends to CMS main DAQ via one or two S-LINK64 interfaces

June 9, 2003: Initial drawing, June 23, Need more check
June 26, 2003: Power and ground design
July 28, 2003: Copy the project from cmspc003:\wvdesign\dccp\ to m:\wv\d785\d785g\
July 31, 2003: Added six 100 Ohm resisters for clock termination
Aug. 14, 2003: Add a clock driver MAX9310 for RocketIO reference clock
Apr. 1, 2004: Modifications according to the ver1 tests
Apr. 6, 2004: Main FPGA pin re-assignment, and TTC backplane signal switching
Apr. 7, 2004: Change the hard_reset logic.
June 15, 2005: Re-arrange the CMS_CLK, and L1A distribution,using 74fct20807 buffer
July 9, 2004: Final check on the schematics, tie FIFO TRST LOW
Jan. 28, 2005: replace the IDT72T40118 with IDT72V36110, start rev3 DCC
Feb. 2, 2005: removed the Program data line LEDs (16 in total)
Feb. 21, 2005: Add buffers for SLINK

Aug. 31, 2005: Added /AS to Emergency Load Logic
Aug. 31, 2005: Changed FMM LED Power from V3PIO to V33P
Aug. 31, 2005: Added thevinin terminator to TCMSCLK
Sept, 6, 2005: Added series LED to V5PRAW Front Panel LED
Sept, 6, 2005: Changed V5PRAW, SLDONE, RXDONE LED current limiting resistor to 330z
Sept, 6, 2005: Added (10) 10uF tantalums to the Analog FPGA 2.5V powers
Sept, 7, 2005: Increased size of P1 Test Port Power Trace
Sept, 7, 2005: Converted all regulator back to the adjustable type (placement and ordering purposes)
Sept, 7, 2005: Added (20) 220nF caps to the input FPGA's
Sept, 7, 2005: Added (7) 220nF caps to the control FPGA

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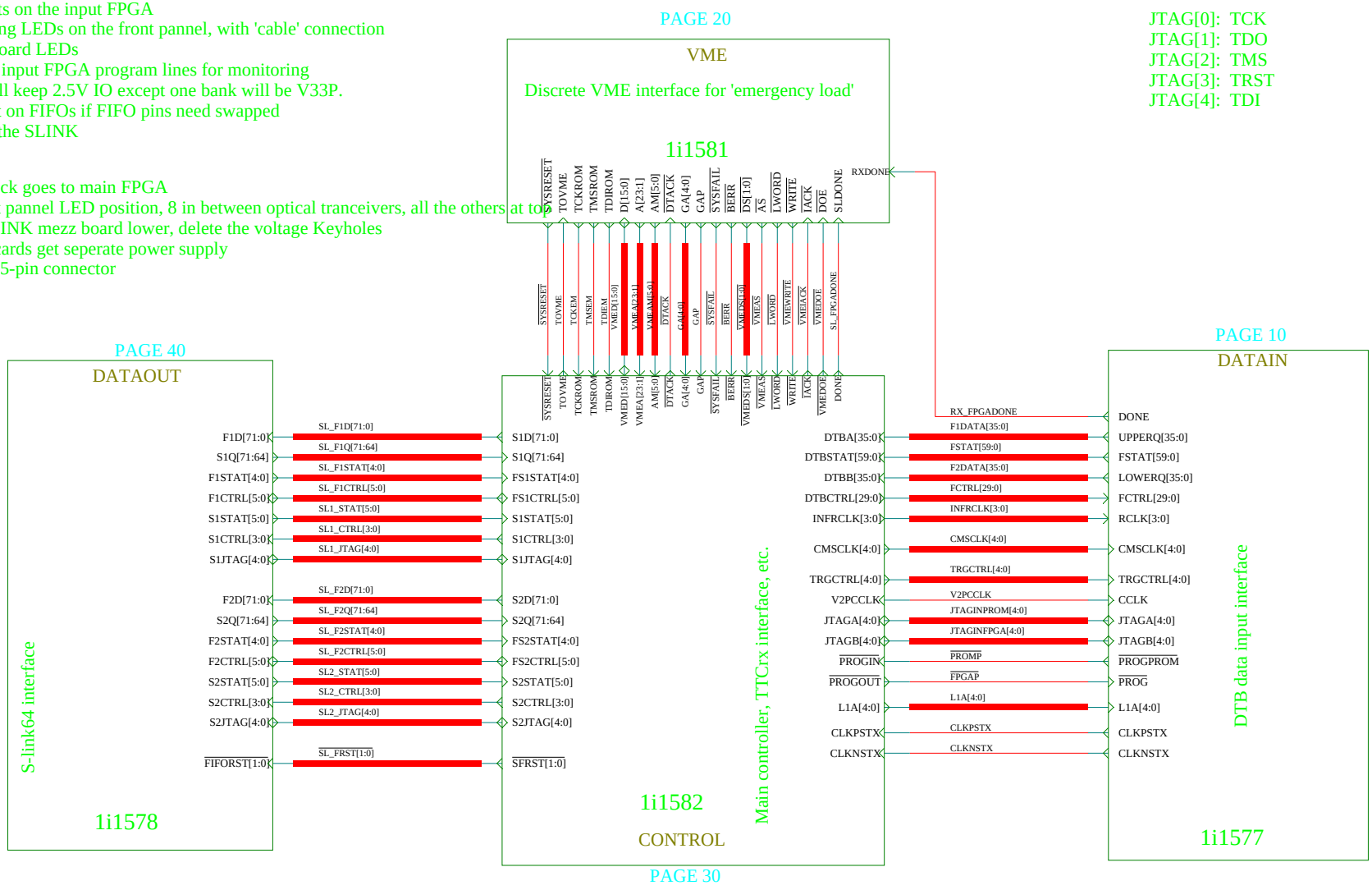
Major changes for rev3:

1. Main FPGA uses V3PIO. 3V compatible IOs
2. Use IDT72V36110 FIFOs, remove the IDT72T40118 fifos
3. Add many test points on the input FPGA
4. Add many monitoring LEDs on the front pannel, with 'cable' connection
5. Remove all the in-board LEDs
6. Add a buffer on the input FPGA program lines for monitoring
7. The input FPGA will keep 2.5V IO except one bank will be V33P.
8. Add some aux point on FIFOs if FIFO pins need swapped
9. Add buffers before the SLINK

Minor changes for rev3:

1. the 156.25MHz clock goes to main FPGA
2. Re-arange the front pannel LED position, 8 in between optical tranceivers, all the others at top
3. Move the upper SLINK mezz board lower, delete the voltage Keyholes
4. The SLINK mezz cards get seperate power supply
5. Add a SLINK Jtag 5-pin connector

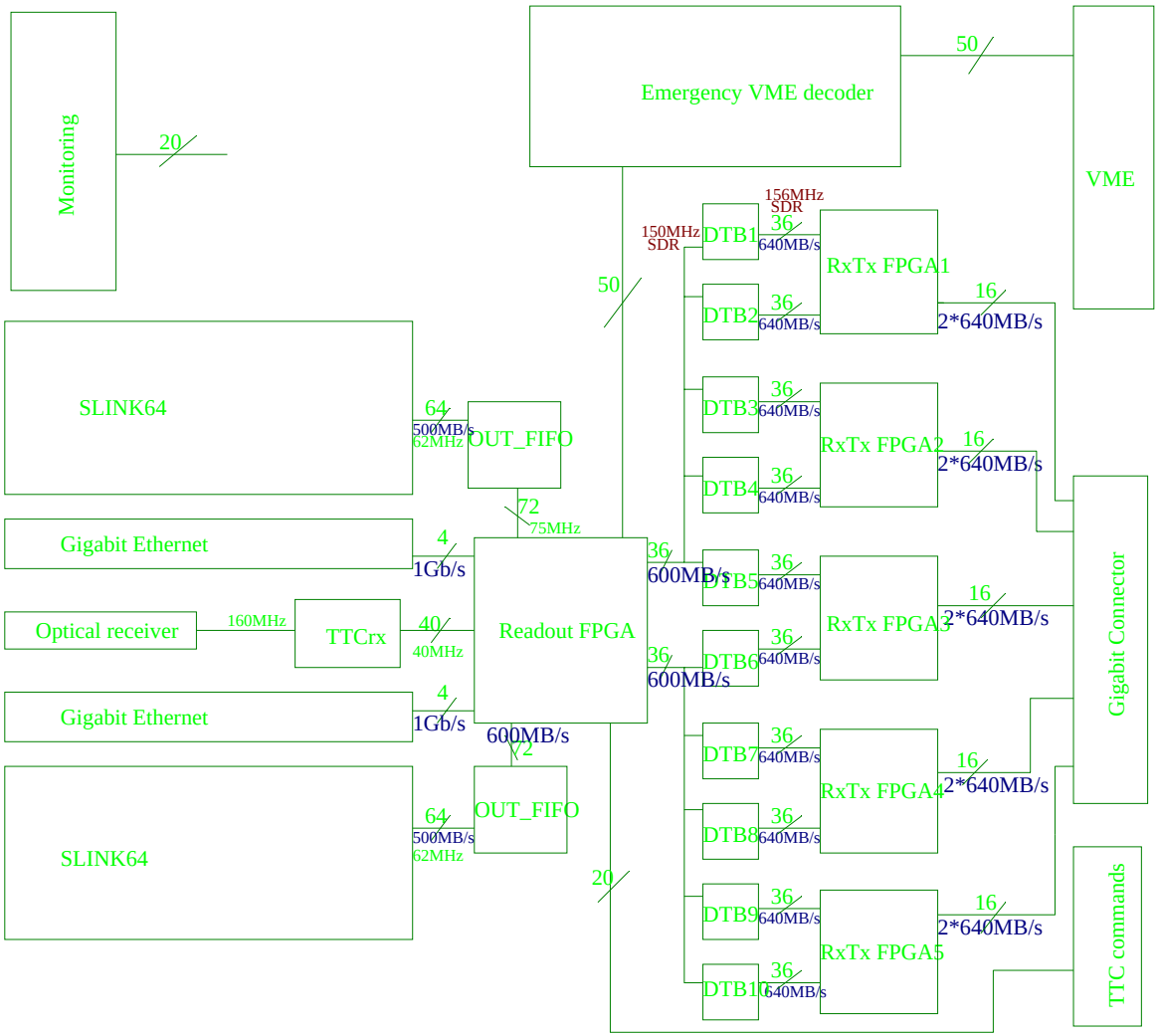
JTAG[0]: TCK
JTAG[1]: TDO
JTAG[2]: TMS
JTAG[3]: TRST
JTAG[4]: TDI



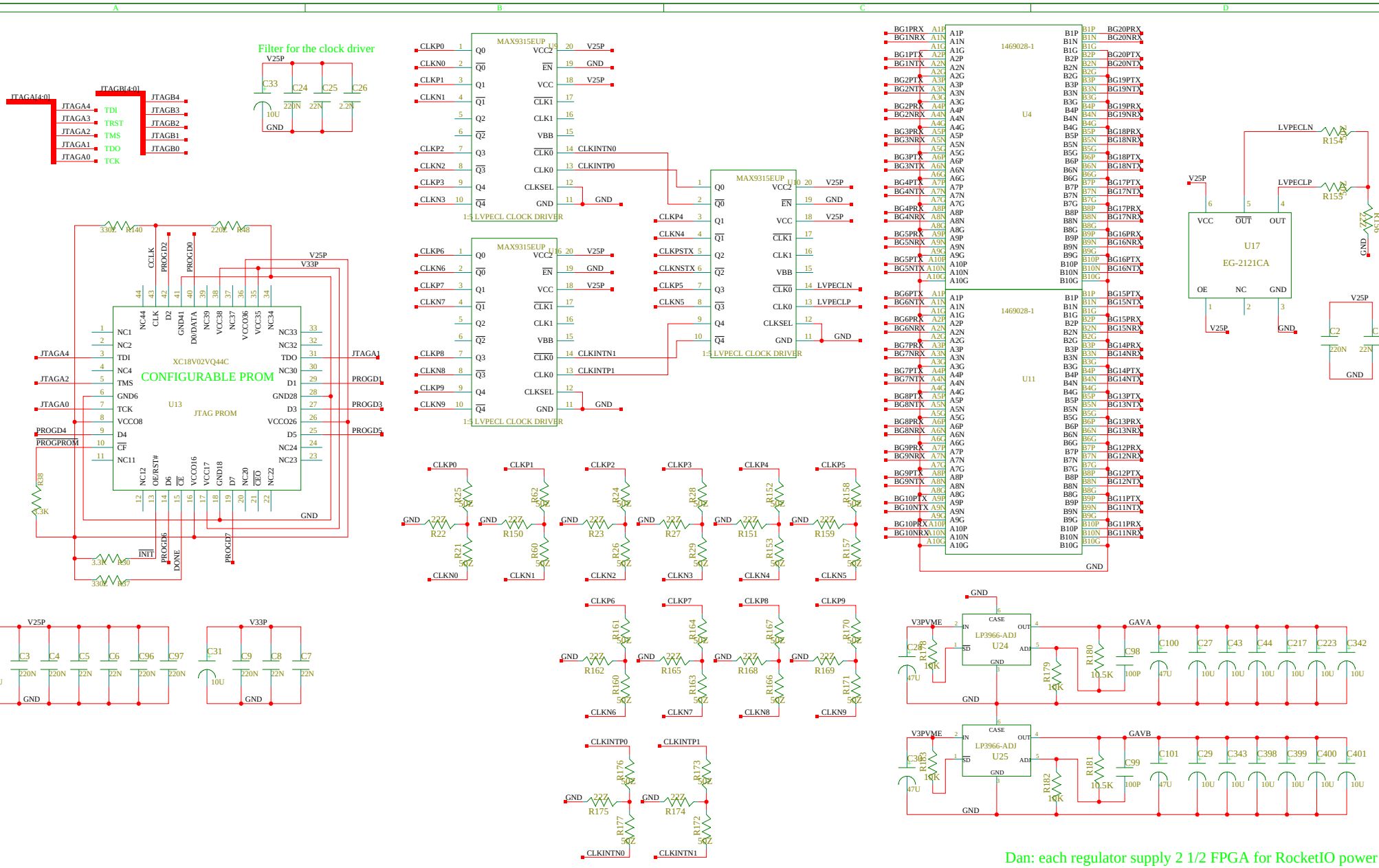
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Top Level Block Diagram CMS CSC Data Concentrator Card CMS CSC ELECTRONICS	BY: GU DATE: 3-17-2006_8:53	PARENT PAGE FILE: BLOCK . 1
		PROJECT: DCC	PAGE: 1

DCC layout and minimum signal required for data flow

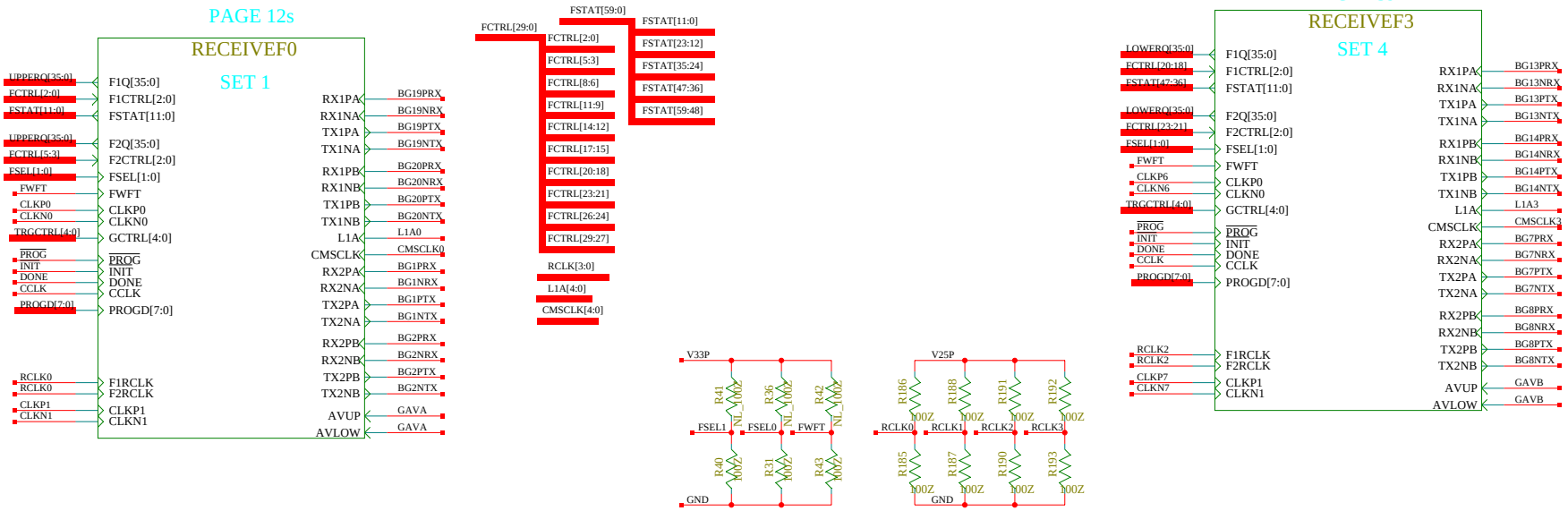
DDDDD D DDDDD DDD D DDD
TTTTT C TTTTT TTT C TTT
BBBBB C BBBBB BBB C BBB



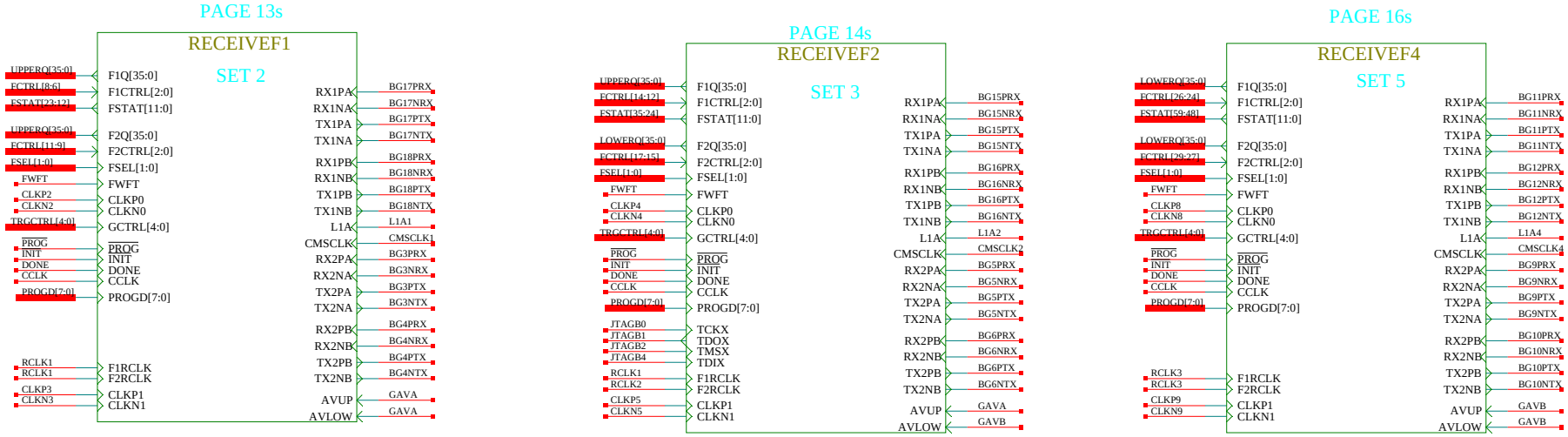
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Top Level Block Diagram CMS CSC Data Concentrator Card CMS CSC ELECTRONICS	BY: GU DATE: 1-31-2005_13:06	PARENT PAGE PROJECT: DCC FILE: BLOCK . 2 PAGE: 1



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: TCB input interface, Higher level CMS CSC DCC CMS CSC ELECTRONICS	BY: GU DATE: 9-22-2005_14:45	PARENT PAGE: 1 FILE: DATAIN . 1	PROJECT: DCC PAGE: 10



Set one bank on the FPGA to 3.3VIO (V3PIO), all the others remain 2.5V



THE OHIO STATE UNIVERSITY
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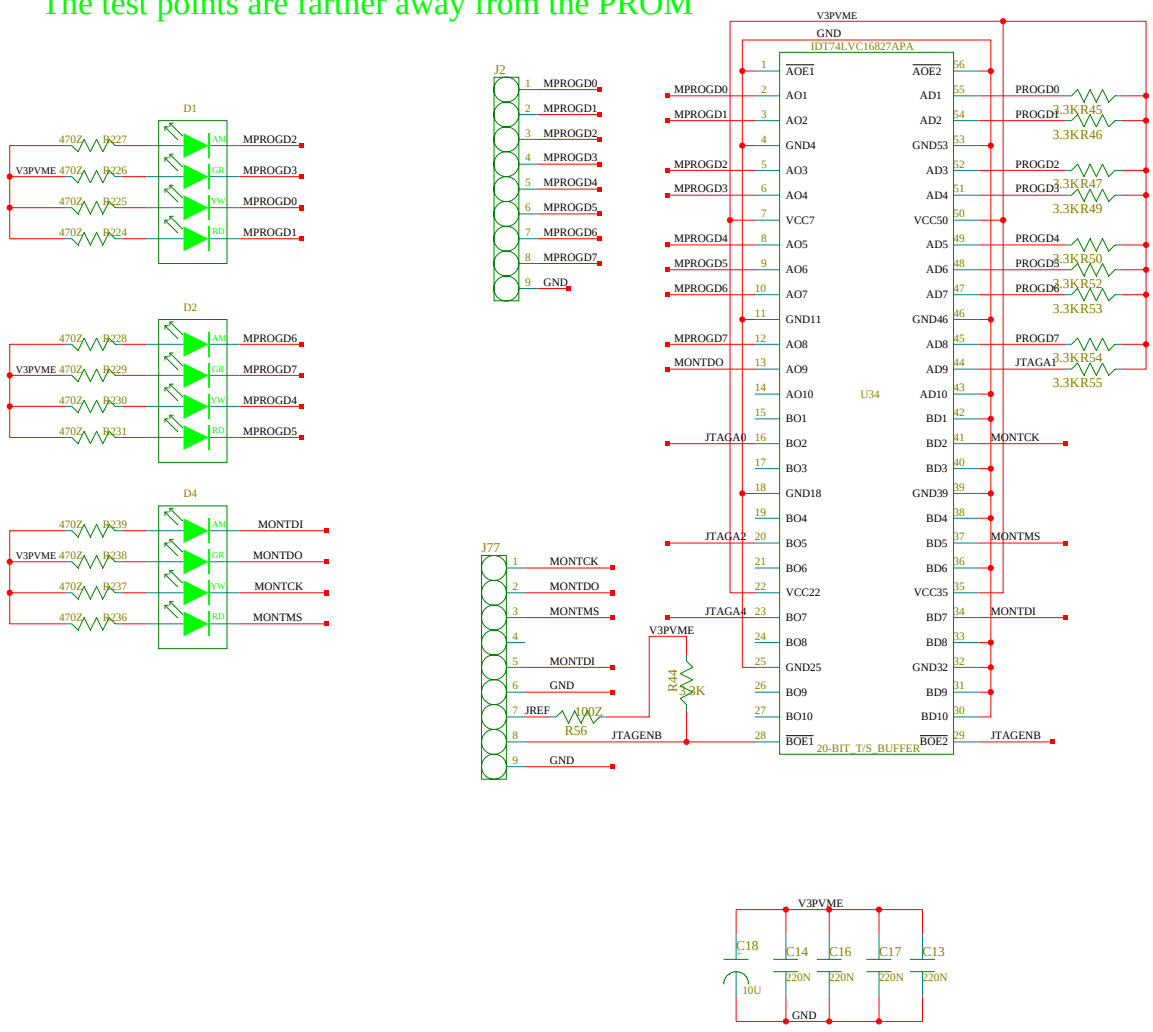
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: TCB input interface, Higher level
CMS CSC DCC
CMS CSC ELECTRONICS

BY: GU
PARENT PAGE: 1
PROJECT: DCC
DATE: 9-8-2005_13:42
FILE: DATAIN . 2
PAGE: 10A

Dan: This is to replace the program LEDs for input FPGAs
The test points are farther away from the PROM



THE OHIO STATE UNIVERSITY
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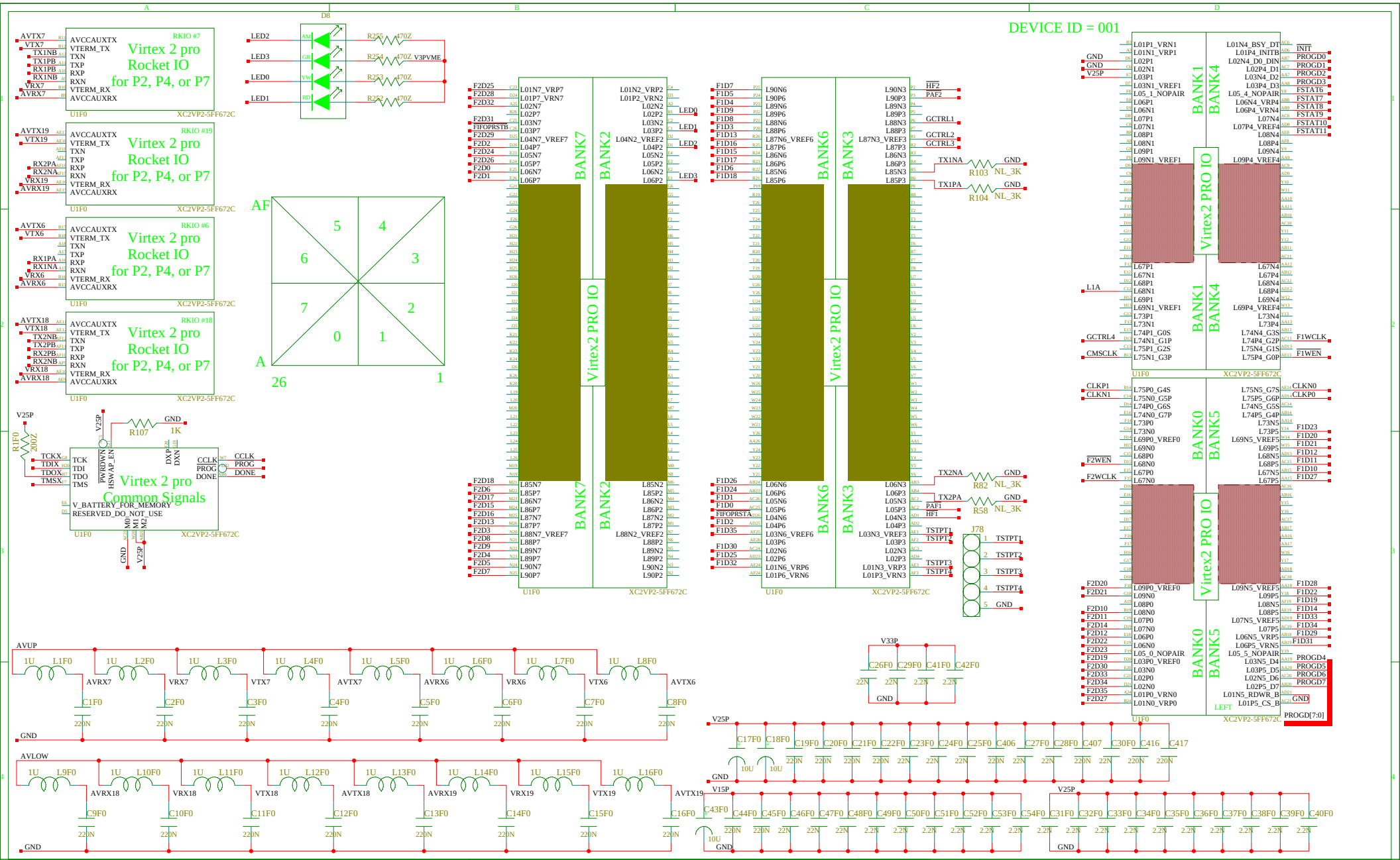
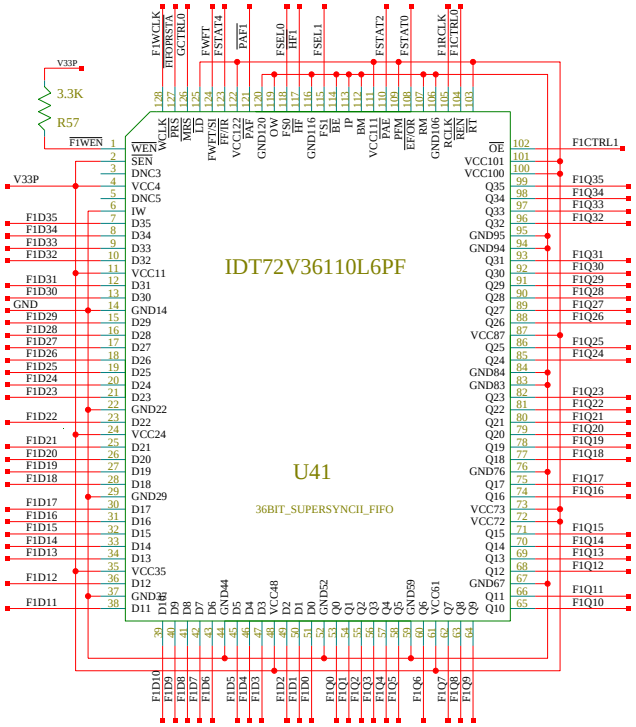
174 WEST 18TH AVE, COLUMBUS OH 43210

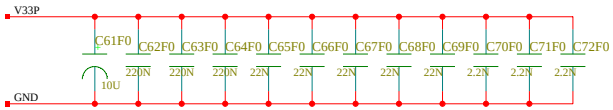
TITLE: Input FPGA monitoring through PROG lines
CMS CSC DCC
CMS CSC ELECTRONICS

BY	PARENT PAGE	PROJECT
GU	1	DCC
DATE	FILE	PAGE
9-8-2005_13:46	DATAIN . 3	10B


DEVICE ID = 001
Virtex 2 pro Rocket IO for P2, P4, or P7
Virtex 2 pro Common Signals
Virtex2 PRO IO
BANK7
BANK2
BANK6
BANK3
BANK1
BANK4
BANK0
BANK5
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TCB input interface, and FPGA power
CMS CSC DCC
CMS CSC ELECTRONICS
GU
1
DCC
11-1-2005_13:44
RECEIVEF0 . 1
12

Fifo Setting
36 bits IN, 36 bits OUT



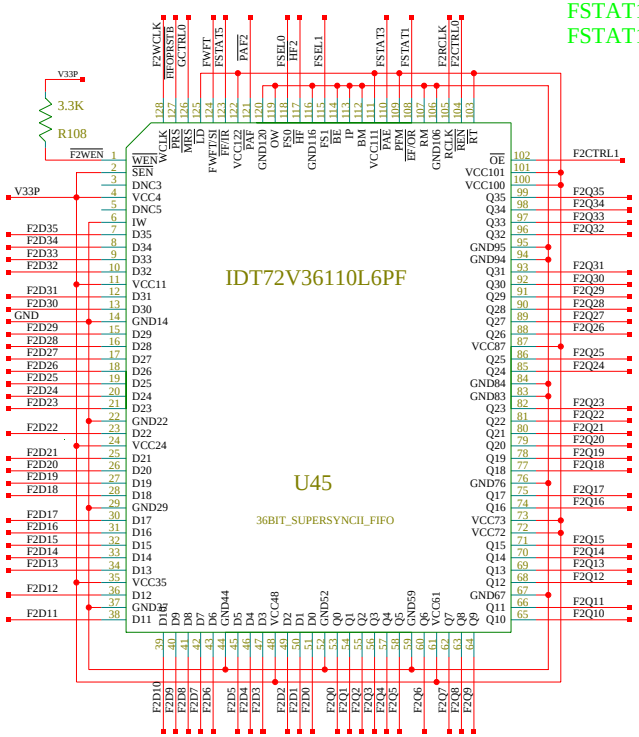


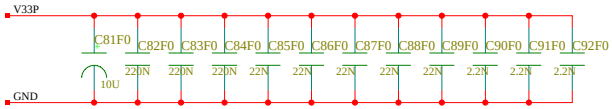
FSTAT[11:0]
GCTRL[4:0]
F1CTRL[2:0]
F2CTRL[2:0]
FSEL[1:0]
F2D[35:0]
F2Q[35:0]
F1D[35:0]
F1Q[35:0]

FnCTRL0: REN~
FnCTRL1: OE~
FnCTRL2: RCS~

GCTRL0: MRST~
GCTRL1: PRST~
GCTRL2: L1A
GCTRL3: RESET
GCTRL4: CMS Clock

FSTAT0: F1 Empty~
FSTAT1: F2 Empty~
FSTAT2: F1 PAE~
FSTAT3: F2 PAE~
FSTAT4: F1 FULL~
FSTAT5: F2 FULL~
FSTAT6: FPGA Status
FSTAT7: FPGA Status
FSTAT8: FPGA Status
FSTAT9: FPGA Status
FSTAT10: FPGA Status
FSTAT11: FPGA Status





THE OHIO STATE UNIVERSITY
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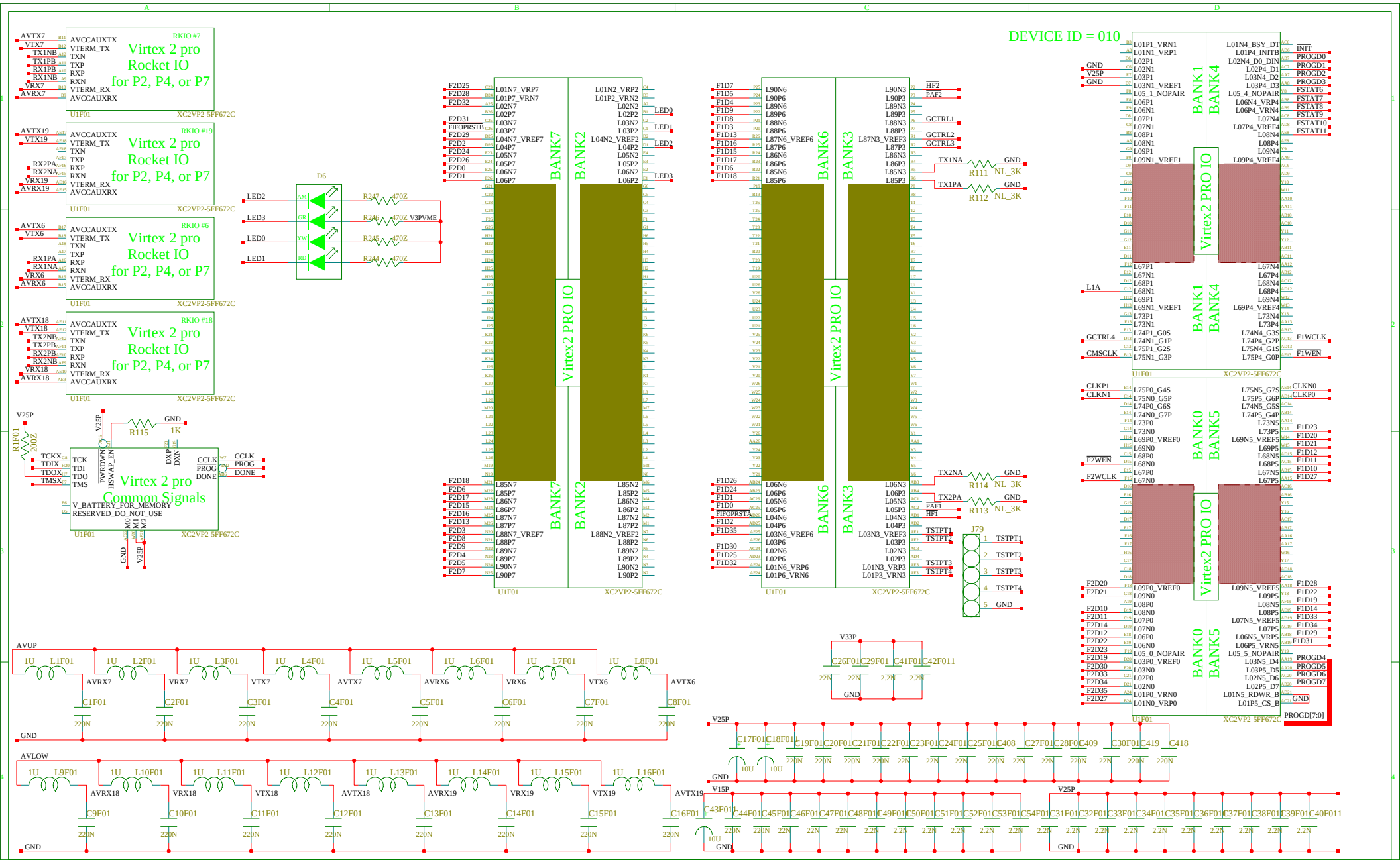
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: FIFO_1 data storage
CMS CSC DCC
CMS CSC ELECTRONICS

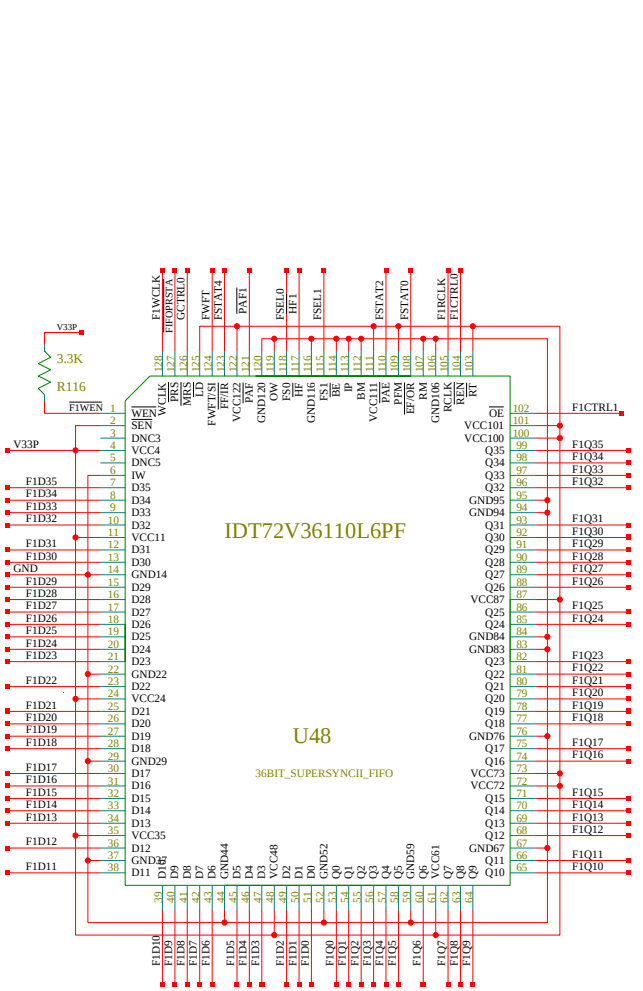
BY: GU
PARENT PAGE: 1
PROJECT: DCC
DATE: 11-1-2005_13:44
FILE: RECEIVEF0 . 2
PAGE: 12A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: TCB input interface, and FPGA power CMS CSC DCC CMS CSC ELECTRONICS	BY: GU DATE: 11-1-2005_13:45	PARENT PAGE: 1 FILE: RECEIVEF1 . 1	PROJECT: DCC PAGE: 13

Fifo Setting

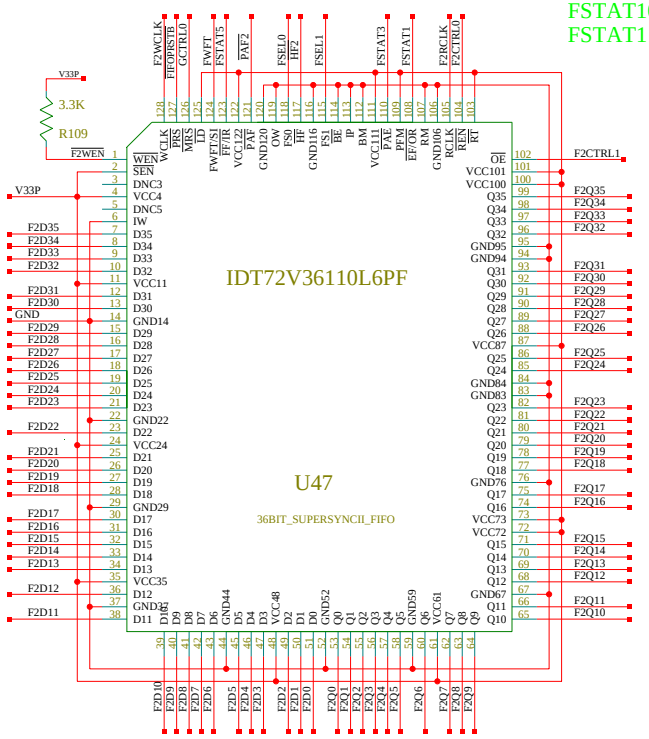
36 bits IN, 36 bits OUT

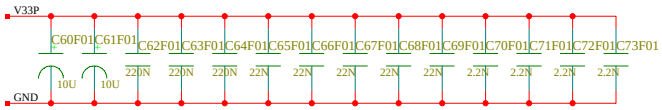


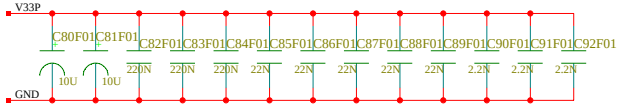
FnCTRL0: REN~
FnCTRL1: OE~
FnCTRL2: RCS~

GCTRL0: MRST~
GCTRL1: PRST~
GCTRL2: L1A
GCTRL3: RESET
GCTRL4: CMS Clock

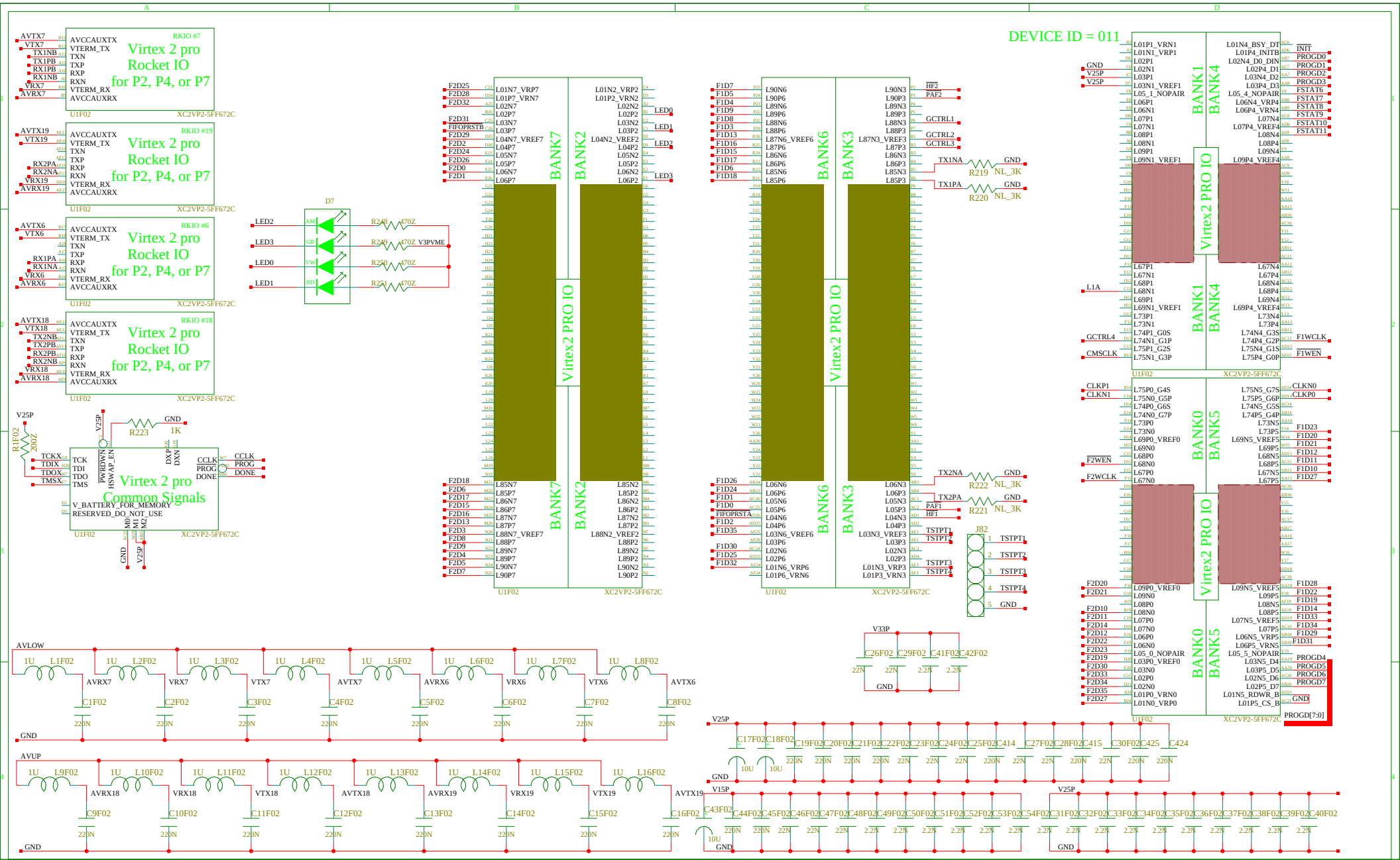
FSTAT0: F1 Empty~
FSTAT1: F2 Empty~
FSTAT2: F1 PAE~
FSTAT3: F2 PAE~
FSTAT4: F1 FULL~
FSTAT5: F2 FULL~
FSTAT6: FPGA Status
FSTAT7: FPGA Status
FSTAT8: FPGA Status
FSTAT9: FPGA Status
FSTAT10: FPGA Status
FSTAT11: FPGA Status







THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: FIFO_1 data storage CMS CSC DCC CMS CSC ELECTRONICS	BY: GU PARENT PAGE: 1 DATE: 11-1-2005_13:45	PROJECT: DCC FILE: RECEIVEF1 . 2 PAGE: 13A


DEVICE ID = 011
Virtex 2 pro Rocket IO for P2, P4, or P7
RKIO #7
RKIO #19
RKIO #6
RKIO #18
U1F02
XC2VP2-5FF672C
Virtex 2 pro Common Signals
TCK
TDI
TDO
TMS
V_BATTERY_FOR_MEMORY
RESERVED_DO_NOT_USE
Virtex2 PRO IO
BANK7
BANK2
BANK6
BANK3
BANK1
BANK4
BANK0
BANK5
D7
LED0
LED1
LED2
LED3
R223 1K
R248 470Z
R249 470Z
R250 470Z
R251 470Z
V3PVME
R219 NL_3K
R220 NL_3K
R221 NL_3K
R222 NL_3K
J82
TSTPT1
TSTPT2
TSTPT3
TSTPT4
GND
V25P
V33P
AVLOW
AVUP
L1F02
L2F02
L3F02
L4F02
L5F02
L6F02
L7F02
L8F02
L9F02
L10F02
L11F02
L12F02
L13F02
L14F02
L15F02
L16F02
C1F02
C2F02
C3F02
C4F02
C5F02
C6F02
C7F02
C8F02
C9F02
C10F02
C11F02
C12F02
C13F02
C14F02
C15F02
C16F02
AVRX7
VRX7
VTX7
AVTX7
AVRX6
VRX6
VTX6
AVTX6
AVRX18
VRX18
VTX18
AVTX18
AVRX19
VRX19
VTX19
AVTX19
220N
1U
10U
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
TCB input interface, and FPGA power
CMS CSC DCC
CMS CSC ELECTRONICS
BY
GU
PARENT PAGE
1
PROJECT
DCC
DATE
11-1-2005_13:46
FILE
RECEIVEF2 . 1
PAGE
14

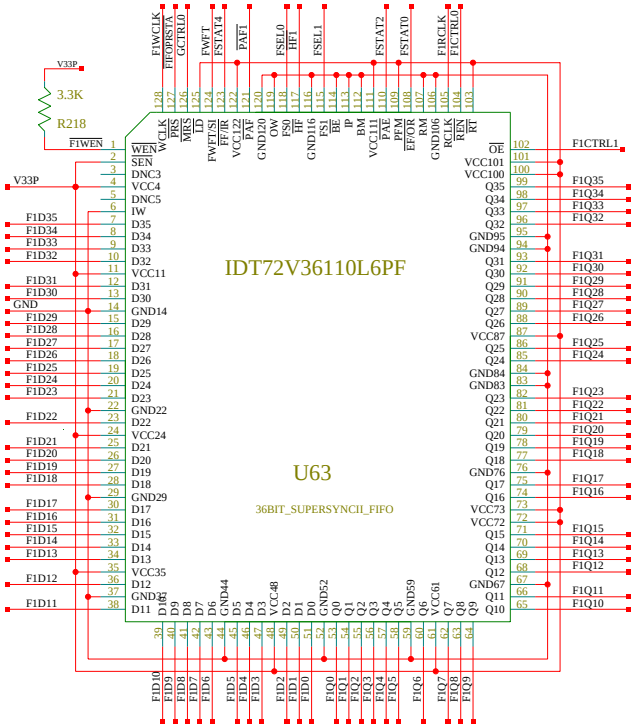
Fifo Setting
36 bits IN, 36 bits OUT

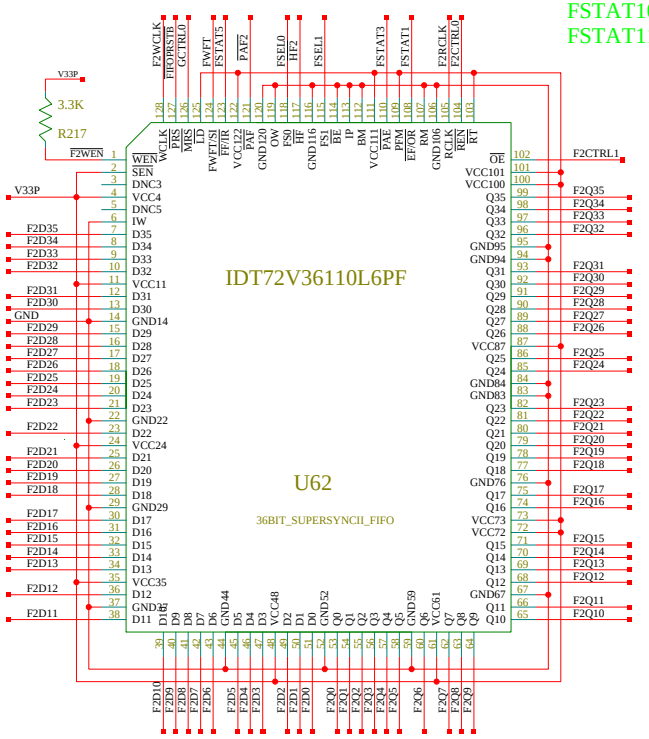
FSTAT[11:0]
GCTRL[4:0]
F1CTRL[2:0]
F2CTRL[2:0]
FSEL[1:0]
F2D[35:0]
F2Q[35:0]
F1D[35:0]
F1Q[35:0]

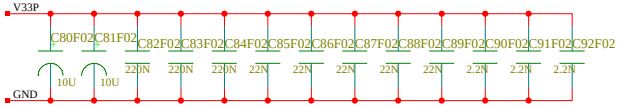
FnCTRL0: REN~
FnCTRL1: OE~
FnCTRL2: RCS~

GCTRL0: MRST~
GCTRL1: PRST~
GCTRL2: L1A
GCTRL3: RESET
GCTRL4: CMS Clock

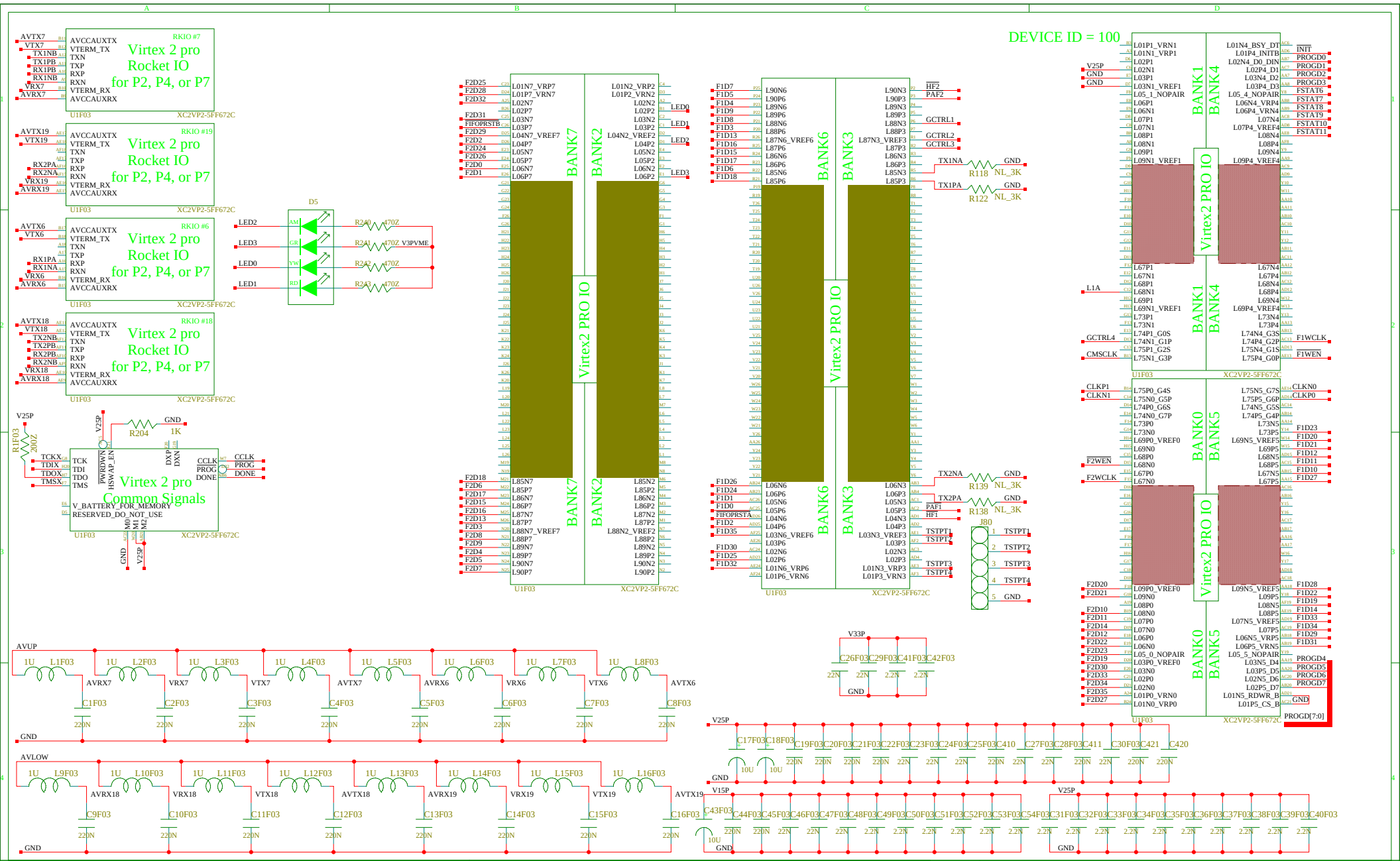
FSTAT0: F1 Empty~
FSTAT1: F2 Empty~
FSTAT2: F1 PAE~
FSTAT3: F2 PAE~
FSTAT4: F1 FULL~
FSTAT5: F2 FULL~
FSTAT6: FPGA Status
FSTAT7: FPGA Status
FSTAT8: FPGA Status
FSTAT9: FPGA Status
FSTAT10: FPGA Status
FSTAT11: FPGA Status







THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: FIFO_1 data storage CMS CSC DCC CMS CSC ELECTRONICS	BY: GU	PARENT PAGE: 1
		DATE: 11-1-2005_13:46	PROJECT: DCC
		FILE: RECEIVEF2 . 2	PAGE: 14A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: TCB input interface, and FPGA power CMS CSC DCC CMS CSC ELECTRONICS	BY: GU DATE: 11-1-2005_13:43	PARENT PAGE: 1 FILE: RECEIVEF3 . 1	PROJECT: DCC PAGE: 15

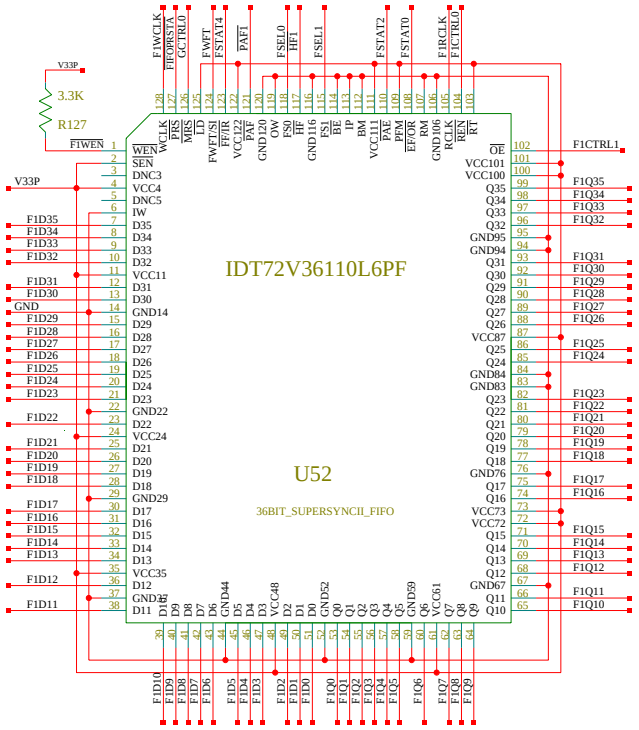
Fifo Setting
36 bits IN, 36 bits OUT

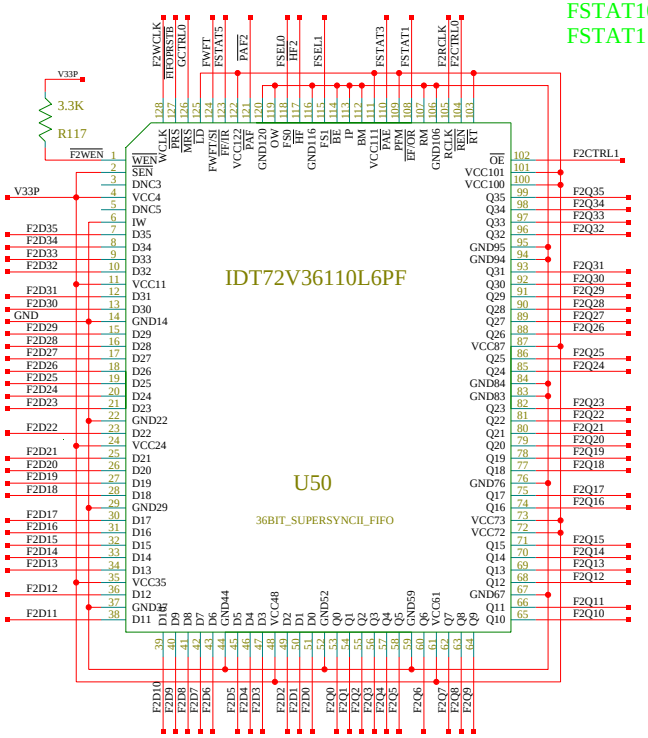
FSTAT[11:0]
GCTRL[4:0]
F1CTRL[2:0]
F2CTRL[2:0]
FSEL[1:0]
F2D[35:0]
F2Q[35:0]
F1D[35:0]
F1Q[35:0]

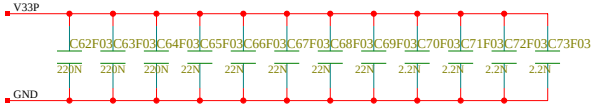
FnCTRL0: REN~
FnCTRL1: OE~
FnCTRL2: RCS~

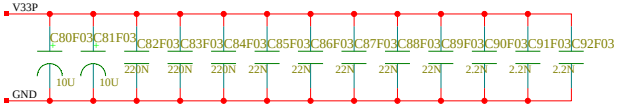
GCTRL0: MRST~
GCTRL1: PRST~
GCTRL2: L1A
GCTRL3: RESET
GCTRL4: CMS Clock

FSTAT0: F1 Empty~
FSTAT1: F2 Empty~
FSTAT2: F1 PAE~
FSTAT3: F2 PAE~
FSTAT4: F1 FULL~
FSTAT5: F2 FULL~
FSTAT6: FPGA Status
FSTAT7: FPGA Status
FSTAT8: FPGA Status
FSTAT9: FPGA Status
FSTAT10: FPGA Status
FSTAT11: FPGA Status

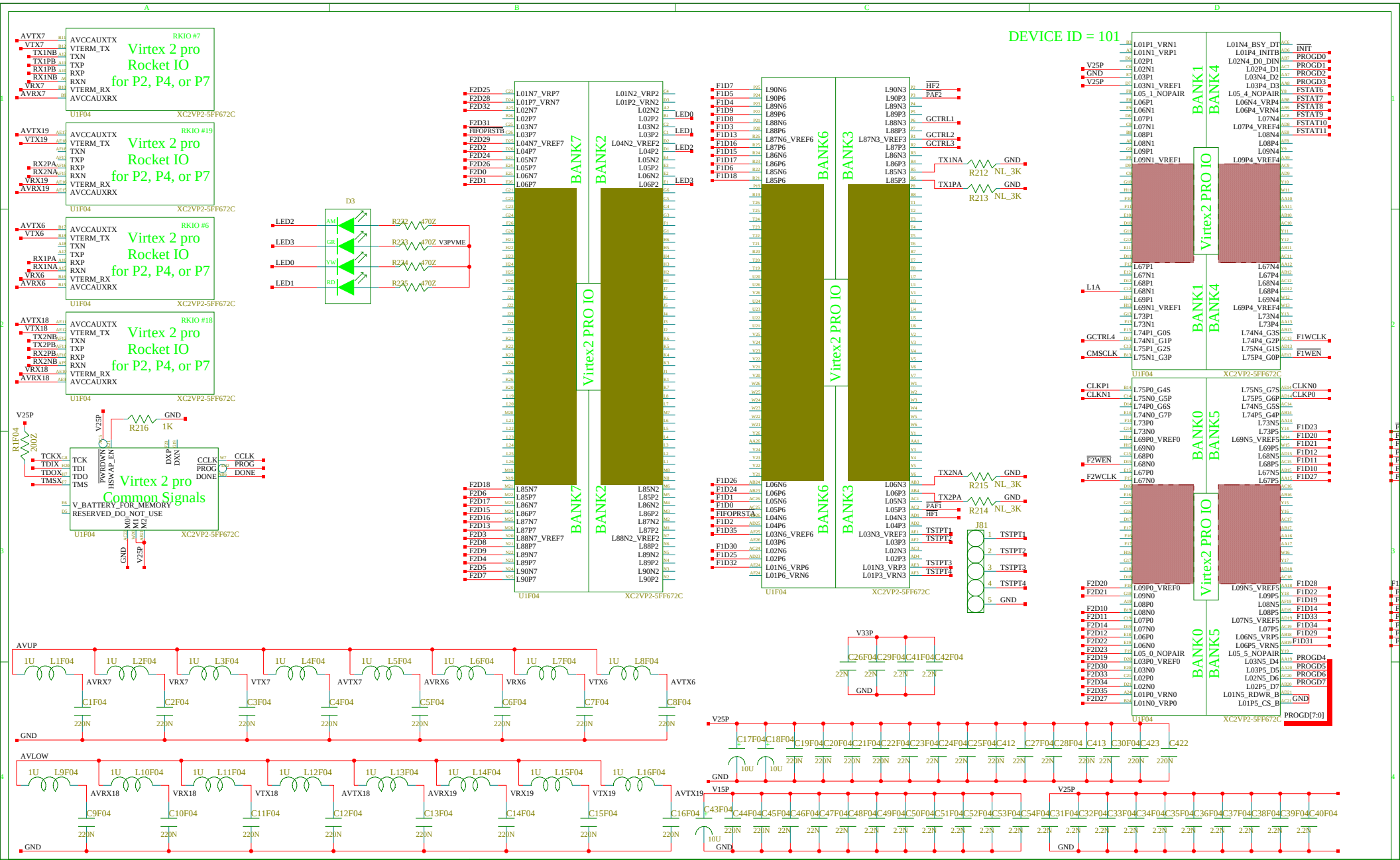






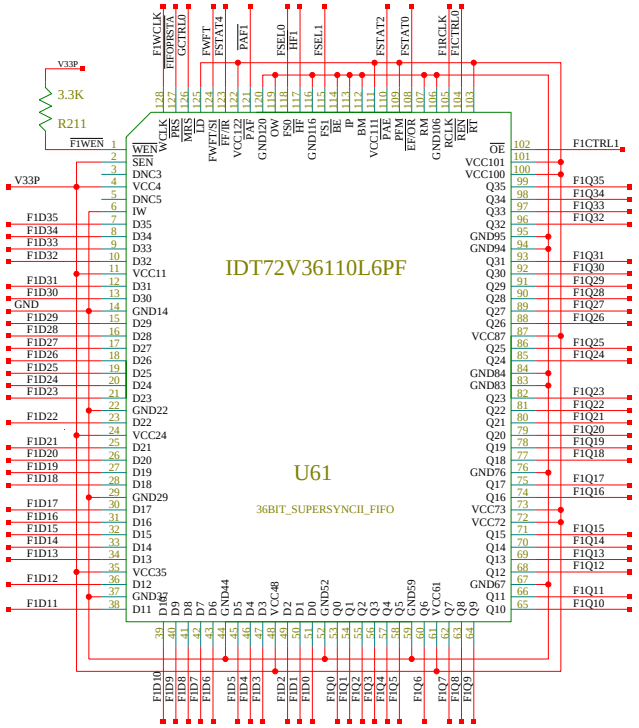


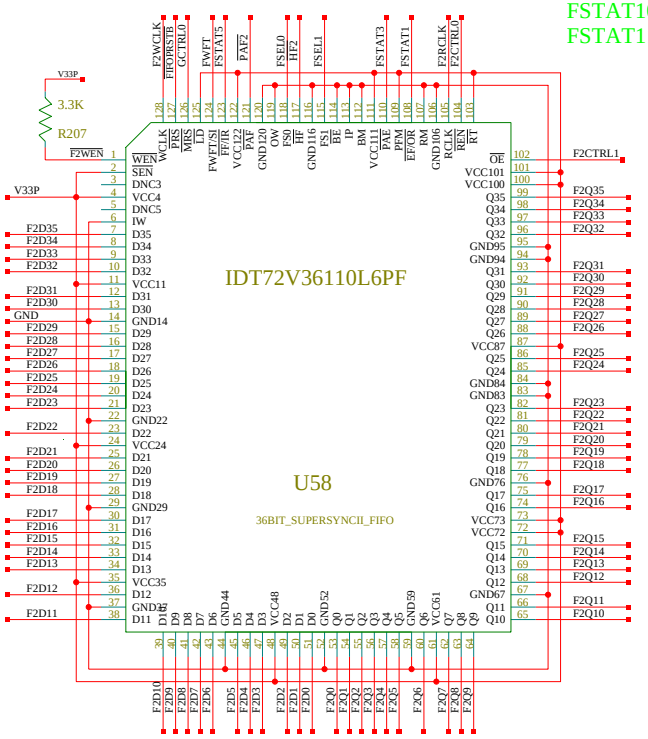
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: FIFO_1 data storage CMS CSC DCC CMS CSC ELECTRONICS	BY: GU	PARENT PAGE: 1
		DATE: 11-1-2005_13:43	PROJECT: DCC
		FILE: RECEIVEF3 . 2	PAGE: 15A

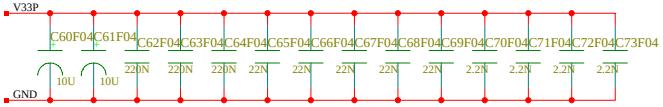


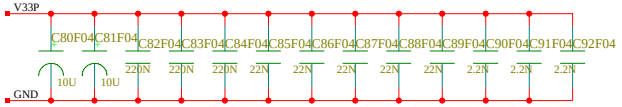
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: TCB input interface, and FPGA power CMS CSC DCC CMS CSC ELECTRONICS	BY: GU DATE: 11-1-2005_13:42	PARENT PAGE: 1 FILE: RECEIVEF4 . 1	PROJECT: DCC PAGE: 16

Fifo Setting
36 bits IN, 36 bits OUT









FnCTRL0: REN~
FnCTRL1: OE~
FnCTRL2: RCS~

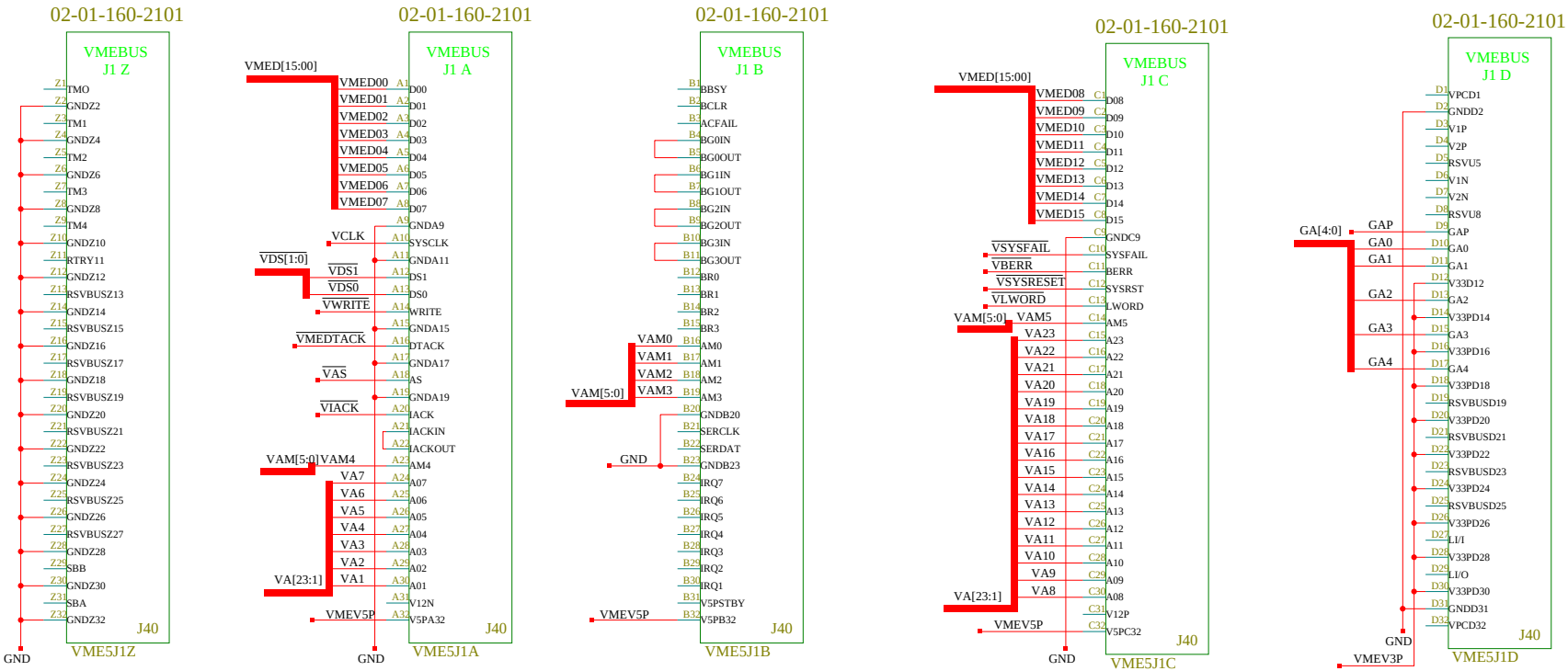
GCTRL0: MRST~
GCTRL1: PRST~
GCTRL2: L1A
GCTRL3: RESET
GCTRL4: CMS Clock

FSTAT0: F1 Empty~
FSTAT1: F2 Empty~
FSTAT2: F1 PAE~
FSTAT3: F2 PAE~
FSTAT4: F1 FULL~
FSTAT5: F2 FULL~
FSTAT6: FPGA Status
FSTAT7: FPGA Status
FSTAT8: FPGA Status
FSTAT9: FPGA Status
FSTAT10: FPGA Status
FSTAT11: FPGA Status

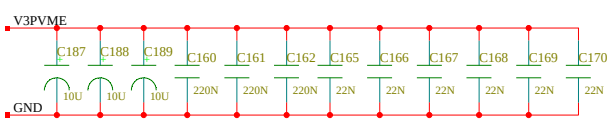
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

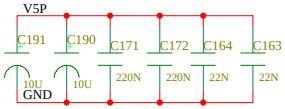
TITLE: FIFO_1 data storage
CMS CSC DCC
CMS CSC ELECTRONICS

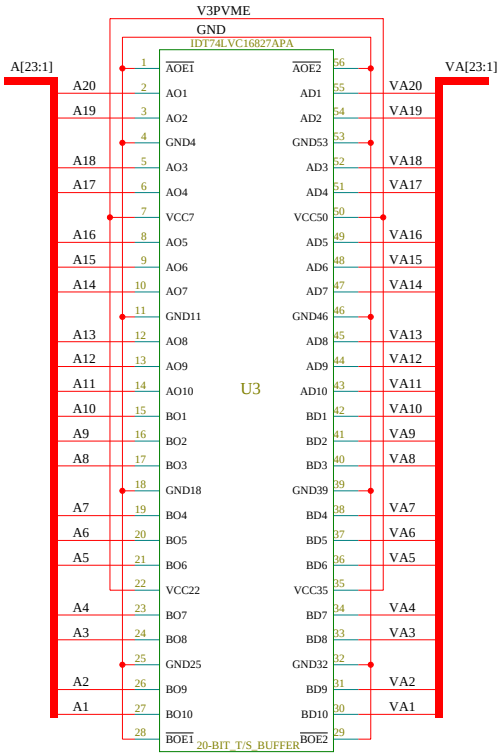
BY: GU
PARENT PAGE: 1
PROJECT: DCC
DATE: 11-1-2005_13:42
FILE: RECEIVEF4 . 2
PAGE: 16A

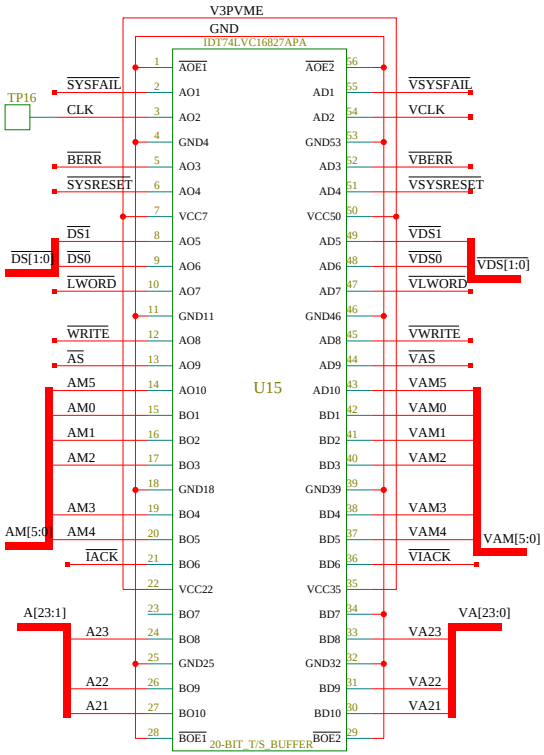


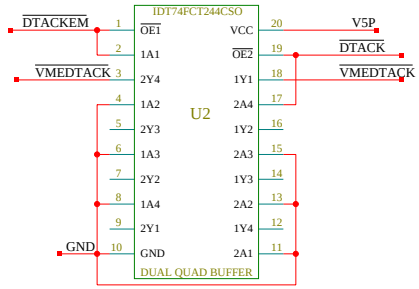
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE VMEbus P1 CMS CSC Data Concentrator Card CMS CSC Electronics	BY GU	PARENT PAGE 1	PROJECT DCC
		DATE 11-1-2005_10:33	FILE VME . 1	PAGE 20



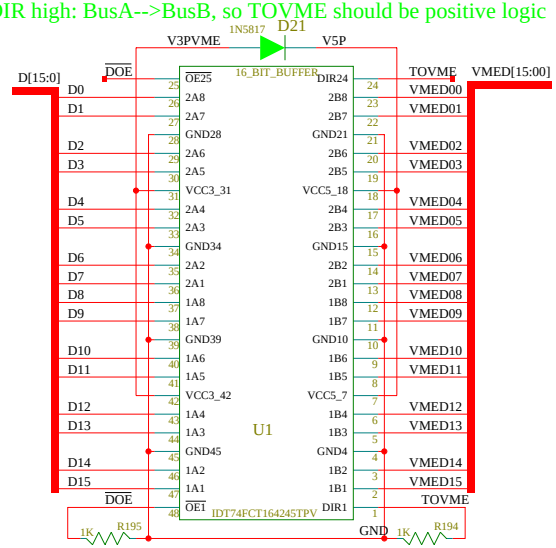








The Diode here to maintain (Vcc5 > Vcc3-0.5V) requirement
DIR high: BusA-->BusB, so TOVME should be positive logic

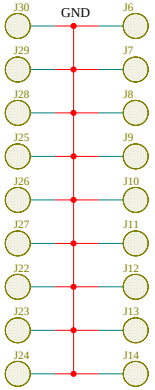


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

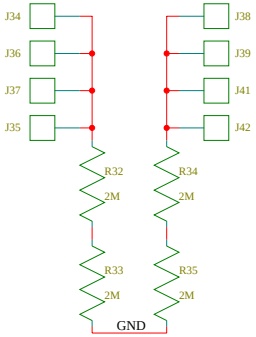
TITLE: VMEbus P1 transceivers
CMS CSC Data Concentrator Card
CMS CSC Electronics

BY: GU
PARENT PAGE: 1
PROJECT: DCC
DATE: 11-1-2005_10:33
FILE: VME . 2
PAGE: 20A

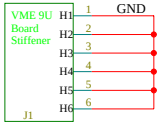
GROUND POINTS



DISCHARGE UNIT

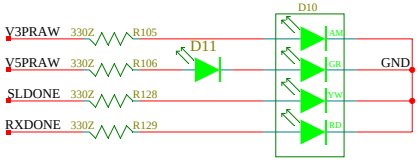


BOARD STIFFENER

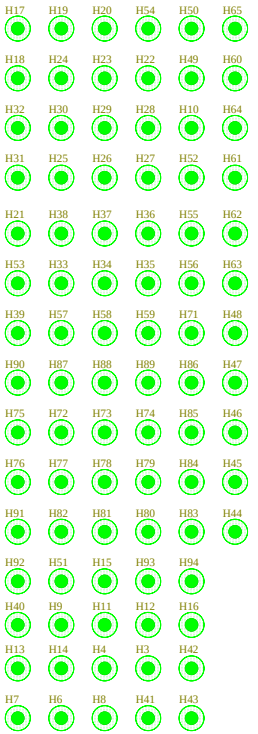


FRONT PANEL MOUNTS

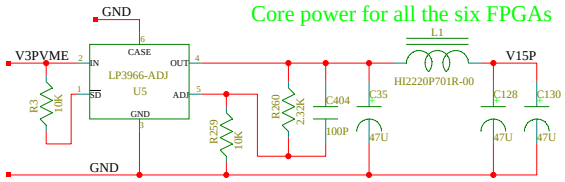
POWER MONITOR



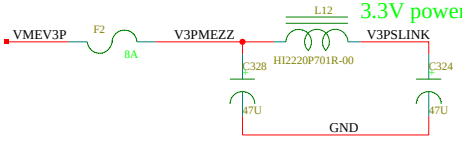
PART FIDUCIALS



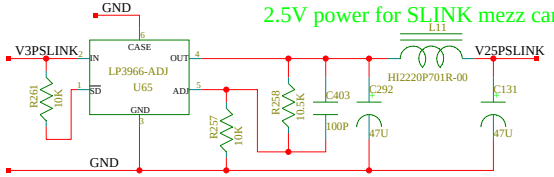
Core power for all the six FPGAs

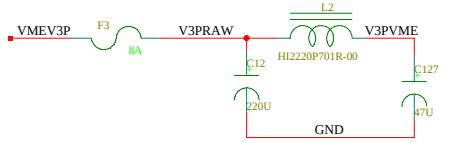


3.3V power for SLINK mezz cards

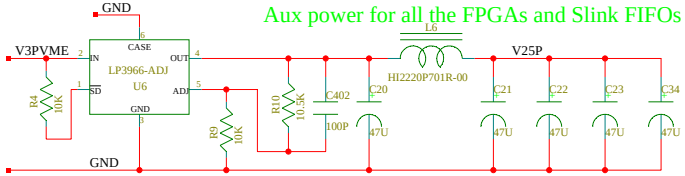


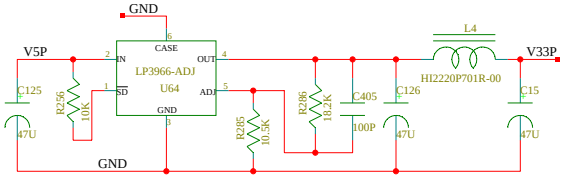
2.5V power for SLINK mezz cards



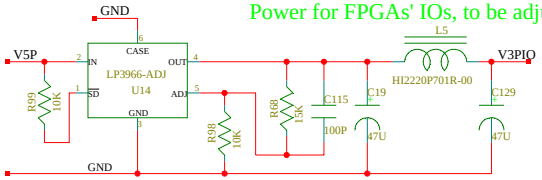


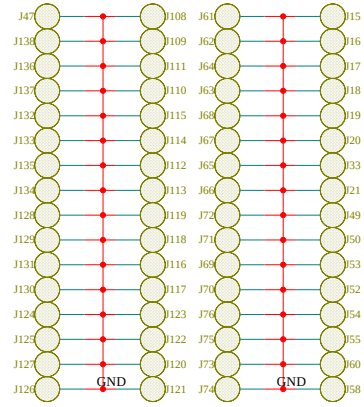
Aux power for all the FPGAs and Slink FIFOs





Power for FPGAs' IOs, to be adjusted at 3.0V



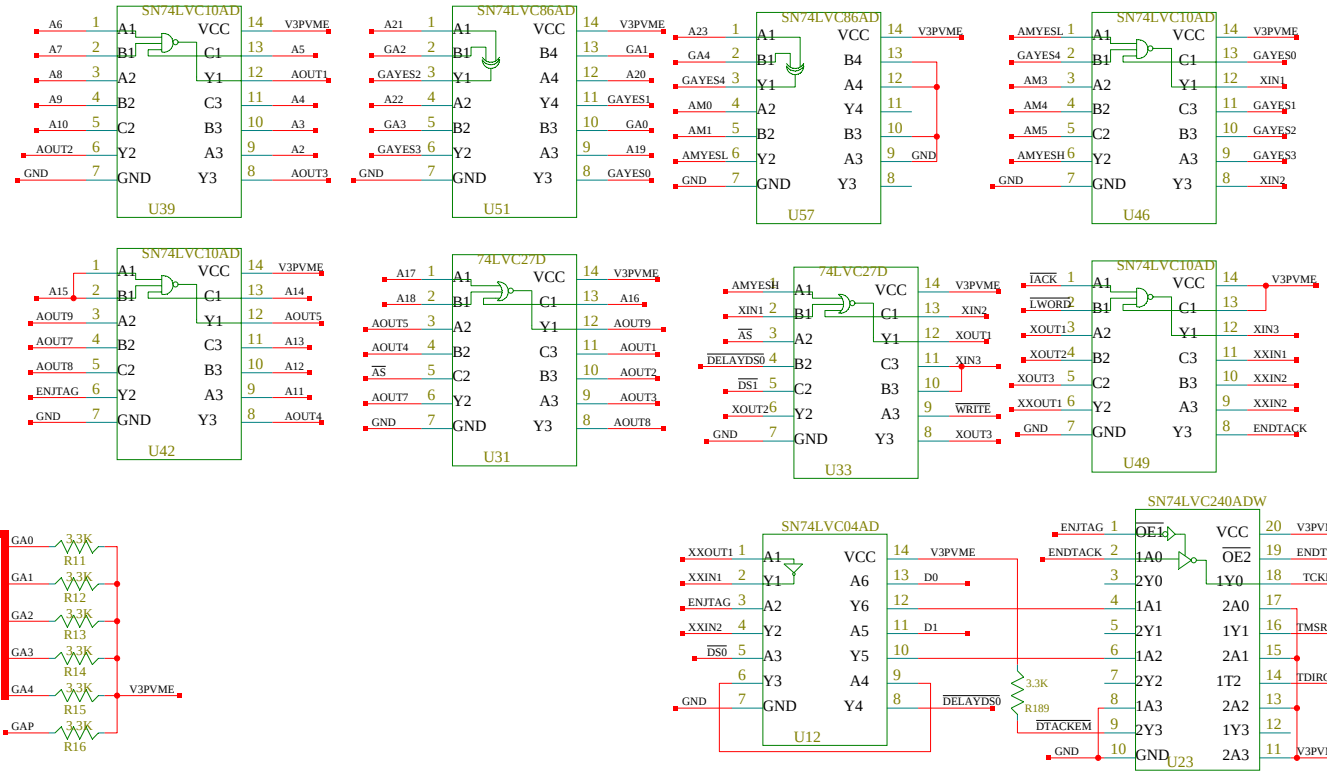


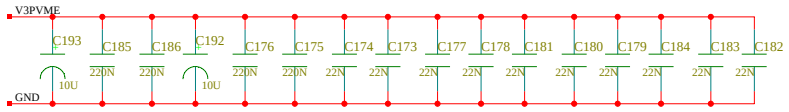
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Power, Ground, stiffener
CMS CSC Data Concentrator Card
CMS CSC ELECTRONICS

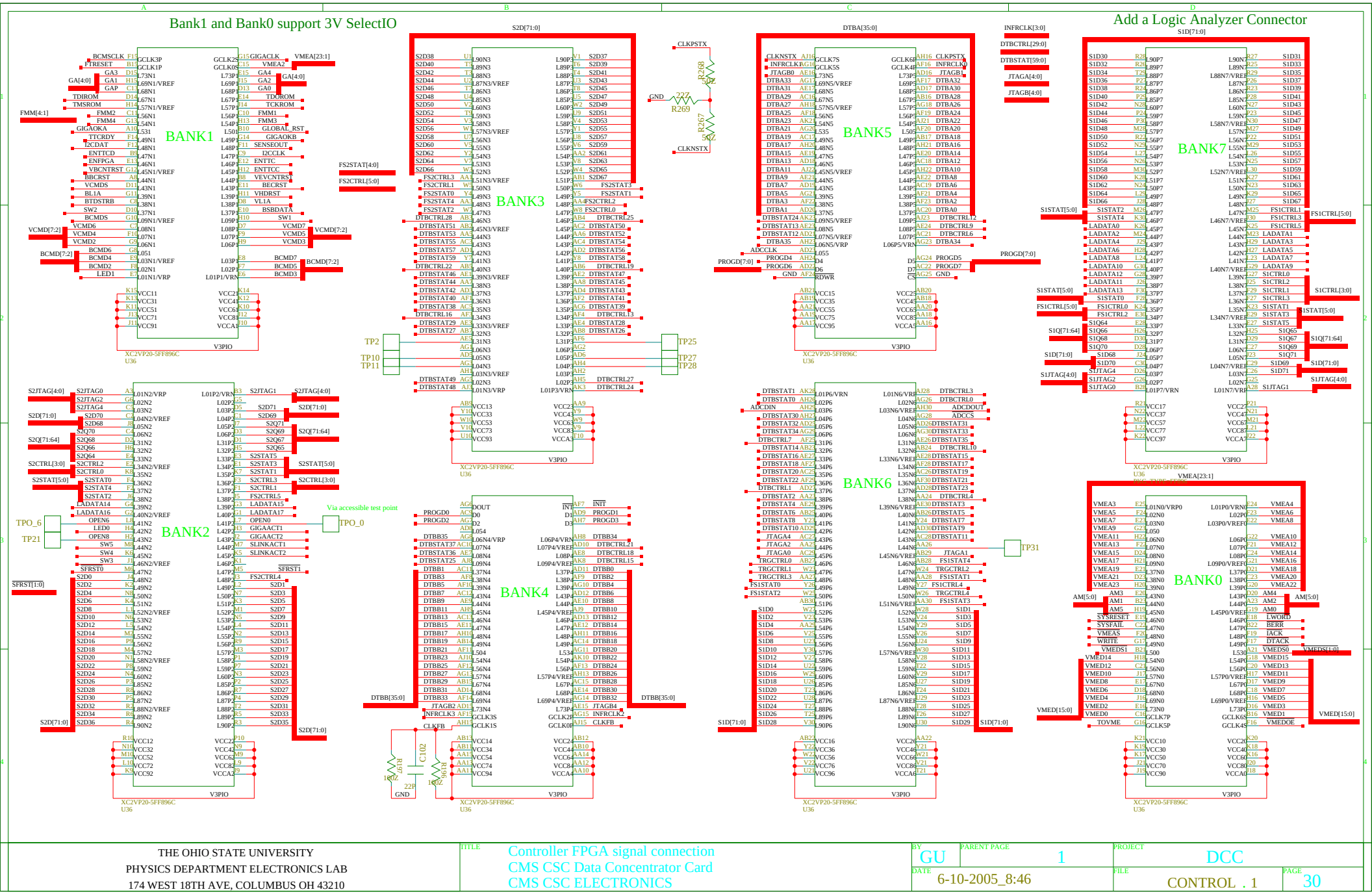
BY: DCH
PARENT PAGE: 1
PROJECT: DCC
DATE: 12-5-2005_16:51
FILE: VME . 3
PAGE: 20B

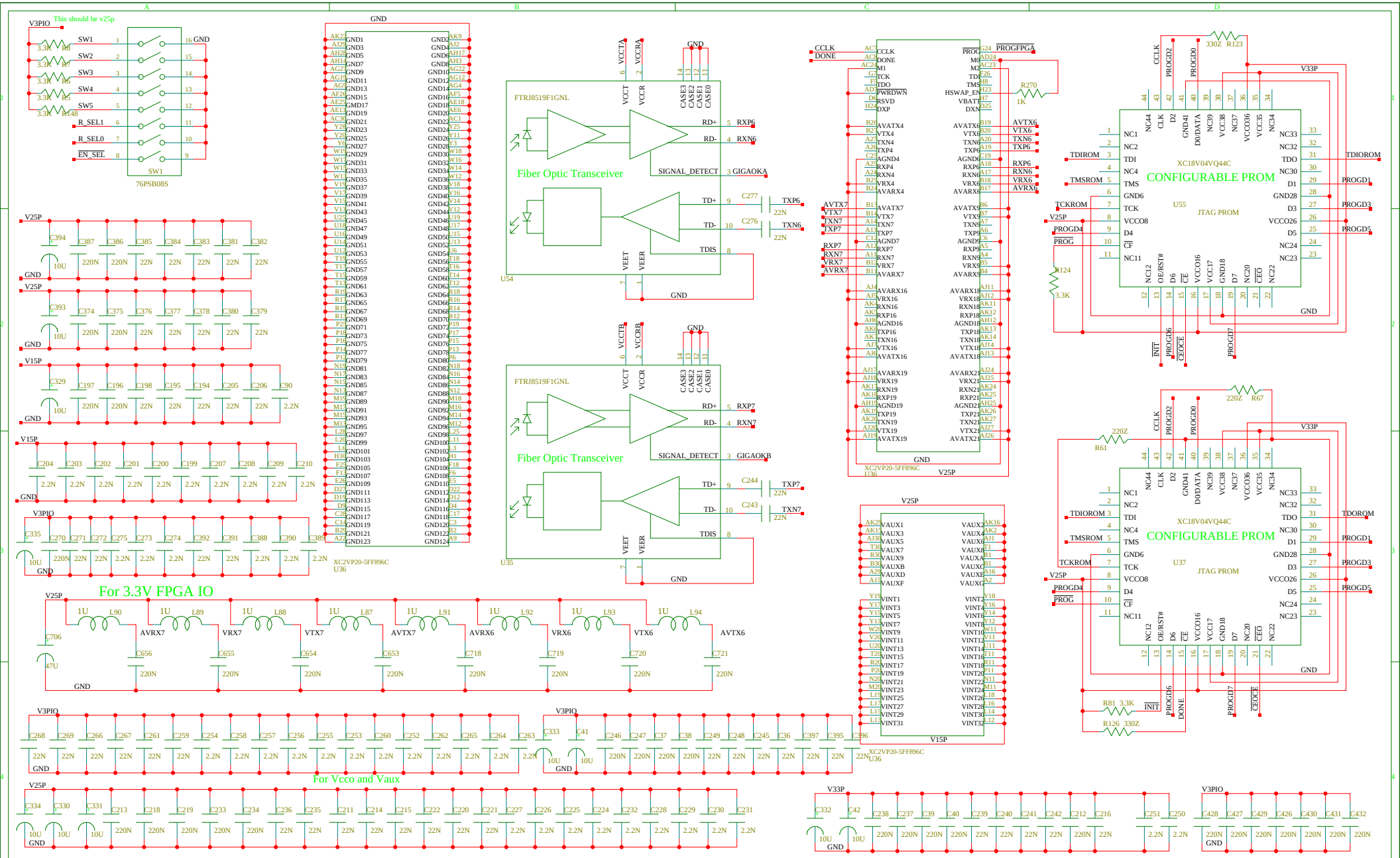
Discrete logic to load the VPROM in emergency



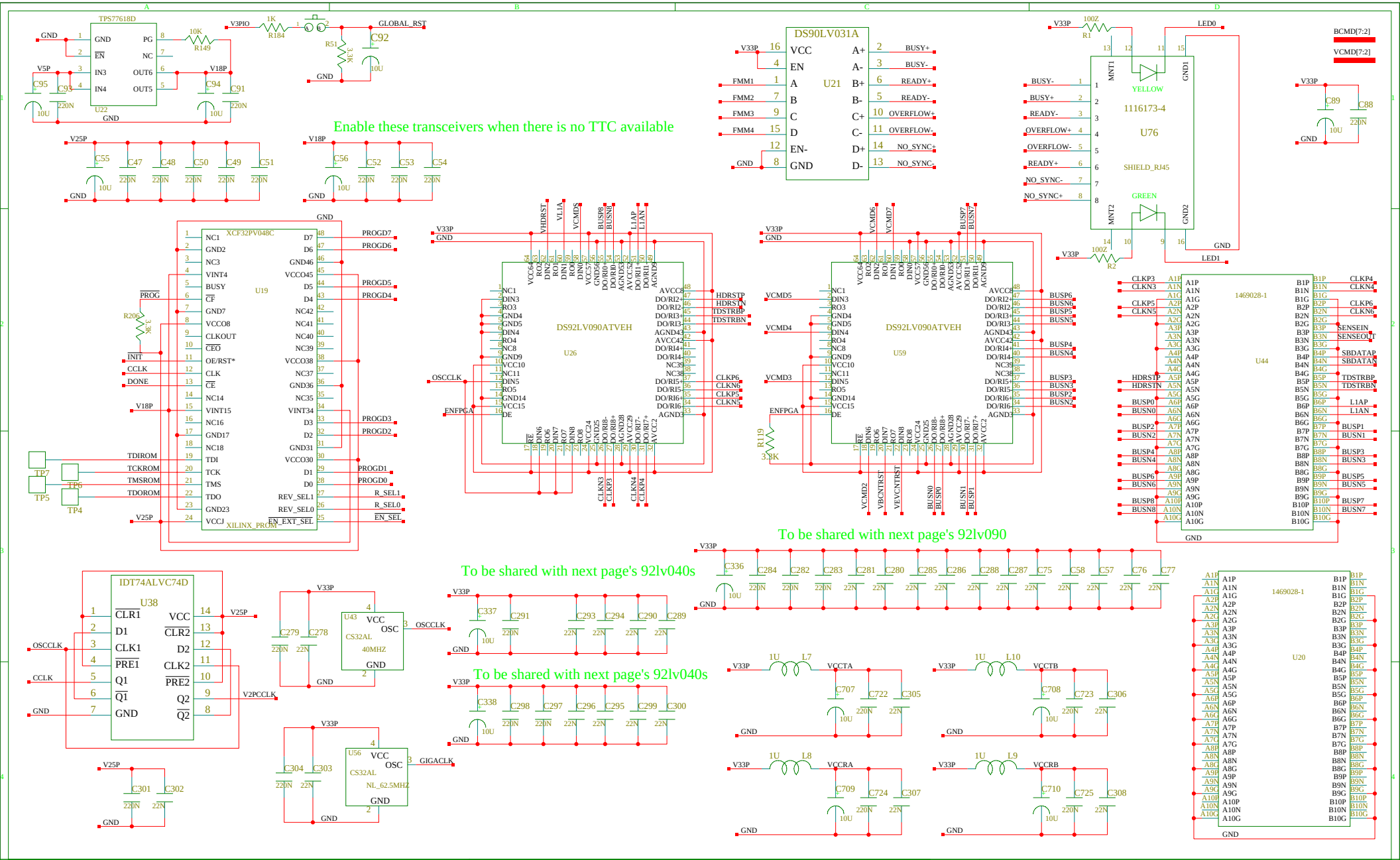


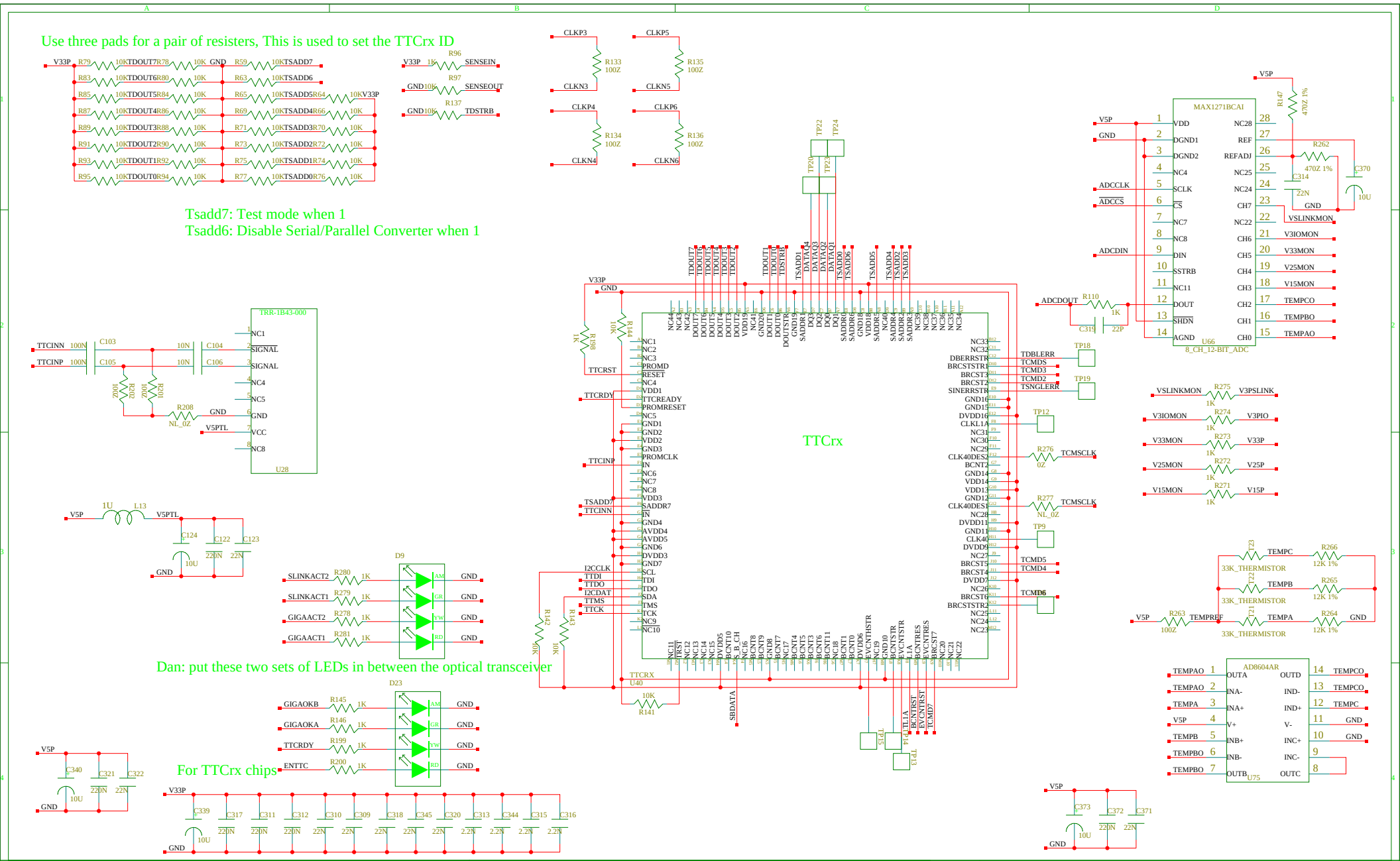
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Emergency start CMS CSC Data Concentrator Card CMS CSC ELECTRONICS	BY: GU DATE: 11-1-2005_10:33	PARENT PAGE: 1 FILE: VME . 4	PROJECT: DCC PAGE: 20C


Bank1 and Bank0 support 3V SelectIO
Add a Logic Analyzer Connector
BANK1
BANK2
BANK3
BANK4
BANK5
BANK6
BANK7
BANK0
XC2VP20-5FF896C
U36
V3PIO
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
Controller FPGA signal connection
CMS CSC Data Concentrator Card
CMS CSC ELECTRONICS
GU
1
DCC
6-10-2005_8:46
CONTROL . 1
30



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Controller FPGA power and ISPROM CMS CSC Data Concentrator Card CMS CSC ELECTRONICS	BY: GU	PARENT PAGE: 1
		DATE: 9-7-2005_11:31	PROJECT: DCC
			FILE: CONTROL . 2
			PAGE: 30A


Enable these transceivers when there is no TTC available
To be shared with next page's 92lv090
To be shared with next page's 92lv040s
To be shared with next page's 92lv040s
TPS77618D
DS90LV031A
U21
YELLOW
1116173-4
U76
SHIELD_RJ45
GREEN
BCMD[7:2]
VCMD[7:2]
XCF32PV048C
U19
XILINX_PROM
DS92LV090ATVEH
U26
DS92LV090ATVEH
U59
1469028-1
U44
IDT74ALVC74D
U38
CS32AL
40MHZ
U43
CS32AL
NL_62.5MHZ
U56
1469028-1
U20
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
TTCrx interface
CMS CSC Data Concentrator Card
CMS CSC ELECTRONICS
BY
GU
PARENT PAGE
1
PROJECT
DCC
DATE
9-22-2005_14:48
FILE
CONTROL . 3
PAGE
30B


Use three pads for a pair of resisters, This is used to set the TTCrx ID
Tsadd7: Test mode when 1
Tsadd6: Disable Serial/Parallel Converter when 1
TTCrx
Dan: put these two sets of LEDs in between the optical transceiver
For TTCrx chips
MAX1271BCAI
8_CH_12-BIT_ADC
AD8604AR
TRR-1B43-000
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
TTCrx interface
CMS CSC Data Concentrator Card
CMS CSC ELECTRONICS
BY
GU
PARENT PAGE
1
PROJECT
DCC
DATE
7-29-2005_10:38
FILE
CONTROL . 4
PAGE
30C

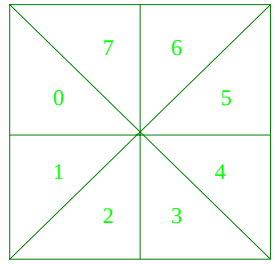
If BAP and BAN is connected on the backplane, the SENSEOUT will be high, or else it will be low

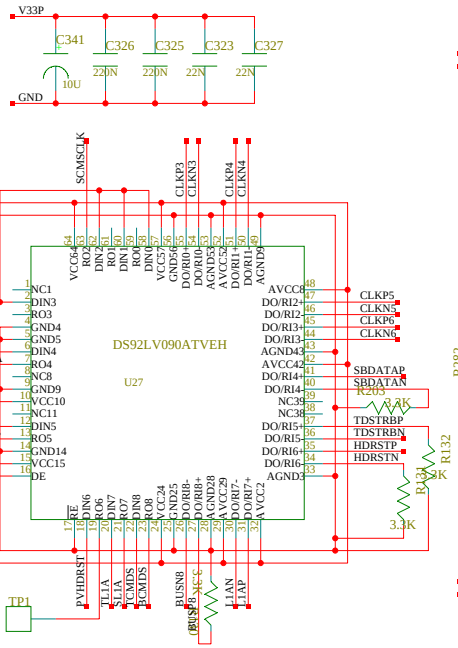
The bus signals are terminated on both ends of the backplane with 100 Ohm

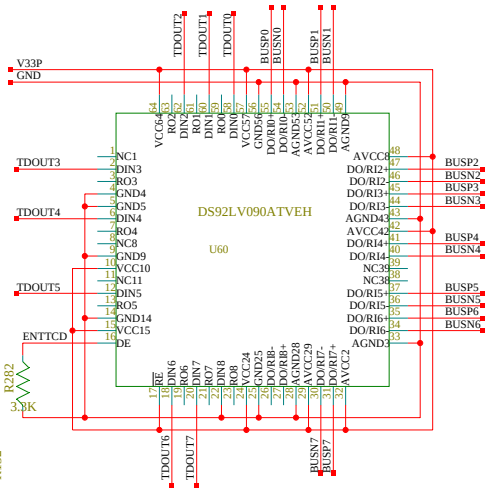
The clock signals are terminated on this board and the backplane, except the passive DCC slot

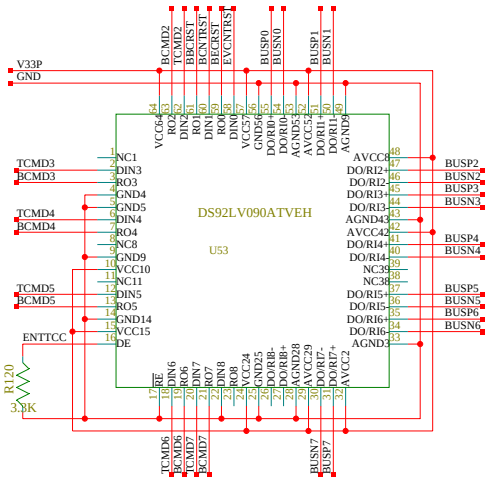
clock3: slot 3,4,5,6,7; clock5: 8,9,10,11,12,13; clock6: 14,15,16,17; clock4: 18,19,20

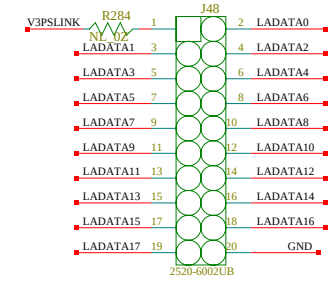
(slot 8 is the avtive DCC, slot 17 is the passive DCC)

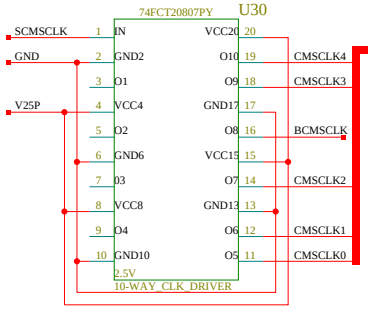


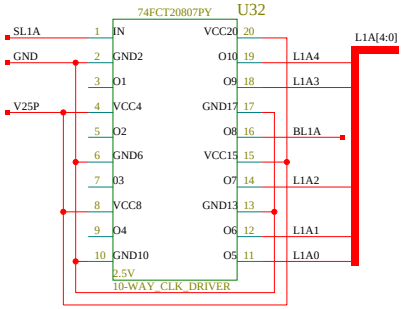


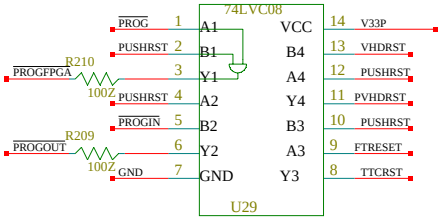


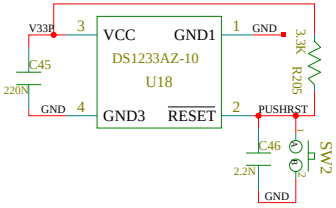


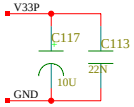


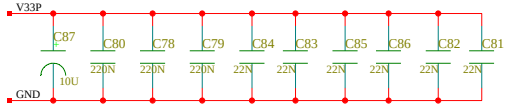


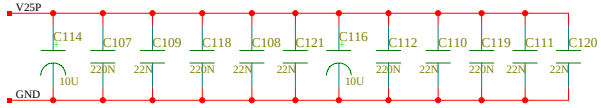










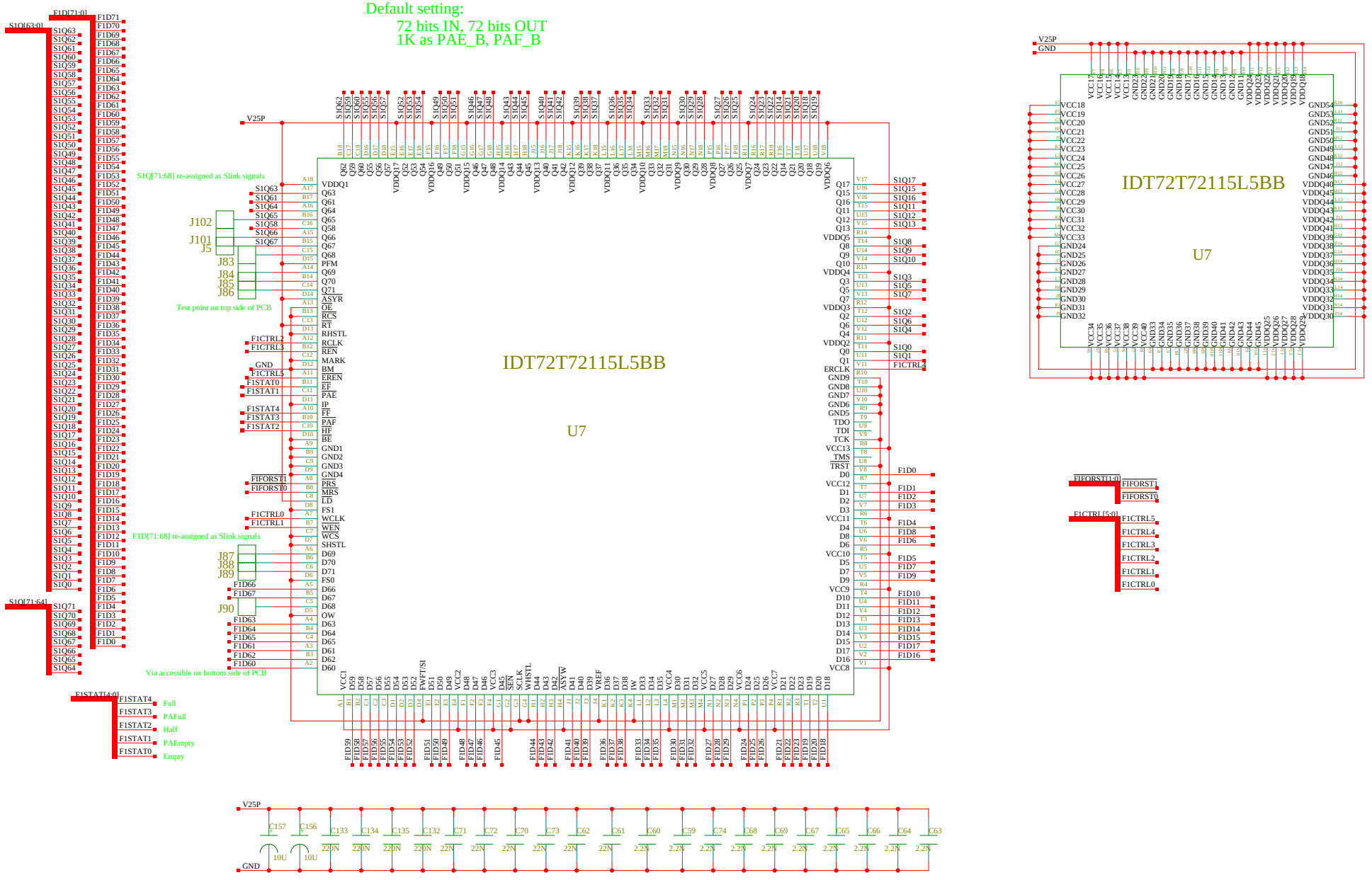


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

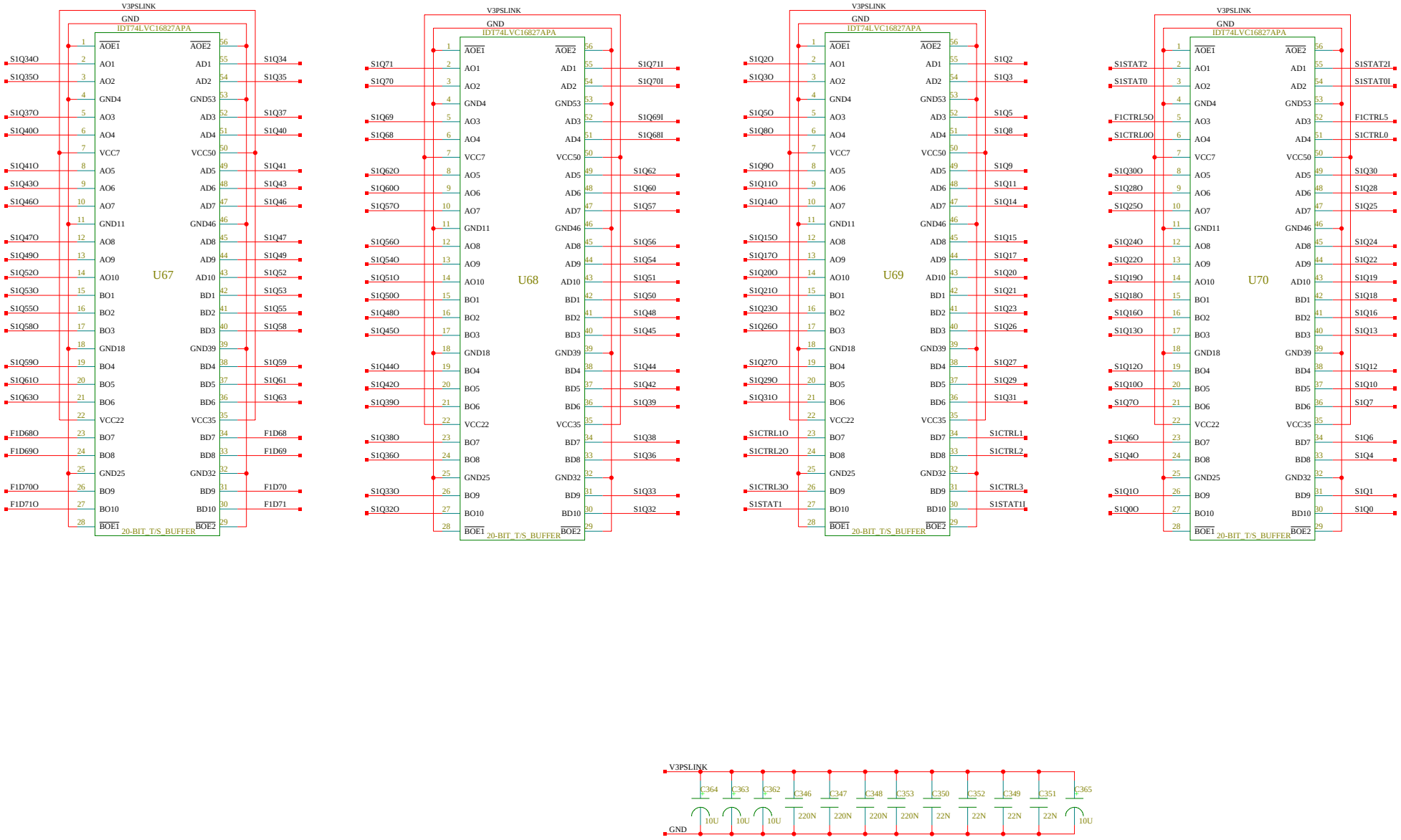
TITLE: TTCrx data to backplane interface; Controller FPGA signal connection
CMS CSC Data Concentrator Card
CMS CSC ELECTRONICS

BY	PARENT PAGE	PROJECT
GU	1	DCC
DATE		FILE
12-5-2005_16:49		CONTROL . 5

PAGE: 30D



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: First S-link64 interface FIFO CMS CSC Data Concentrator Card CMS CSC ELECTRONICS	BY: GU	PARENT PAGE: 1
		DATE: 11-1-2005_10:21	PROJECT: DCC
		FILE: DATAOUT . 1	PAGE: 40



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE
First SLINK INTERFACE
CMS CSC Data Concentrator Card
CMS CSC Electronics

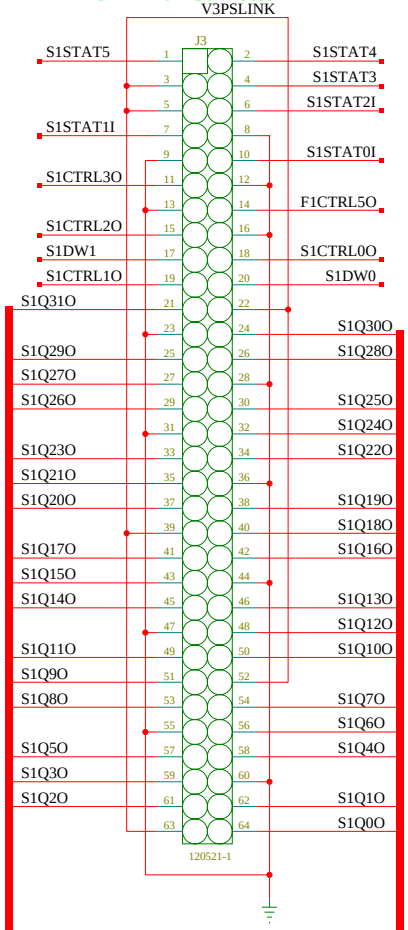
BY DCH/GU
PARENT PAGE 1
PROJECT DCC
DATE 11-1-2005_10:21
FILE DATAOUT . 2
PAGE 40A

Implement basic S-LINK architechture on DDU board?

Replace these control with S1STAT[4:0] and S1CTRL[4:0]

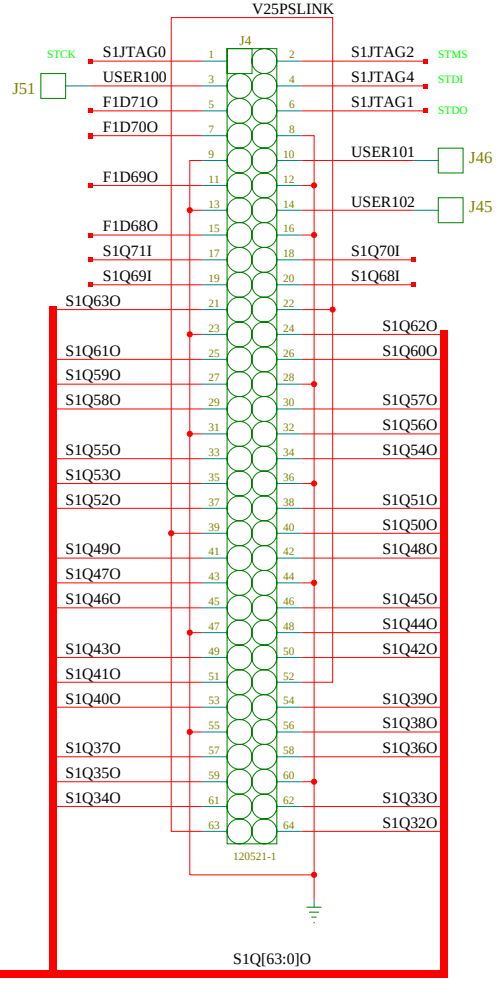
AMP 120521-1

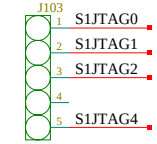
SLINK64 Connector 1



JTAG NOT IMPLEMENTED ON SLINK

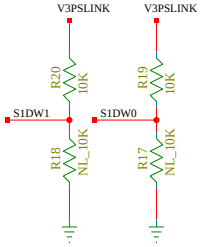
SLINK64 Connector 2 EXT 64





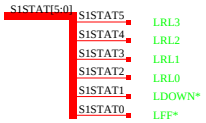
Not Used on Current LSC

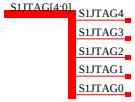
S1QW[0:1] = 11 FOR 64 BIT TRANSFERS



SLINK64/LSC Standoff Holes

Isolated per SLINK Spec pg. 43/62





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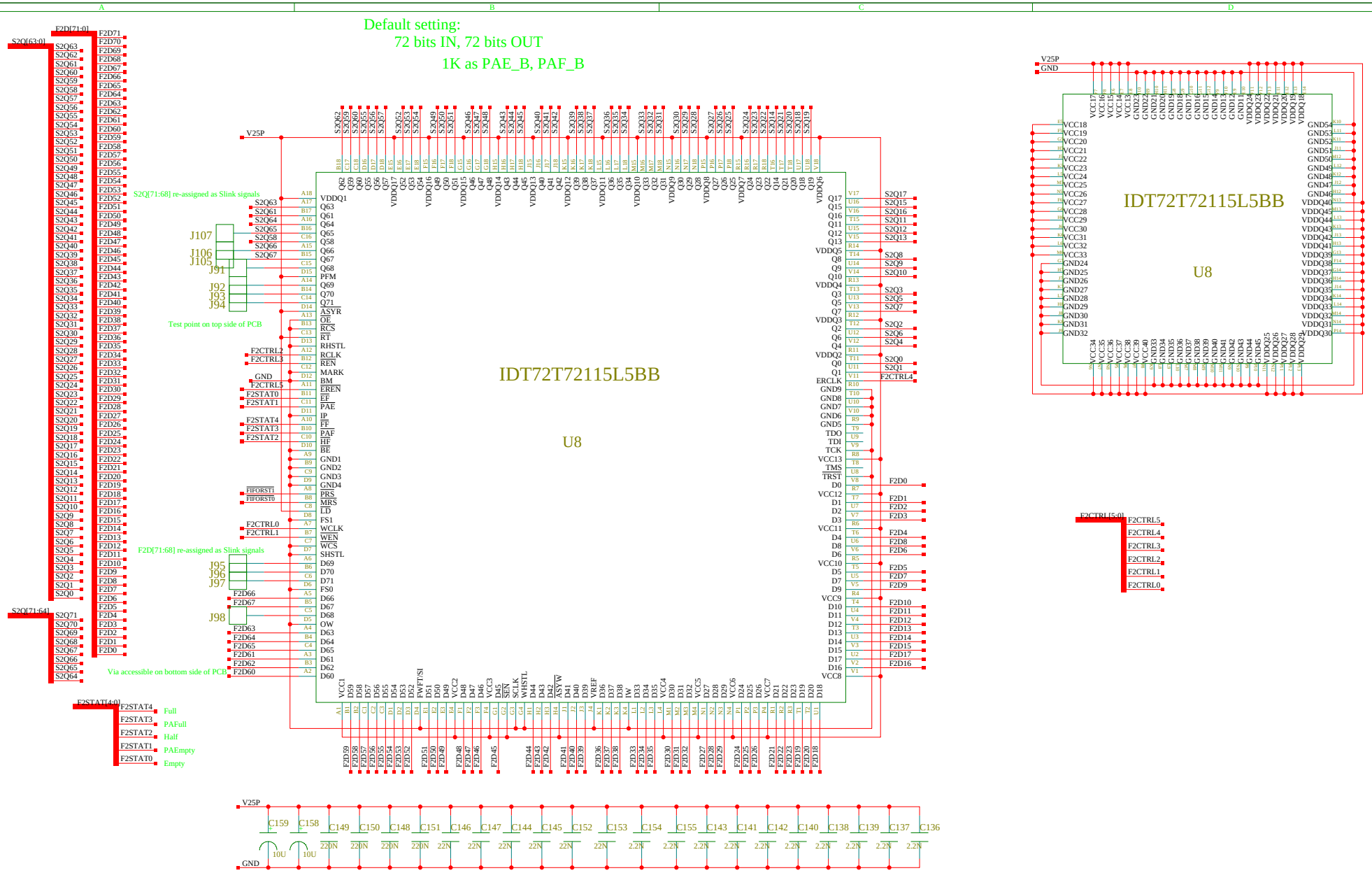
TITLE: First SLINK INTERFACE
CMS CSC Data Concentrator Card
CMS CSC Electronics

BY: DCH/GU
PARENT PAGE: 1
PROJECT: DCC
DATE: 12-5-2005_16:50
FILE: DATAOUT . 3
PAGE: 40B



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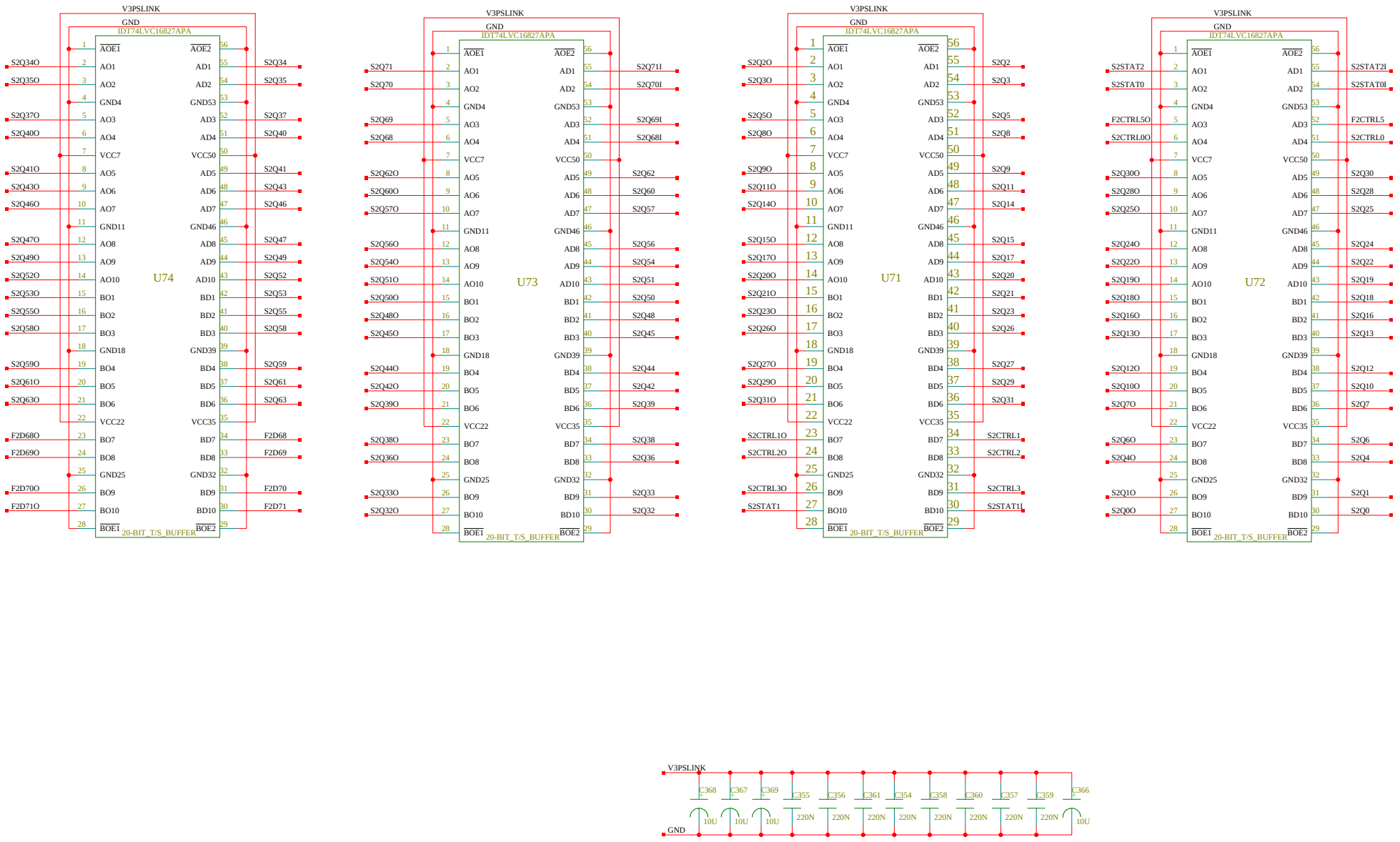
		DATE: 11-1-2005_10:21	FILE: DATAOUT . 4
		PROJECT: DCC	PAGE: 40C



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Implement basic S-LINK architechture on DDU board?

Replace these control with S2STAT[4:0] and S2CTRL[4:0]

AMP 120521-1

SLINK64 Connector 1

V3PSLINK

J44

S2STAT5 1 2 S2STAT4
3 4 S2STAT3
5 6 S2STAT2I
S2STAT1I 7 8
9 10 S2STAT0I
S2CTRL3O 11 12
13 14 F2CTRL5O
S2CTRL2O 15 16
S2DW1 17 18 S2CTRL0O
S2CTRL1O 19 20 S2DW0
S2Q31O 21 22
23 24 S2Q30O
S2Q29O 25 26 S2Q28O
S2Q27O 27 28
S2Q26O 29 30 S2Q25O
31 32 S2Q24O
S2Q23O 33 34 S2Q22O
S2Q21O 35 36
S2Q20O 37 38 S2Q19O
39 40 S2Q18O
S2Q17O 41 42 S2Q16O
S2Q15O 43 44
S2Q14O 45 46 S2Q13O
47 48 S2Q12O
S2Q11O 49 50 S2Q10O
S2Q9O 51 52
S2Q8O 53 54 S2Q7O
55 56 S2Q6O
S2Q5O 57 58 S2Q4O
S2Q3O 59 60
S2Q2O 61 62 S2Q1O
63 64 S2Q0O

120521-1

JTAG NOT IMPLEMENTED ON SLINK

SLINK64 Connector 2 EXT 64

V25PSLINK

J31

STCK J59 S2JTAG0 1 2 S2JTAG2 STMS
USER200 3 4 S2JTAG4 STDI
F2D71O 5 6 S2JTAG1 STDO
F2D70O 7 8
9 10 USER201 J56
F2D69O 11 12
13 14 USER202 J57
F2D68O 15 16
S2Q71I 17 18 S2Q70I
S2Q69I 19 20 S2Q68I
S2Q63O 21 22
23 24 S2Q62O
S2Q61O 25 26 S2Q60O
S2Q59O 27 28
S2Q58O 29 30 S2Q57O
31 32 S2Q56O
S2Q55O 33 34 S2Q54O
S2Q53O 35 36
S2Q52O 37 38 S2Q51O
39 40 S2Q50O
S2Q49O 41 42 S2Q48O
S2Q47O 43 44
S2Q46O 45 46 S2Q45O
47 48 S2Q44O
S2Q43O 49 50 S2Q42O
S2Q41O 51 52
S2Q40O 53 54 S2Q39O
55 56 S2Q38O
S2Q37O 57 58 S2Q36O
S2Q35O 59 60
S2Q34O 61 62 S2Q33O
63 64 S2Q32O

120521-1

J104
1 S2JTAG0
2 S2JTAG1
3 S2JTAG2
4
5 S2JTAG4

S2DW1 S2DW0

V3PSLINK V3PSLINK

R39 10K R101 10K

R102 NL_10K R100 NL_10K

SLINK64/LSC Standoff Holes

Isolated per SLINK Spec pg. 43/62

H103 H101

S2STAT[5:0] S2STAT5 LRL3
S2STAT4 LRL2
S2STAT3 LRL1
S2STAT2 LRL0
S2STAT1 LDOWN*
S2STAT0 LFF*

S2CTRL[3:0] S2CTRL3 UCLK
S2CTRL2 URESET*
S2CTRL1 UCTRL*
S2CTRL0 UTEST*

S2JTAG[4:0] S2JTAG4
S2JTAG3
S2JTAG2
S2JTAG1
S2JTAG0

S2Q64 R125 0Z S2CTRL1

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