Status of CFEB, DMB, DDU

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(Reported by J. Gilmore)

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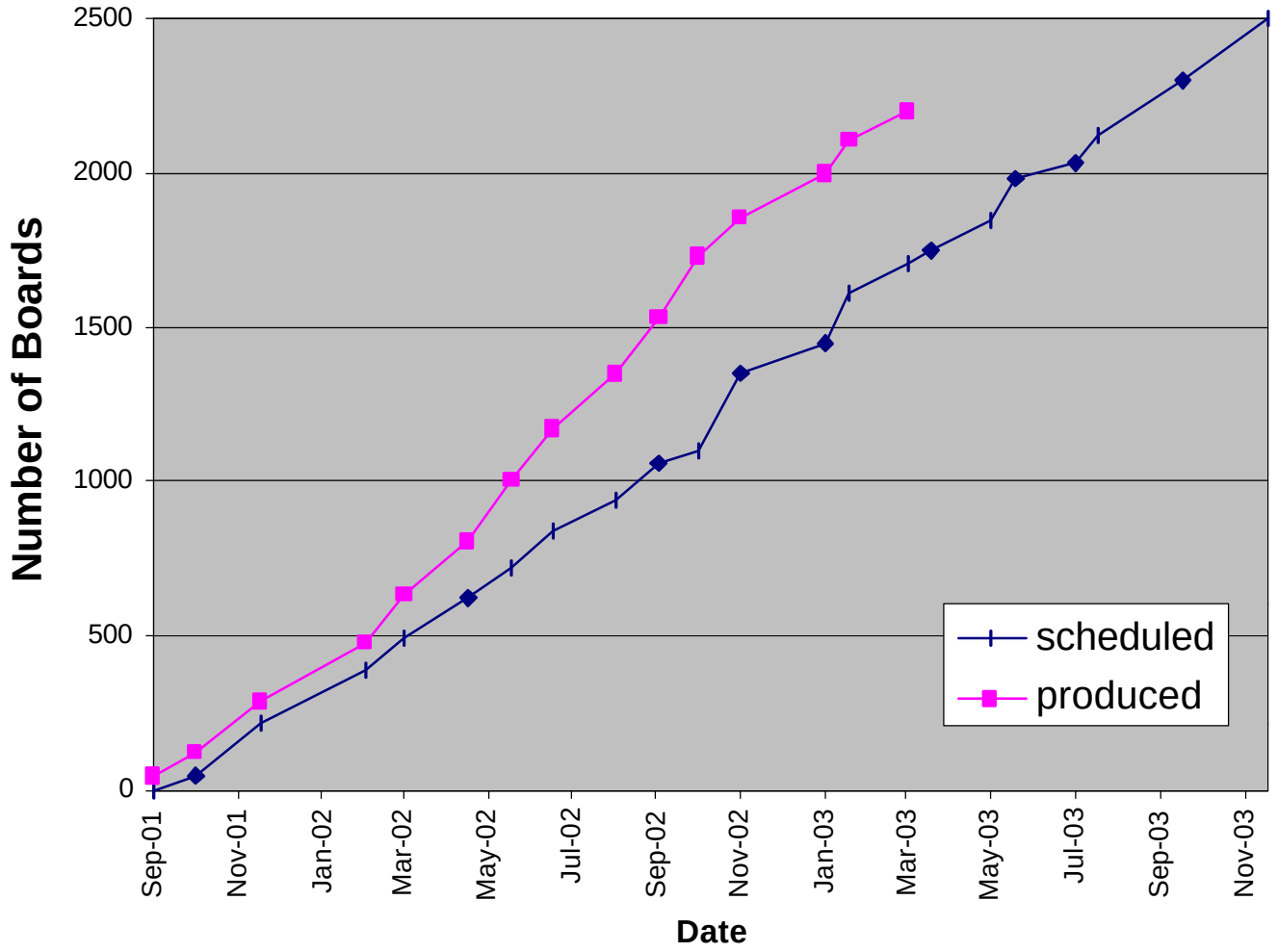
CFEB Production Status

- **A total of 2500 CFEB's will be built.**

Baseline **ME1/2, ME1/3, ME2/1,2 ME3/1,2**	**1728**
ME1/1	**360**
Spares	**412**
Total	**2500**

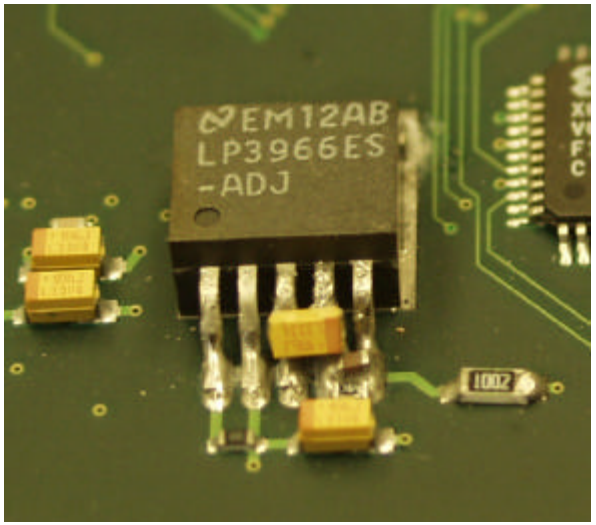
- **As of 3/2003, 2200 of the 2500 boards have been assembled and tested at Ohio State.**
- **Shipment to all FAST sites is on or ahead of schedule.**
- **Expect to finish production by June 03.**

CFEB Production Rate



CFEB Repairs

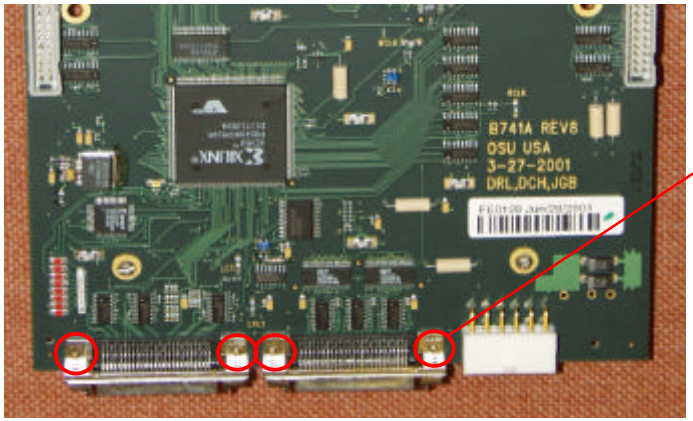
- **Some rejected CFEB's had large pedestal shifts. Problem traced to bad soldering of LV regulator used on the early Rev-8 boards (125 boards).**
  - **National regulators were hand soldered on the 125 Rev-8 boards.**
  - **Solder flux underneath the resistor (or capacitor) was not removed well.**
  - **Moisture absorption lowers the effective resistance between pins, dropping the voltage to Buckeye chip.**



- **All Rev-8 CFEB's not yet mounted were sent back to OSU and fixed. (Oct-02)**
- **B. Bylsma traveled to CERN in Jan-03 and fixed all Rev-8 boards already mounted on CSC's.**

Loose Screws

- **Some screws holding skew-clear cable connector to the CFEB have fallen off after shipping to CERN.**



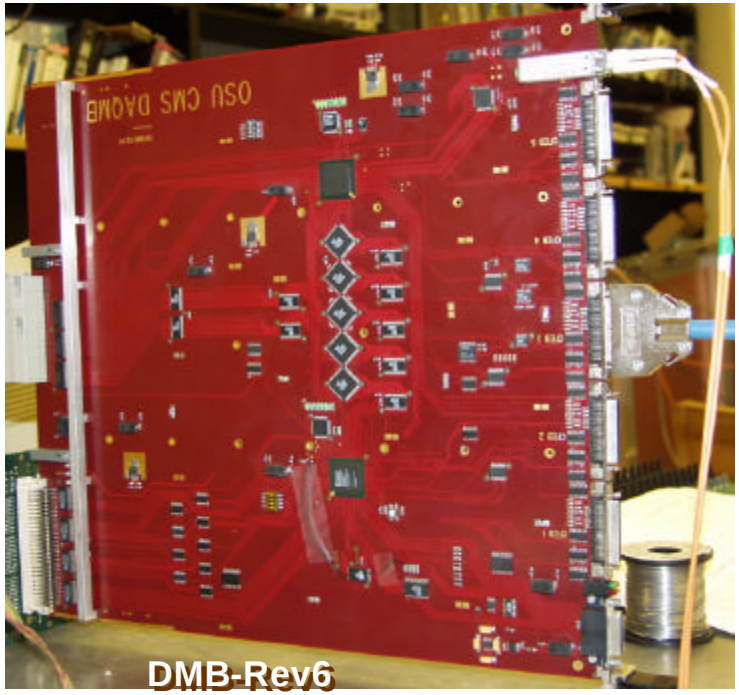
These screws were put on after the board was tested by a technician. Apparently they were not tight enough.

- **Solution proposed and adopted by the collaboration:**
  - **CFEB's already mounted on CSC's: check for screw tightness, dismount CFEB and tighten screw if necessary, then apply "lock-tite" fluid.**
  - **CFEB's not yet mounted on CSC's: check and tighten screws then use "lock-tite" fluid.**
  - **CFEB's at OSU (~1300 to be shipped) have all been fixed.**

DMB Prototype History

	Number	Remarks
DMB – rev 4 (2001-02)	**15**	**13 delivered to UF, UCLA, IHEP,PNPI, CERN and DUBNA. 2 more assembled - to be tested and delivered to UF.**
DMB – rev 5 (2002)	**4**	**Used for first integration test at UCLA in 4/02.**
DMB – rev 6 (2003)	**6**	**2 assembled and tested. To be used for tests at UCLA and CERN (4/03-5/03)**

Preproduction DMB (Rev6)

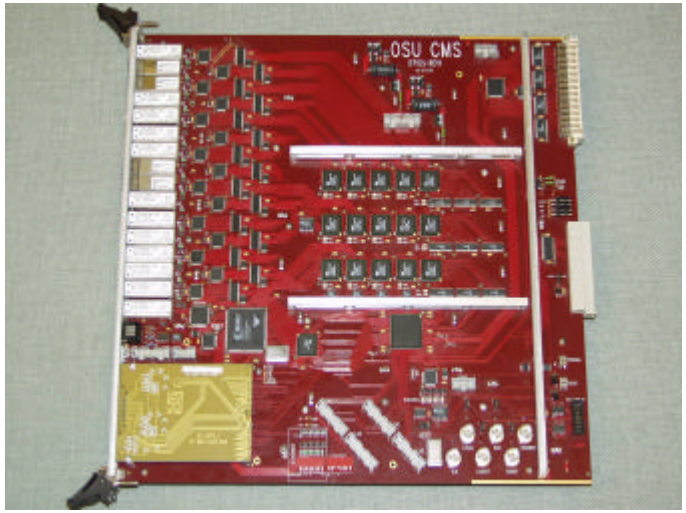


- Uses gold-plated traces - solves soldering problems that plagued Rev4 boards.
- Added a FIFO for ALCT data. Now there are seven FIFO's, five for CFEBs, one for TMB, one for ALCT.
- Added another Flash Memory (AT49BV512) for BUCKEYE pattern loading.

- Optical transceiver changed from Agilent to Finisar.
- DDU or 'translator' card is required to send data from DMB to computer. Data path via Gigabit Ethernet removed.
- Added several serial resistors on LVMB signals as asked by UCD.

DDU Development

- **First 9U DDU board. Produced and tested in 2002. This board will be used for beam test at CERN (May 03).**



- ✓ **Full error checking implemented**
- ✓ **Interface to VME**
- ✓ **PC readout via Gigabit Ethernet (90 MB/s data transfer)**
- ✓ **DMB calibration pulses, regular and random timing**
- ✓ **S-Link64 tested**
- – **Need to integrate w/ FMM and TTS**

- **For next revision of DDU, we plan to use Virtex-II Pro FPGA's to handle input logics, gigabit ethernet and main control. Output data will be sent to DCC's via custom backplane.**
- **EMU will have 36 DDU's and 8 DCC's in 4 FED crates located in USC55.** *(http://cmsdoc.cern.ch/~wsmith/USC55_racks.html)*