DDU5CTRL (file 0dductrl)

6-19-2009_14:34

CF048A01 Version 48

CMS CSC DDU5, Central Control FPGA

v40: DMB & Trig.CRCs use MUX to load Zeroes (not Tbufs), change DDUfb reset
-r2: add time constraint to DDUFB reg to eliminate DDUCRC logic lag. r3: tune BuffOvfl & EthLim logic
v41: SCA_Ovfl separated from DMB_Err & SomethingBad. r2: tune KillFiber glitch
v42: change to proposed format for ALCT; r2: FOV=6, on TFsig kill ALCT/TMBerr, correct SBXN for
3564-4096 difference in BX<40 case (from CloseL1A logic) r3: change to new ALCT/TMB data format
r4: fix TRG bugs in stage2 r5: reduce RST logic delays, may have caused TrgTrail detect problems
added bit usage notes in FIFOCTRL, 27nov2007 v43: tune CMD Strobe timing; r2, adjust TMB/ALCT Fful bits
r3: fixed bug in TrgL1err reporting. v44: change TF-DDU definition (0xc0 in Flash-Page7)
v45: tune TrigTrailProb, CfebCntErr logic, add CSC RepeatErr logic to LsumErr reg & take it to JTAG F35
r2: remove DMBwarn from FMMwarn logic. r3: add vote3 for DDUCRC r4: remove CRC voting, delay S-Link clock by 3.2ns
v46: tests ck156, SLink clk from DCM --> SLink. r2: shift OWCLK by +3.2ns
v47: move ROD pipe reg. into stage2 before DDUCRC
v48: GbE skips Empty Events for Global runs

Set All I/O to 3.3V

PART=XC2VP7-6-FF672

PROM=2*XC18V04-VQ44 (PARALLEL)

DDU5ctrl\DDU5ctrl\ddu5ctrl
C045DD99
C145DD99

DDUCNTRL

PromID: 05026093h
FPGAid: 2124A093h

PROGRAM takes < 55 ms (31ms this FPGA)

1: Mode Bit 0 LED0 on top, pins on away-side from LEDs
2: Mode Bit 1 RST_1=Asynchronus Reset for FPGA1 and ALL FIFOs
3: Mode Bit 2
4: Mode Bit 3
5: Mode Bit 4; High for GBE debug, Low otherwise
6: GbE test, send counter on GBE link
7: Set L1A Fake mode, Kill TTC L1A/BXR/ECR if SW8 is off
8: FPGA version on LEDs

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DDU Format Since DDUctrl v15:

BOE1 type L1A Number BXN ID FOV K-Status
H1: 0x/5T/NN.NNNN/XXX/I.II/VK

49-bit ~unique constant DMBfull(15)
H2: 0x/8000/0001/8000/HHHH

LiveDMB(15) Ostat DMB-DAV(15) BOEstat DMBcnt
H3: 0x/LLLL/oooo/ZZZZ/GGMY

64-bit unique constant
T-2: 0x/8000/FFFF/8000/8000

DDU EOE Status DMBerr DMBwarn(15)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP

EOE WordCount CRCword EOEstat K-Status
TR: 0x/A/?/WW.WWWW/RRRR/UUMK

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount _8 TS assumed_

mojo

DDU5CTRL -- Project History

v1-2: from ddu4ctrl_v28, FIFO Full JTAG Reg is 16-bits
Last w/DDU_FOV=4 --->> v10-12: Add RCLK1, Tune OutUnit GT resets, tune DCC_WAIT modes & add Klll optio
v13-14: Fix LVT/LVA, kill DMB-CFEB-Sync, bring DMB Results to CRCerr; tune DMB checks, GbE Prescale & SLinkWtEn from VMEct
v15-16: fix DMBwarn, add VME_FakeL1enable; put DMBLIVE[14:0] in HDR3; put DMBwarn/err in TR-1, Tune TRG_Trail_Err resets, FOV=
v17-18: tune DMB_Full, RST_InStat, EndTimeRST, PRST, add InRD-C-Code JTAG path (F20), GbE Packets now 7952 byte
v19: Require SLinkWaitEn for CFEB_L1err check; v20: set RCLK0 to FAST24, CkFB to SLOW6--->rev2: SLOW8
v21: add C-code-err Begin/End to JTAG F20, set CLK40-0 to FAST16, DMBliveErr & In_Time_Out go to BOE_Sta
v22: add DMBLIVE reg's on F25/26, CLK40-1 is FAST16, L1A uses OFD_1; rev2: CLK40's use F16-OFDDR
Good! rev3: tune PDMBLIVE_EN & RST_STRT logic v23: add KillCFEBchecks & require FKILL15 to EnableCheckDisable
Good! v24: tune DMBlive timing (yellow FMM), bring signals to LEDm10/LA0/1
v25: tune L1err & InFerr "DMBliveOK", fix TTMB_Err, tune RstBOE, check CFEB L1A only on 1st sample (not critical
v26: BXorbit=3563 now, add IDMB_FULL flag on ERB. v27: tune CFEB_L1er, 8/16 sample flag, WarnMon & BX offse
v28: add Big debug reg. on F21, Timeout reg. on F28 use LnextFIFO, replace LLLREN w/LFOE for TimeoutReg
make FRA-St/End-TO perm. . v29: fix Mult.L1Err logic, add InSingWarn/InML1Err, tune DDUsyncErr, L1A-fake kills TTC-L1A
v30: tune Critical Error, InRdWarn, SpyOvfl & LextStop logic
v31: tune CFEB-DAV check (OR DAVs from DMB Hdr1 & Hdr2), add SP/TF compatibility & diagnostic logic
v32: add/fix CfebCalDisable default to True, remove DDU_DLL_Err from FMMerr (InRdErr4), modified ERB13 for perm DDU_DLL_err
add DDU CSC-Board occupancy monitor-F34? r2: add zeroing logic at RST for Occ.Mon. -r3: fix LRST logic
v33: change SourceID=760=2F8h for TF-DDU v34: Inverted CCB_CMD bus & L1A **for TF-DDU ONLY!**
v35: Autodetects TF-DDU, now compatible w/wo TF; add SyncHold & CloseL1A logic; r2, removed redundan
RdyIn2 requirement for SEN bits. r3-4, OSyncRst on ~Clk40, tune OFIFO Mon, req. VMEctrv17+ & InCtrlv22r3+
v36: non-TF DDUs have SrcID==BrdID, NoLiveFibers now readout on L1A. r2: change TF_SIG to FDRE, Reset CheckCRC with NewTFDMI
v37: diagnostic changes....Tune DMBL1err(notALCTerr), BadCtrl(notMissTrg), LIE(addMissTrg),
DMB/TMB/ALCTerr account for MissTrgTrail, DMB-to on Era15, XtraTrgTrails on Erc5+13,DDUfmm 3-bits held Reset until SystemRd
v37r2-3: tune CfebL1aErr/SyncErr &DMBcritErr logic, MultL1err logic, InSingWarn=Era10,ValidDMBfull=Erb0,DMBtimeout=Era1
v38: DMBcritErr=Erc7, improve Htmb/alct timing,C-codeErr goes to InMxmitReg, InTimeout goes to EndTimeBusyReg
r2: make DAQovfl for FF case only, include C-CodeErr w/MultXmitErr, CFEBcrc flags Reset on BOE, C-code-L1er=FIFOb15
LDMB_CRCok held at least 4 cycles
r3: add DMB-TO/FIFOfull to TMB/ALCTerr Regs, adjust their time to L2DMBrd; TrgWC only Comp 8 bits, A-T-Switch Req. NoSpwdEr
r4: fix LWCb8 Reset logic for long ALCT case (still not inc. in WC check though)
v39: 64bit_err reset on BOE, TrgWC now uses all 9 bits, CloseL1A range now 1usec, BIG L1Afifo w/better Warn/Busy Logic
r2: add hysteresis for L1A_AF/Busy state, tune DAQovfl logic, tune SysRdy/BUSY logic. r3: tune L1pipe/StuckData logic
-r4: tune CRC_Cnt_Err monitor logic; r5: tune SCAovfl Reset & CountSample timing

To Do:
- COMPARE BXN (DMB/TMB too)
- Watch for TRG buff overflows
- Determine correct values to store in Flash Vers
  ---> BX offset, KillCh's, FIFO thresh, Board ID
- Test DCC/SlinkWait feedback function & thresh's
  ---> Make DMB stop too
- Verify that CFEB-CRC is fixed for B-code case
- No logic for BUS1, DCC SBDATA & TDxxx, 4 LSF, 4 LRL
- Make Verilog module to get Fiber/DMB_RD in one CLK?
- Multiple TRG_L1err ought to request a Sync Reset?
  * Same for consecutive events with a TRG_L1err?
- Check Phase of CMD to CLK40
  * pg. 2G & 3I
- CFEB-DMB sync check pg. 12C
- CFEB-L1A check disabled, pg. 12D: not! Found a fix...
- options for Monitoring on pg. 3H, 12E?
- Does CFEB-Check-Disable cause TF/SP mimic?

TST	Clock	BUFGMUX		
0P	drck1	5P	*4P	TR
2P	2clk	5S	*1S	
3S	clk	7S	*7S	
0S	clk625	2S-	*2S	
7P	ck125	1P	*0S	-BL
5P	clk40	0S	*3P	
4S-	clk156	4S-	*4S	
1S	drck2	3P	*5S	
6S-	sclk	6S-	*6S	

* denotes LOCed position

New Ideas: Store & check DMB source ID's from each fiber?
Feed SLINK status into FMM logic (for UF).
Set DMB CRC OK flag for DDU Empty Events? no...
In case of StuckData send PRST? How to distinguish SEU? Later event still gets LostHdr or Timeout, could self-correct. Add "PRSTed" VME register to track occurrence.
In case of L1Amismatch, let it run and see if it is better a few~10 evts later. Possible to self-correct as above...? Can only work if DMB really lost event data.

Default Startup Order:
Release DLL (no wait)
4) DONE
5) En. Outputs
6) Release WE

CSC_L1Err <--Bring to VME-JTAG Reg?

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BOE1 type L1A Number BXN ID FOV K-Status
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H2: 0x/8000/0001/8000/HHHH
LiveDMB(15) Ostat DMB-DAV(15) BOEstat DMBcnt
H3: 0x/LLLL/oooo/ZZZZ/GGMY

64-bit unique constant
T-2: 0x/8000/FFFF/8000/8000
DDU EOE Status DMBerr DMBwarn(15)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP
EOE WordCount CRCword EOEstat K-Status
TR: 0x/A/?/WW.WWWW/RRRR/UUMK

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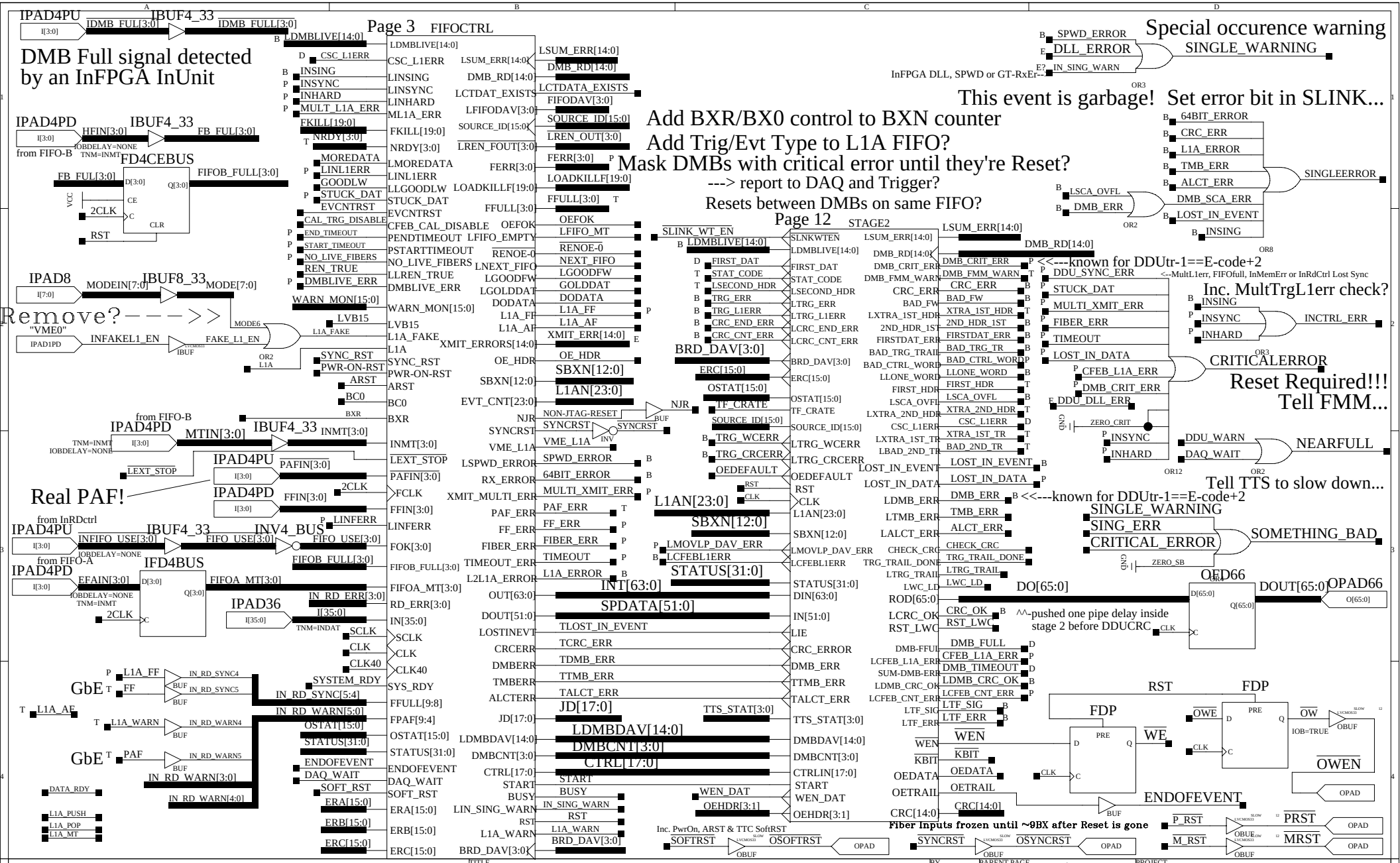
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount _8 TS assumed_

DDU WC, 3 DMB with 1 CFEB (nCFEB=3): 26Ah = 618 dec, 4944 Bytes
DDU WC, 4 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes
DDU WC, 11 DMB with 1 CFEB (nCFEB=11): 8CAh = 2250 dec, 18000 Bytes
DDU WC, 12 DMB with 1 CFEB (nCFEB=12): 996h = 2454 dec, 19632 Bytes
DDU WC, 15 DMB with 1 CFEB (nCFEB=15): BFAh = 3066 dec, 24528 Bytes


DMB Full signal detected by an InFPGA InUnit
Page 3
FIFOCTRL
Special occurence warning
SINGLE_WARNING
InFPGA DLL, SPWD or GT-RxEr
This event is garbage! Set error bit in SLINK...
Add BXR/BX0 control to BXN counter
Add Trig/Evt Type to L1A FIFO?
Mask DMBs with critical error until they're Reset?
---> report to DAQ and Trigger?
Resets between DMBs on same FIFO?
Page 12
STAGE2
<<----known for DDUtr-1==E-code+2
Inc. MultTrgL1err check?
<--MultL1err, FIFOfull, InMemErr or InRdCtrl Lost Sync
CRITICALERROR
Reset Required!!!
Tell FMM...
Tell TTS to slow down...
Real PAF!
Remove?
"VME0"
Fiber Inputs frozen until ~9BX after Reset is gone
^^-pushed one pipe delay inside stage 2 before DDUCRC
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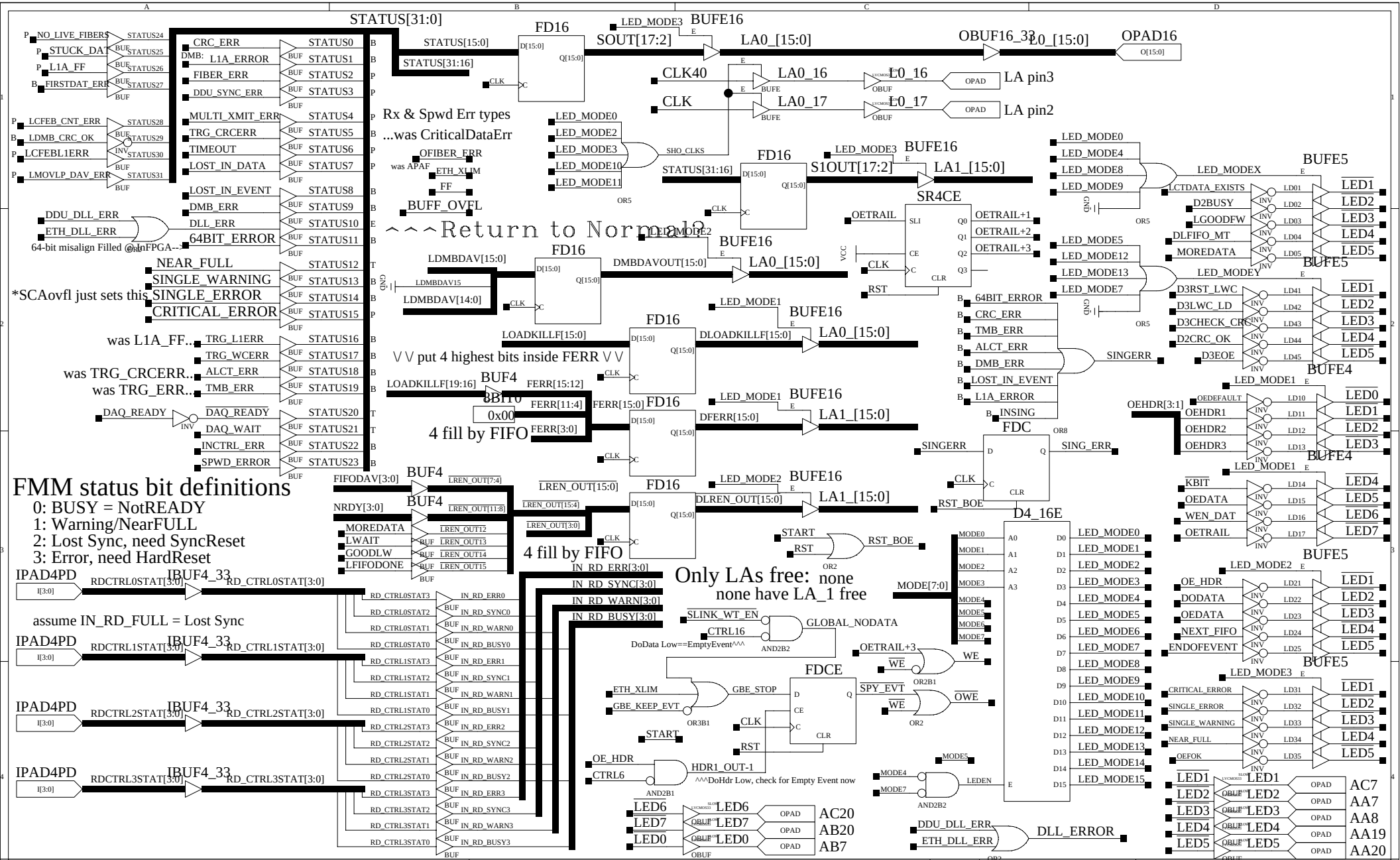
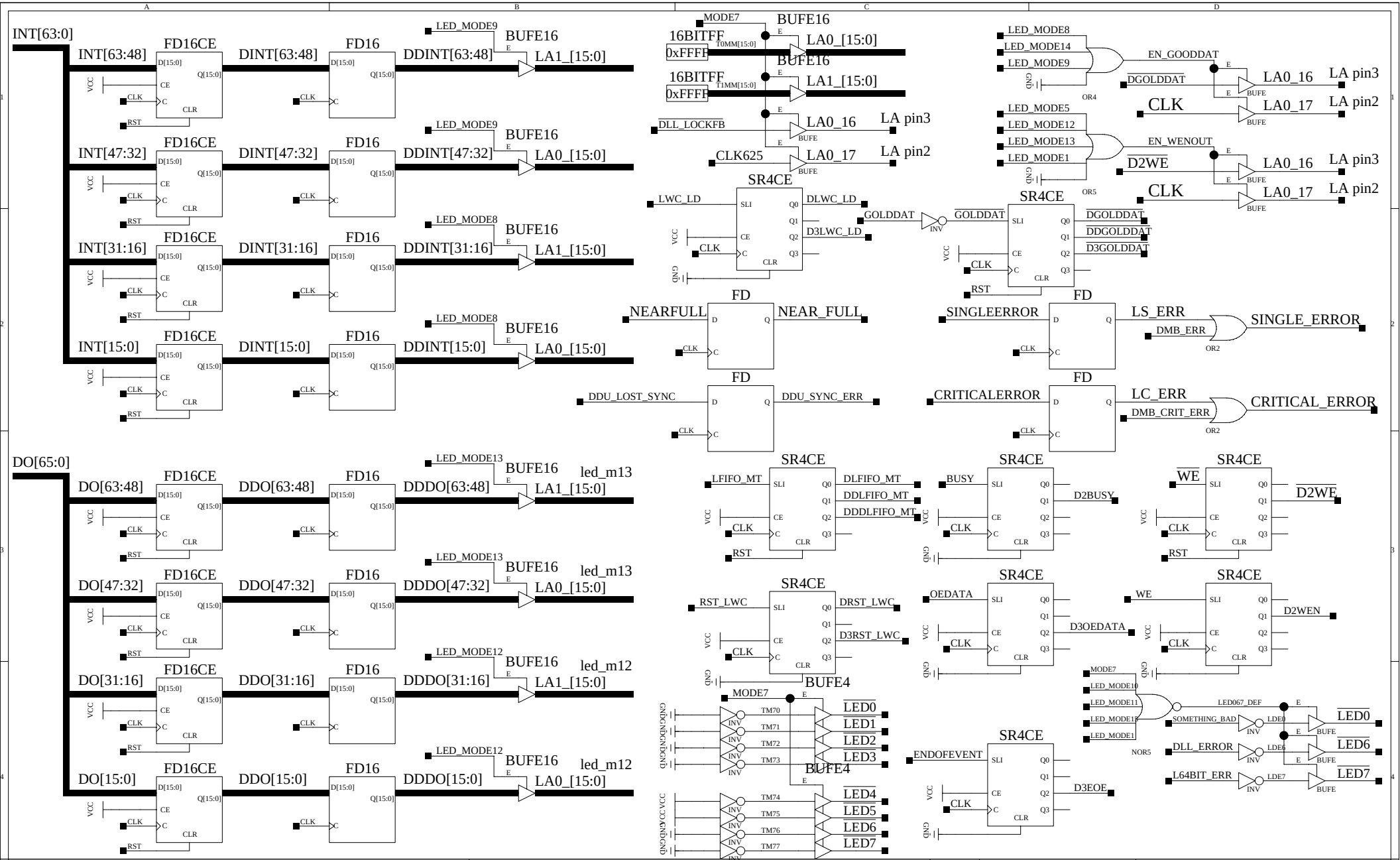
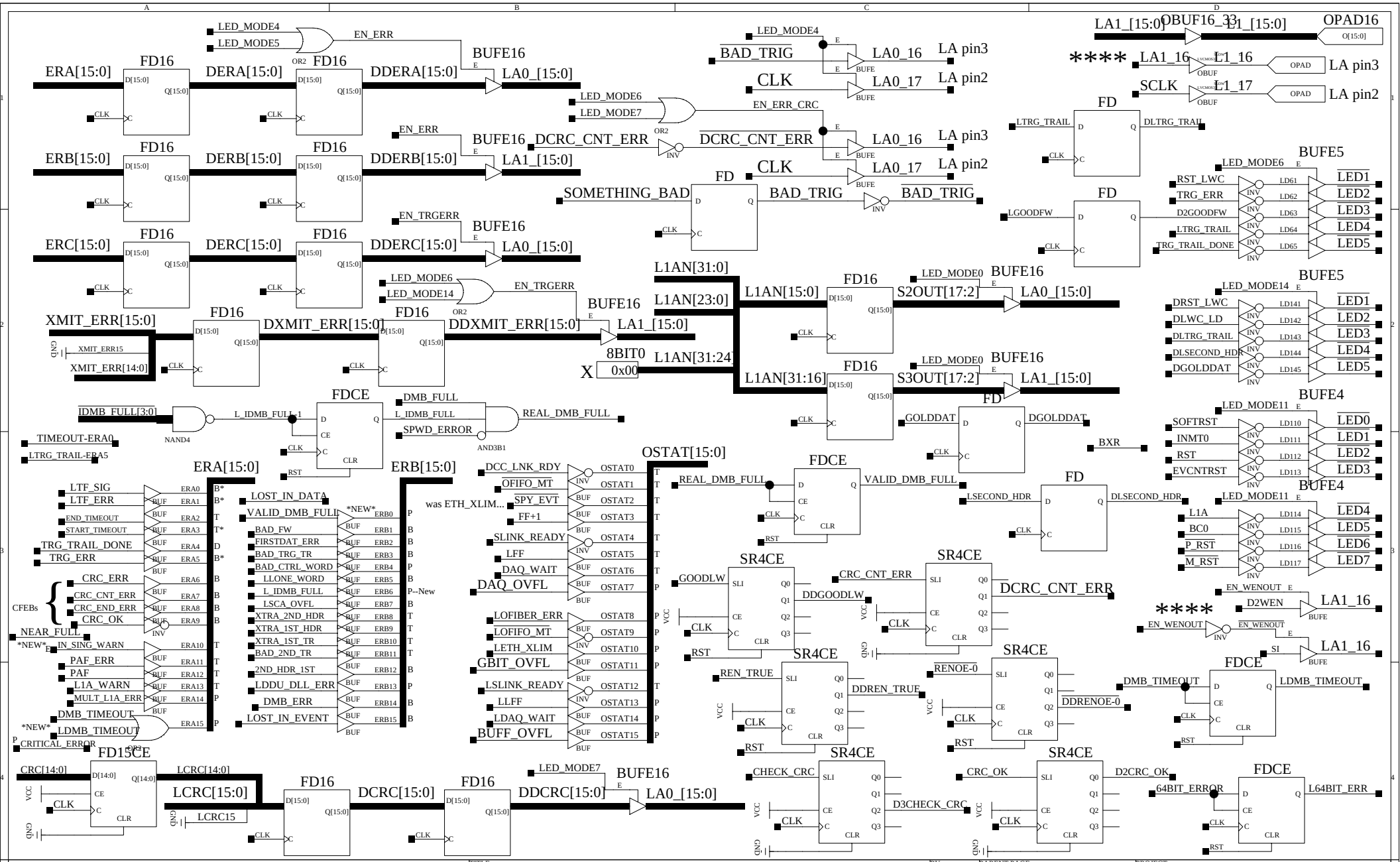
DDU Control
DDU Controller Logic
CMS CSC Electronics
JRG
1
D785C
6-19-2009_14:23
DDUCNTRL . 1
2



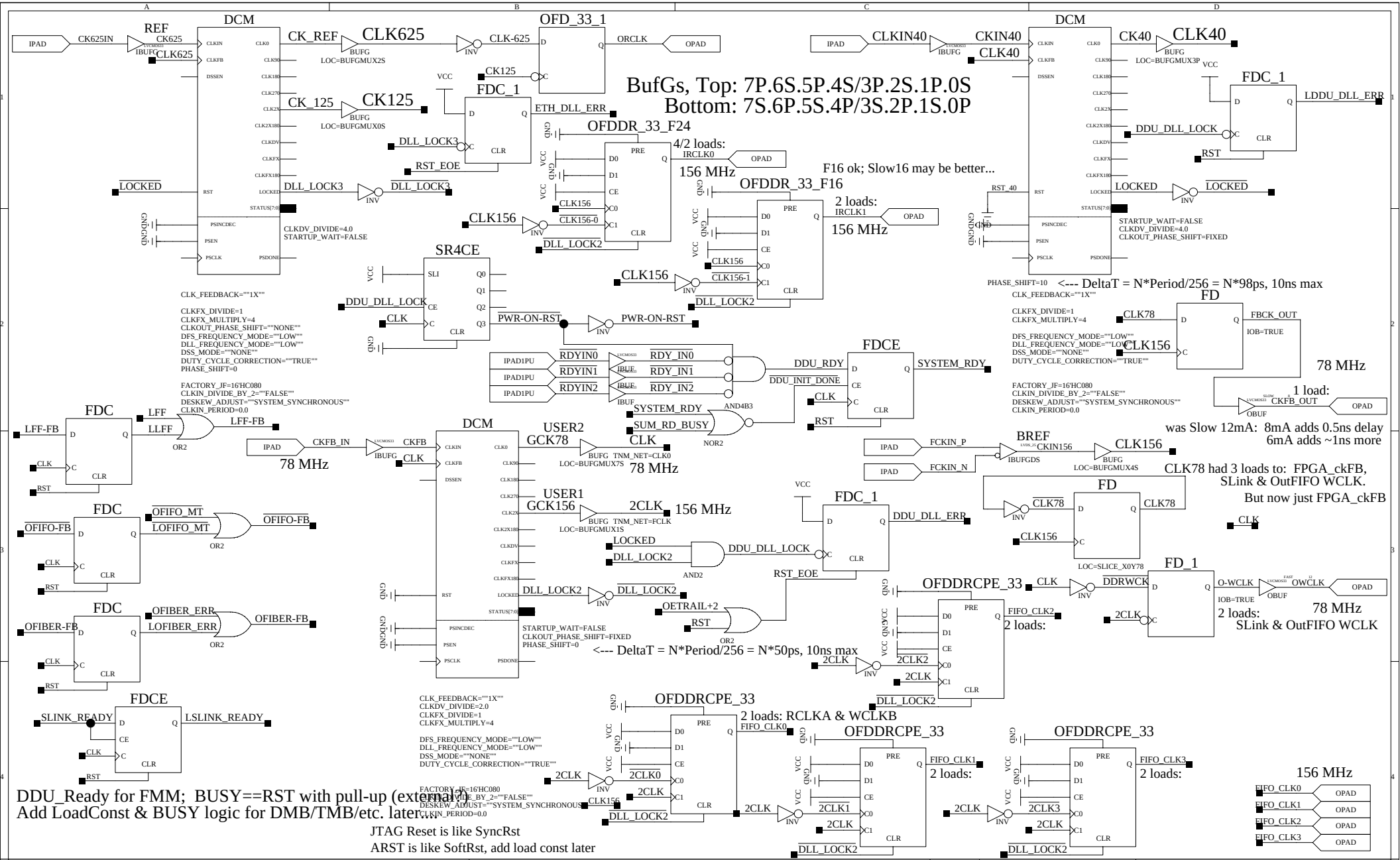
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Control DDU Controller Logic CMS CSC Electronics	BY JRG DATE 6-19-2009_14:26	PARENT PAGE 1 FILE DDUCNTRL . 2	PROJECT D785C PAGE 2A



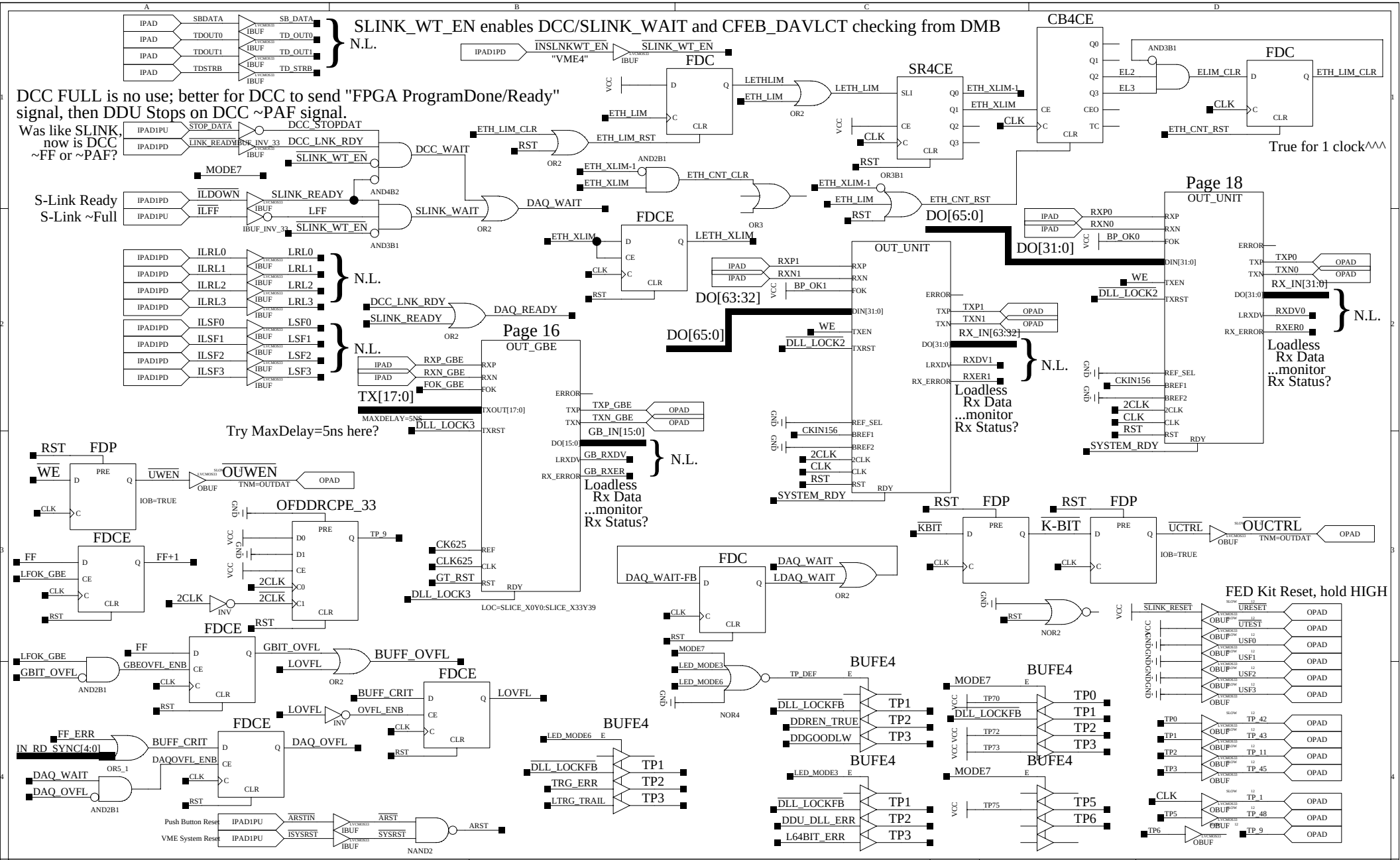
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785C
		DATE: 6-19-2009_14:30	FILE: DDUCNTRL . 3	PAGE: 2B



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 1	PROJECT: D785C
		DATE: 12-8-2006_17:57	FILE: DDUCNTRL . 4	PAGE: 2C



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG PARENT PAGE: 1 DATE: 5-12-2009_14:28	PROJECT: D785C FILE: DDUCNTRL . 5 PAGE: 2D


SLINK_WT_EN enables DCC/SLINK_WAIT and CFEB_DAVLCT checking from DMB
N.L.
DCC FULL is no use; better for DCC to send "FPGA ProgramDone/Ready" signal, then DDU Stops on DCC ~PAF signal.
Was like SLINK, now is DCC ~FF or ~PAF?
S-Link Ready
S-Link ~Full
Page 18
OUT_UNIT
Page 16
OUT_GBE
Loadless Rx Data ...monitor Rx Status?
Try MaxDelay=5ns here?
FED Kit Reset, hold HIGH
True for 1 clock^^^
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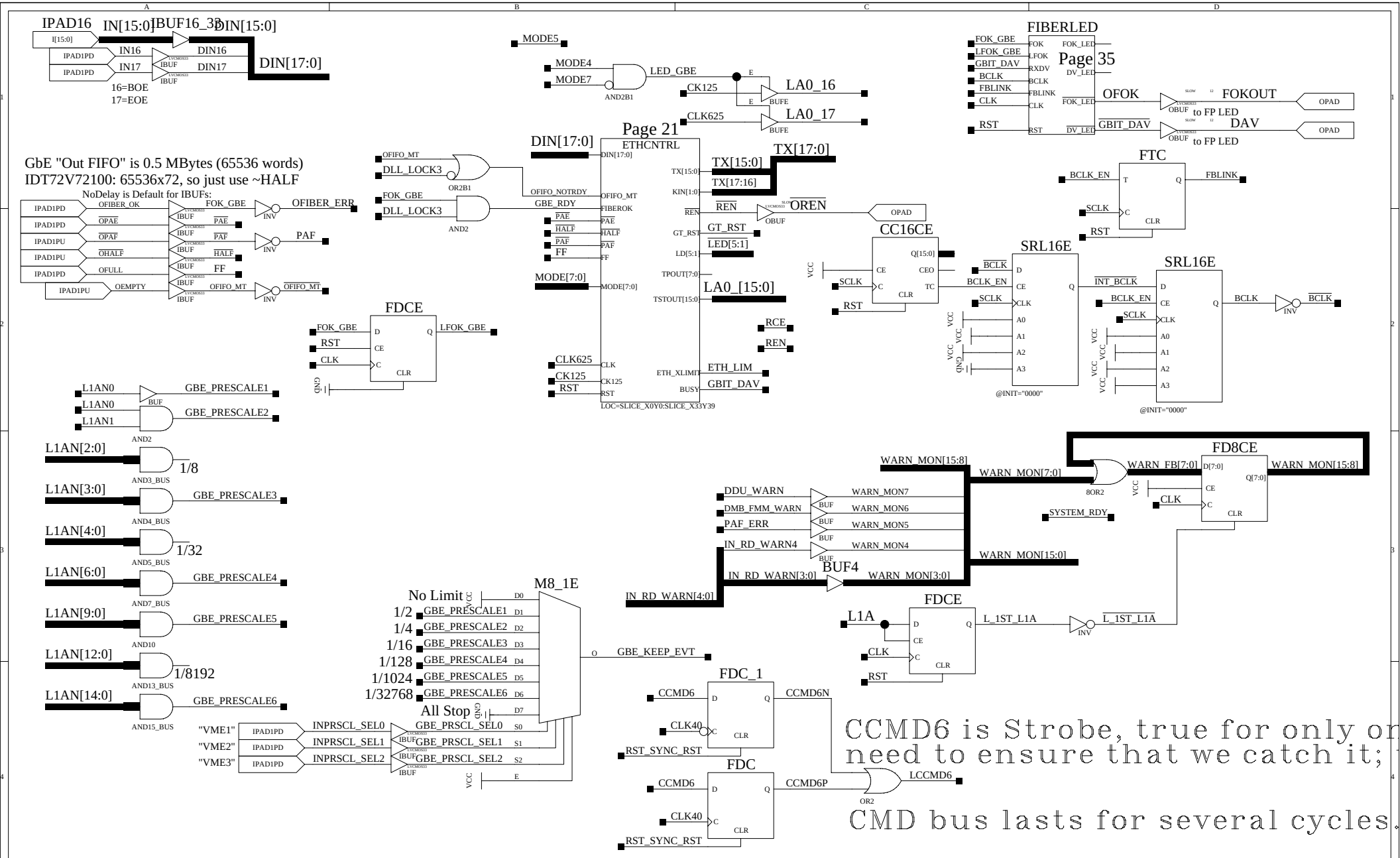
DDU Control
DDU Controller Logic
CMS CSC Electronics
JRG
1
D785C
5-12-2009_14:30
DDUCNTRL . 6
2E



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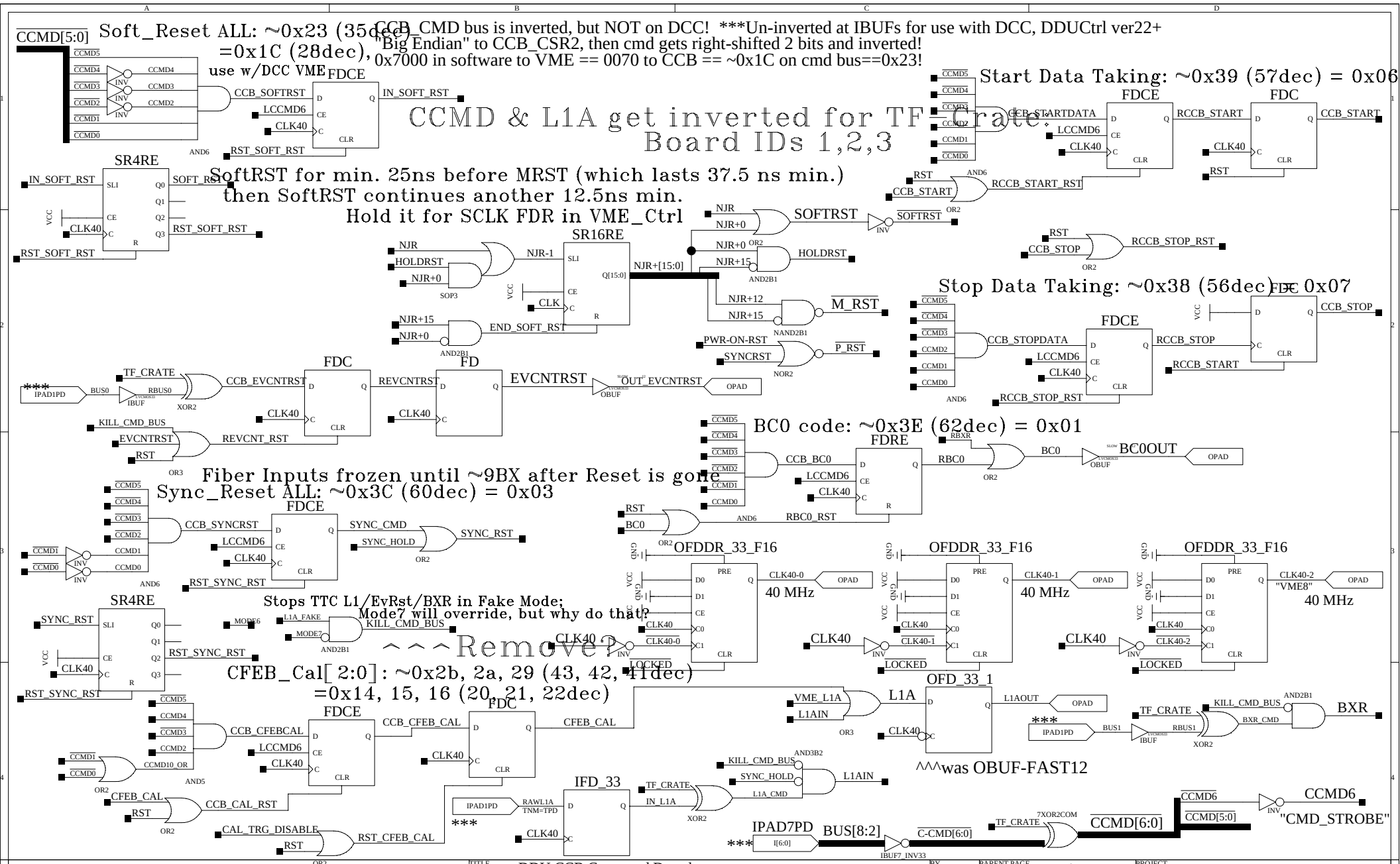
		DATE: 2-21-2008_10:41		FILE: DDUCNTRL . 7	PAGE: 2F


CCMD[5:0]
Soft_Reset ALL: ~0x23 (35dec) =0x1C (28dec), use w/DCC VME
CCB_CMD bus is inverted, but NOT on DCC! ***Un-inverted at IBUFs for use with DCC, DDUCtrl ver22+
"Big Endian" to CCB_CSR2, then cmd gets right-shifted 2 bits and inverted!
0x7000 in software to VME == 0070 to CCB == ~0x1C on cmd bus==0x23!
CCB_SOFTRST
IN_SOFT_RST
RST_SOFT_RST
CCMD & L1A get inverted for TF Crate's
Board IDs 1,2,3
SoftRST for min. 25ns before MRST (which lasts 37.5 ns min.)
then SoftRST continues another 12.5ns min.
Hold it for SCLK FDR in VME_Ctrl
Start Data Taking: ~0x39 (57dec) = 0x06
CCB_STARTDATA
RCCB_START
RCCB_START_RST
Stop Data Taking: ~0x38 (56dec) = 0x07
CCB_STOPDATA
RCCB_STOP
RCCB_STOP_RST
NJR
NJR+0
NJR-1
NJR+[15:0]
NJR+15
NJR+12
HOLDRST
SOFTRST
M_RST
P_RST
END_SOFT_RST
PWR-ON-RST
SYNCRST
TF_CRATE
CCB_EVCNTRST
REVCNTRST
EVCNTRST
OUT_EVCNTRST
KILL_CMD_BUS
EVCNTRST
REVCNT_RST
BC0 code: ~0x3E (62dec) = 0x01
CCB_BC0
RBC0
BC0
BC0OUT
RBC0_RST
Fiber Inputs frozen until ~9BX after Reset is gone
Sync_Reset ALL: ~0x3C (60dec) = 0x03
CCB_SYNCRST
SYNC_CMD
SYNC_HOLD
SYNC_RST
RST_SYNC_RST
Stops TTC L1/EvRst/BXR in Fake Mode;
Mode7 will override, but why do that?
L1A_FAKE
MODE6
MODE7
KILL_CMD_BUS
CLK40 ?
^^^Remove?
CFEB_Cal[2:0]: ~0x2b, 2a, 29 (43, 42, 41dec)
=0x14, 15, 16 (20, 21, 22dec)
CCB_CFEBCAL
CCB_CFEB_CAL
CFEB_CAL
CCMD10_OR
CFEB_CAL_RST
CAL_TRG_DISABLE
RST_CFEB_CAL
IPAD1PD
RAWL1A
TNM=TPD
IFD_33
IN_L1A
L1A_CMD
L1AIN
VME_L1A
L1A
L1AOUT
OFD_33_1
^^^was OBUF-FAST12
BXR
BXR_CMD
IPAD7PD
BUS[8:2]
C-CMD[6:0]
7XOR2COM
CCMD6
"CMD_STROBE"
OFDDR_33_F16
CLK40-0
CLK40-1
CLK40-2
"VME8"
40 MHz
LOCKED
FDCE
FDC
FD
FDRE
SR4RE
SR16RE
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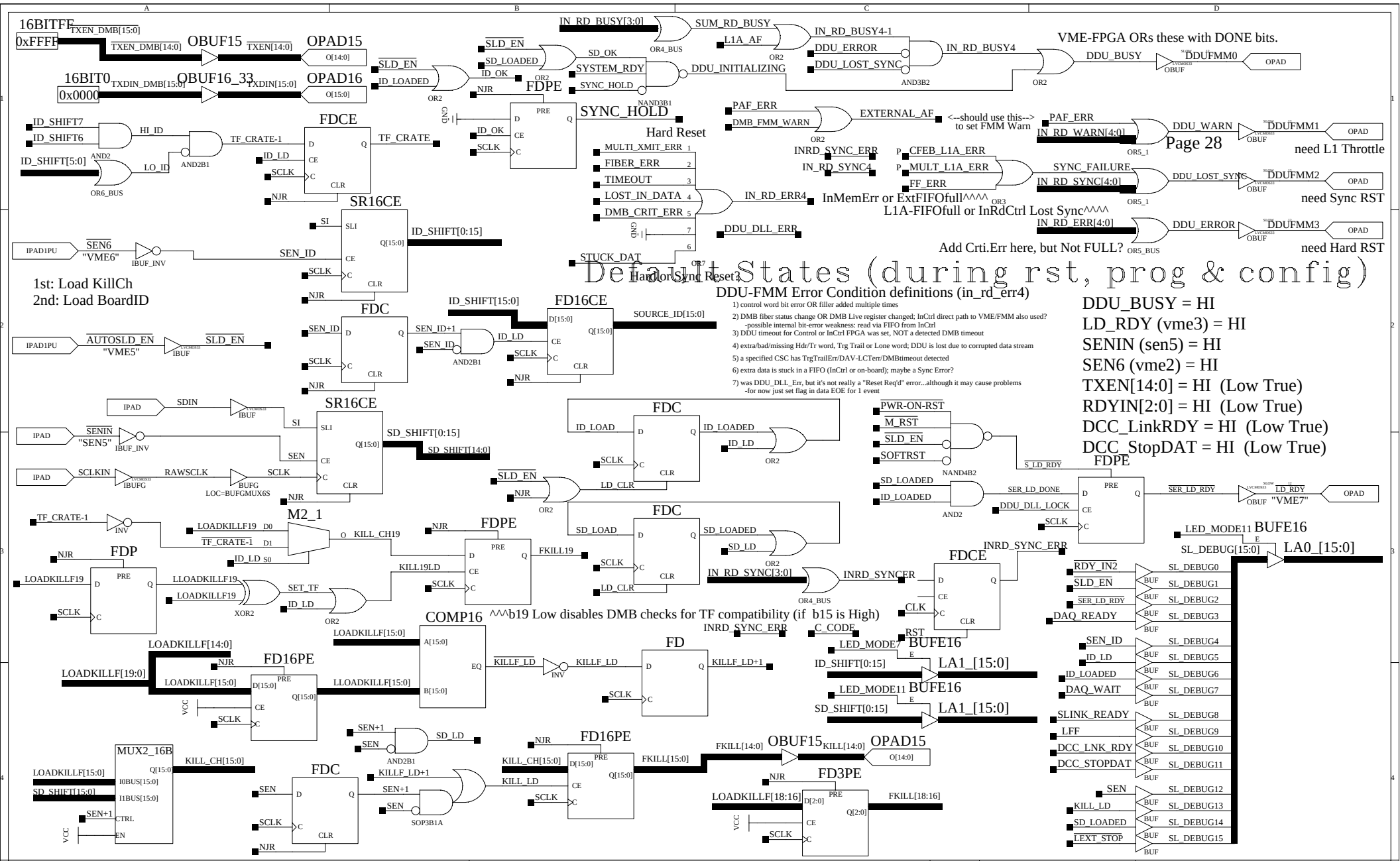
TITLE
DDU CCB Command Decode
DDU Controller Logic
CMS CSC Electronics
BY
JRG
PARENT PAGE
1
PROJECT
D785C
DATE
2-21-2008_10:39
FILE
DDUCNTRL . 8
PAGE
2G



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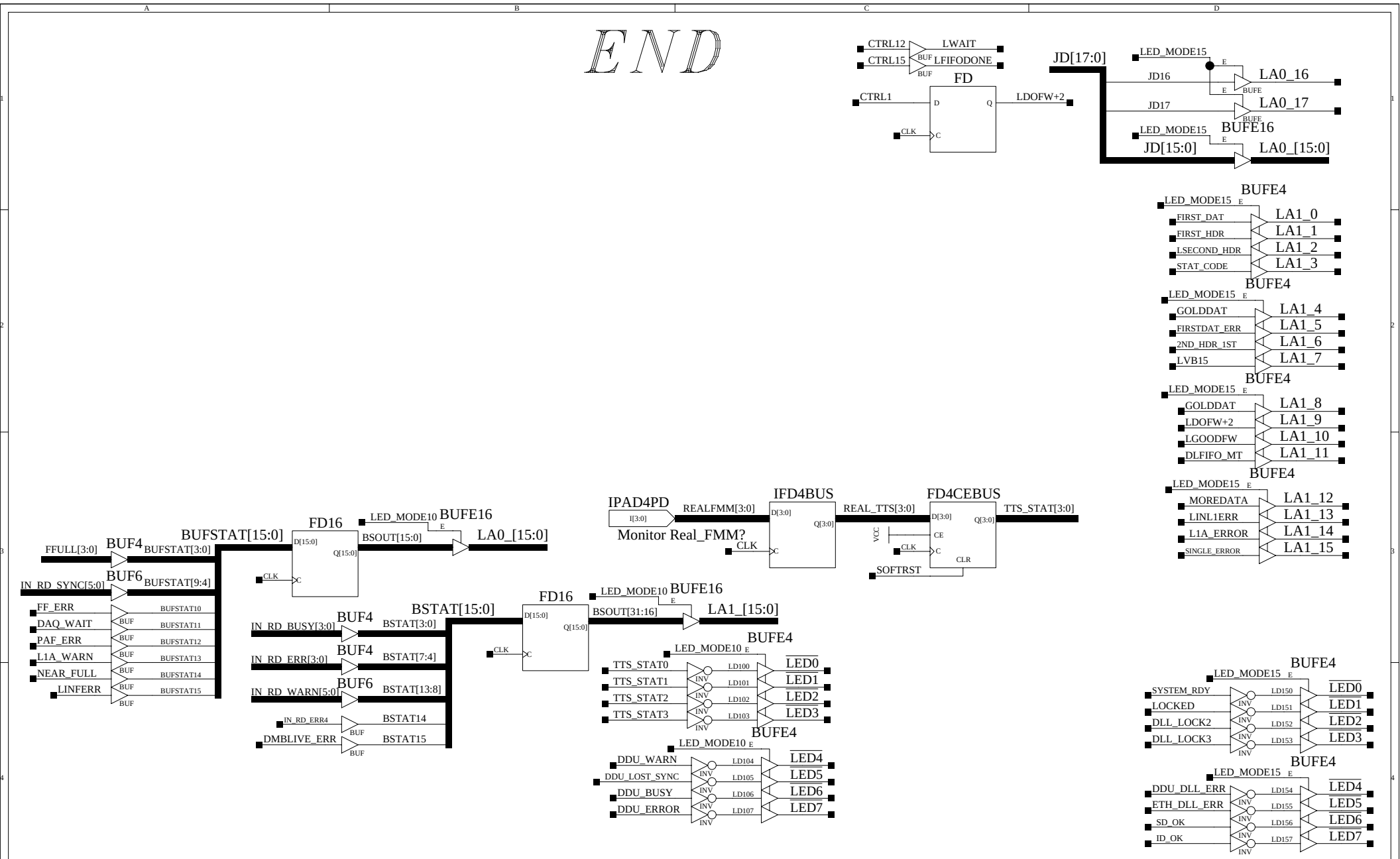
TITLE: DDU Control
DDU Controller Logic
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	1	D785C
DATE	FILE	PAGE
11-7-2008_17:10	DDUCNTRL . 9	2H



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TITLE: DDU Control
DDU Controller Logic
CMS CSC Electronics

BY: JRG
PARENT PAGE: 1
PROJECT: D785C
DATE: 10-30-2006_16:38
FILE: DDUCNTRL . 10
PAGE: 2I

From here on DAT16,53 are only used with C-Codes. But DAT17,52 are always DMBend,Filler. DAT70,71 are never used.

CLK/\ -- DIN[35:0] -- CLK\/ -- Q[35:0] DIN[71:36] -- CLK/\ -- Q[71:36] QS[35:0]

Use these busses for CFEB CRC and Special Word checks-->>

DAT[71:0]

DAT[12:0] BUF13 DOUT[12:0]

DAT[30:18] BUF13 DOUT[25:13]

DAT[48:36] BUF13 DOUT[38:26]

DAT[66:54] BUF13 DOUT[51:39]

DOUT[51:0]

4 * 13-bit SCA data bus

DAT[11:0] BUF12 L1AN[11:0]

DAT[29:18] BUF12 L1AN[23:12]

L1AN[23:0]

L1AN[15:0]

L1AN[23:16]

FD4CE next-to-last word on DAT (last DMB E-codes)

LW D0 Q0 LGOODLW

OLW1 D1 Q1 OLGOODLW1

OLW2 D2 Q2 OLGOODLW2

OLW3 D3 Q3 OLGOODLW3

GND GND GND

LREN_TRUE CE

CLK C

RST CLR

} N.L.

RDAT35 RDAT34 RDAT33 RDAT32 NODAT

NAND4

DAT 34=Hdr, 35=Tr. 70/71 not used

Trail, Hdr & C-code == NoData

SOURCE_ID[15:0]

CSC_L1ERR

L1AMISMATCH+1

GOOD_L1A+1

SOP3

EVT_L1ERR

FDCE D Q CE C CLR

LEVT_L1ERR

L1 Error

CLK

RST_BOE

ADD4_BUS

GND CI

DCNT[3:0] A[3:0]

DMBCNT[3:0] B[3:0]

S[3:0] DMCNT[3:0]

CO OFL

DAQ_WAIT

Use NEW DMB logic here (old L1AN was [51:40] & [31:20])

FD4CEBUS D[3:0] Q[3:0] CE C CLR

DMBCNT[3:0]

LOADFDAV

CLK

RST_EOE

FOE_REN[3:0]

FOE_REN2 FOE_REN3 OR2 FOE_B1

FOE_REN1 OR2 FOE_B0

Lowest 36 RDAT bits synched to falling edge of CLK

IFDDR36C

IN[35:0] D[35:0] Q[71:0] QS[71:0] CLK C CLR RST

RDAT[71:0] (next-to-last word bits) comes with E-codes of last DMB only, followed by C-codes

DAT[71:0]

Page 5

OEFOK RDAT35 RDAT34 LW

Trail & noHdr == Trail C-Code

EVT_ML1ERR

FDCE D Q CE C CLR

LEVT_ML1ERR

N.L.

CLK

RST

INMT[3:0]

LEXT_STOP

RST

OR2B1

SET_LFIFO_EMPTY

TIG

FDS

M4E_BUS

WCGE2F[3:0] D[3:0] O FIFO_EMPTY TIG

FOE_B0 S0

FOE_B1 S1

VCC E

D S Q LFIFO_EMPTY TIG

synched w/DoFW+1,2

CLK C

^^^only for debug/LEDs^^^

OEFOK DAT16 AND3B1 IN_MULTL1A N.L.

In_ML1A done on p.3b

OEFOK DAT52 AND2 RX_ERR "FILL Flag"

GND RXER1 N.L.

LLLREN[3:0]

L1ERRORS[3:0]

4AND2 PATH_L1ER[3:0] OR4_BUS PREV_PATH_L1ER

L2DMB_RD[14:0]

CSC_L1ER[14:0]

15AND2 PREV_L1ER[14:0] OR15 PREV_CSC_L1ER

DAT[15:0] BUF16 OUT[15:0]

DAT[33:18] BUF16 OUT[31:16]

DAT[51:36] BUF16 OUT[47:32]

DAT[69:54] BUF16 OUT[63:48]

OUT[63:0]

GND OUT38 OUT37 OUT36 BUF DCNT3 DCNT2 DCNT1 DCNT0 DCNT[3:0]

OUT39 BUF INL1ERR

DMBLIVE_ERR

LINFERR FIFO_CHG OR3 FIBER_ERR

EMPTYF[3:0] OR4_BUS ONE_NOT_MT TIG

only for CloseL1A/StuckData correction^^^

FEND appears at end: sometimes was never

DAT17 DAT53 BUF FEND0

OLD_FEND1 should be always zero

GND FEND1

set for first 2 E-codes from each DMB

EVT_CNT[23:0]

COMP16 A[15:0] B[15:0] EQ

EVT_CNT[15:0]

L1AN[15:0]

INL1ERR COMP_EV0 COMP_EV1 OR3B2 L1A_MISMATCH

FD D Q CLK C

L1AMISMATCH+1

CB16CE Q[15:0] CE CEO C TC CLR

EVT_CNT[15:0]

START CLK

EVCNTRST RST OR2 RST_EVCNT

COMP8 A[7:0] B[7:0] EQ

EVT_CNT[23:16]

L1AN[23:16]

CB8CE Q[7:0] CE CEO C TC CLR

EVT_CNT[23:16]

PREV_PATH_L1ER L1ERR_LD PREV_CSC_L1ER CSC_L1ER SOP4 ACC_ML1ERR

LEVT_L1ER EVT_L1ER AND2 EVT_ML1ER IN_ML1A_ERR OR3 MULTL1AERR

L1 Error

CLK

FDCE

SYS_RDY D Q CE C CLR IN_RDY

RST

WCGE2F[3:0]

INMT[3:0]

PAFIN[3:0]

FFIN[3:0]

FOK[3:0]

FIFO_RDY

WCGE2F[3:0] MTIN[3:0] IN_RDY PAFIN[3:0] FFIN[3:0] FIBEROK[3:0] START_TIMEOUT END_TIMEOUT RST CLK

EMPTY[3:0] DATA_READY NOT_READY ONE_RDY RDY[3:0] NOTRDY[3:0] LFOK[3:0] MT[3:0] FERR[3:0] FPAF[3:0] FFUL[3:0] PAF_ERROR FF_ERROR FIBER_CHANGE

EMPTYF[3:0] DATA_RDY NOT_RDY ONE_RDY RDY[3:0] N.L. NRDY[3:0] LFOK[3:0] MT[3:0] F_ERR[3:0] FPAF[3:0] FFULL[3:0] PAF_ERR FFERR FIFO_CHG

Page 4

Valid E-Code detected

FDCE

MULTL1AERR D Q CE C CLR ML1A_ERR

CLK

RST

CSC_L1ERR TMBERR ALCTERR AND3B2 DMB_L1ERR L1A_MISMATCH OR3 L1A_ERROR

DOFW+2 GOLDDAT AND2 GOOD_L1A

FDCE D Q CE C CLR

L1 Error

CLK

RST_BOE

(exclude DMB_Err case?)

PREV_CSC_L1ER CSC_L1ER AND2 CSC_MULTL1AERR N.L.

GOLDDAT FEND0 FEND1 SOP4 DMB_END

FDC D Q CLK C CLR

RST

DMB_END+1

DMB_END=DMBEND =Ecode

START_TIMEOUT

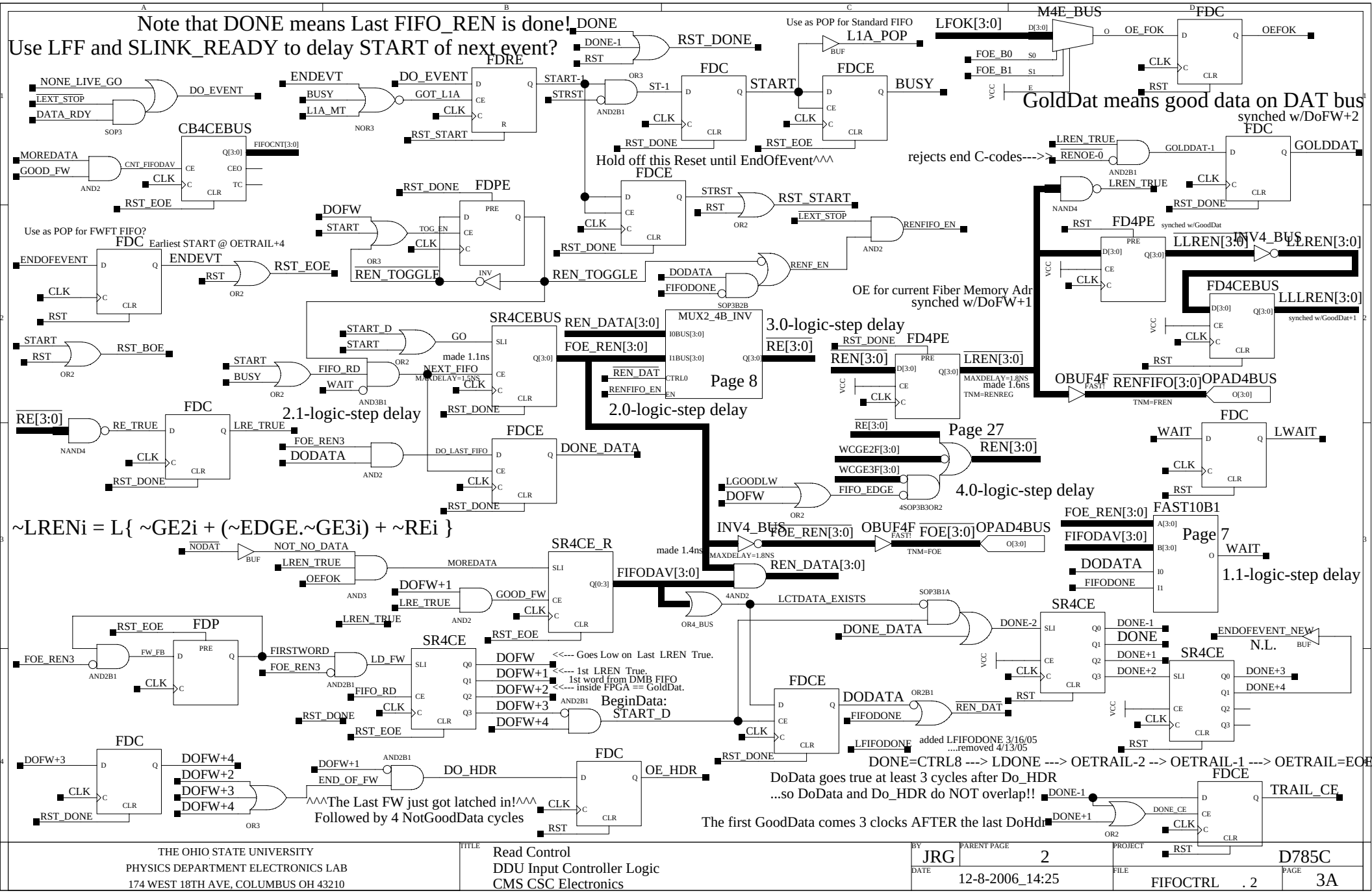
END_TIMEOUT

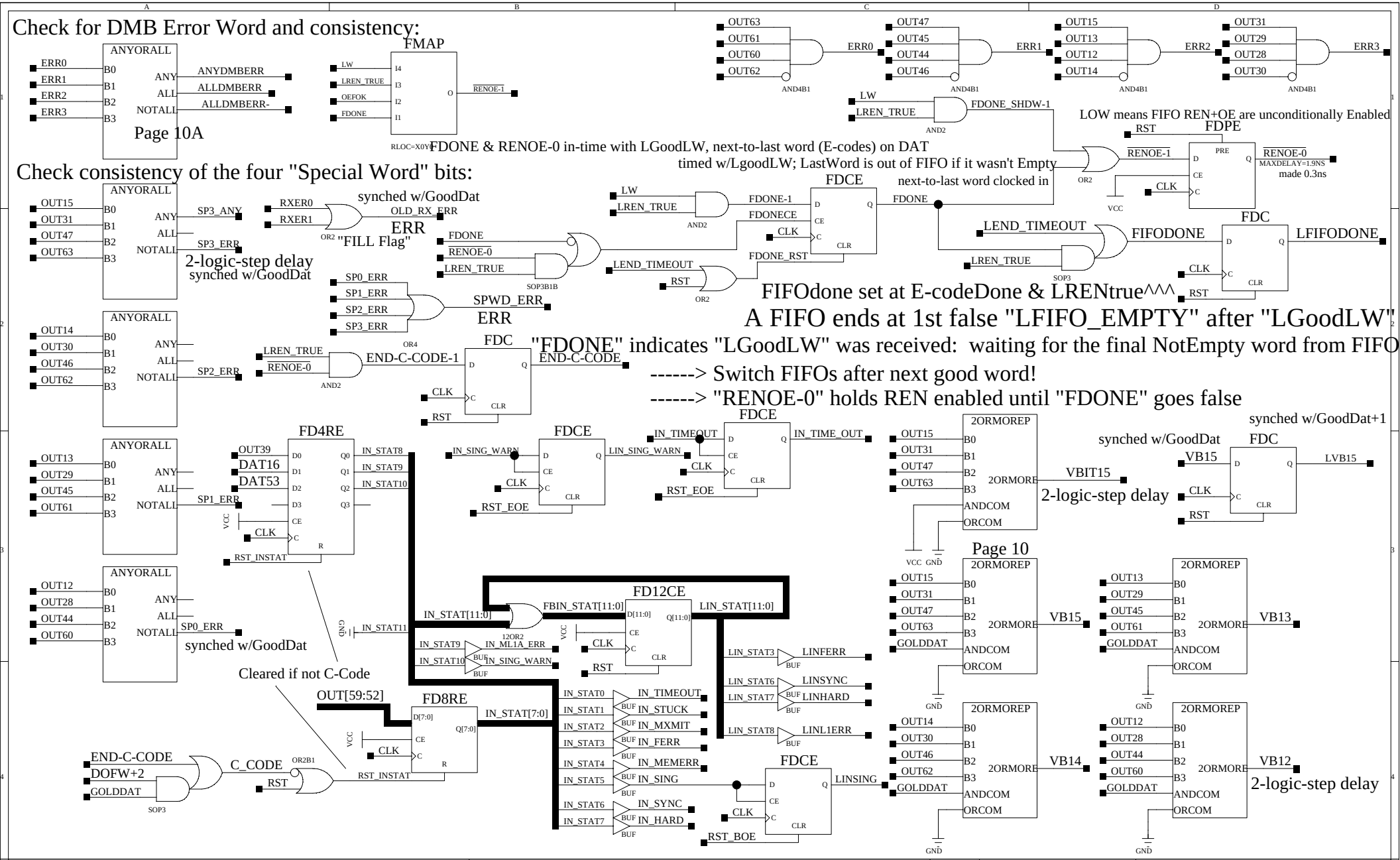
RST

CLK

LFOK[3:0] OR4_BUS SOME_FIBERS_OK INV NO_LIVE_FIBERS

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 2
		DATE 6-19-2009_13:50	PROJECT D785C
		FILE FIFOCTRL . 1	PAGE 3


Note that DONE means Last FIFO_REN is done!
Use LFF and SLINK_READY to delay START of next event?
GoldDat means good data on DAT bus
synched w/DoFW+2
Hold off this Reset until EndOfEvent^^^
rejects end C-codes--->
Use as POP for FWFT FIFO?
Earliest START @ OETRAIL+4
Use as POP for Standard FIFO
OE for current Fiber Memory Adr
synched w/DoFW+1
3.0-logic-step delay
2.0-logic-step delay
2.1-logic-step delay
4.0-logic-step delay
1.1-logic-step delay
Page 8
Page 27
Page 7
made 1.1ns
made 1.6ns
made 1.4ns
~LRENi = L{ ~GE2i + (~EDGE.~GE3i) + ~REi }
<<--- Goes Low on Last LRENTrue.
<<--- 1st LRENTrue.
1st word from DMB FIFO
<<--- inside FPGA == GoldDat.
BeginData:
START_D
^^^The Last FW just got latched in!^^^
Followed by 4 NotGoodData cycles
DONE=CTRL8 ---> LDONE ---> OETRAIL-2 --> OETRAIL-1 ---> OETRAIL=EOE
DoData goes true at least 3 cycles after Do_HDR
...so DoData and Do_HDR do NOT overlap!!
The first GoodData comes 3 clocks AFTER the last DoHdr
added LFIFODONE 3/16/05
....removed 4/13/05
N.L.
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
Read Control
DDU Input Controller Logic
CMS CSC Electronics
BY JRG
PARENT PAGE 2
PROJECT D785C
DATE 12-8-2006_14:25
FILE FIFOCTRL . 2
PAGE 3A

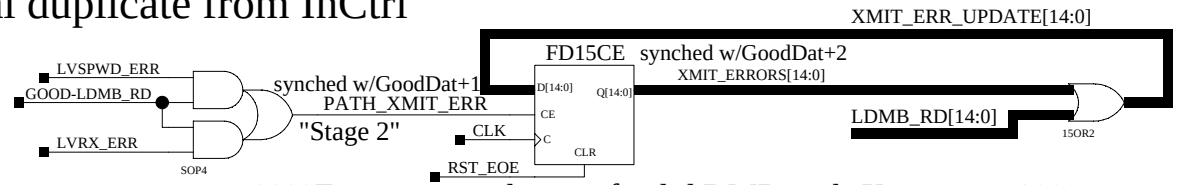


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Read Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG PARENT PAGE: 2 DATE: 11-27-2007_9:58	PROJECT: D785C FILE: FIFOCTRL . 3 PAGE: 3B

Control Bit List:

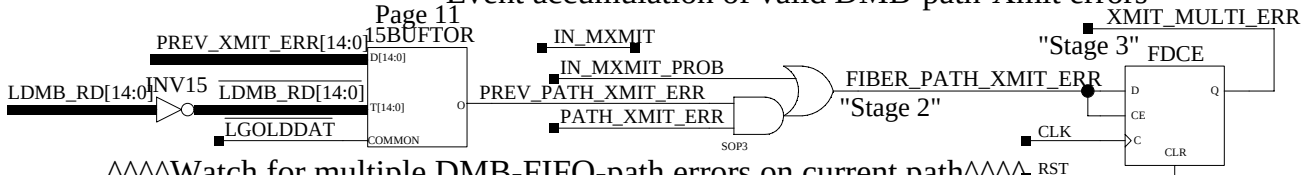
0: Gold Data (Active DMB has REN, OE, notMT, LFOK)
1: DMB First Word Mode
2: Latched Voted Special Bit 12 {2 or more out of 4}
3: Latched Voted Special Bit 13 {2 or more out of 4}
4: Latched Voted Special Bit 14 {2 or more out of 4}
5: Latched Voted Special Bit 15 {2 or more out of 4}
6: Do Header Mode (Header to Output)
7: Word Count Enable (DDU Header, DMB Data)
8: End of Event (DONE--->OETrail)

Virtual duplicate from InCtrl

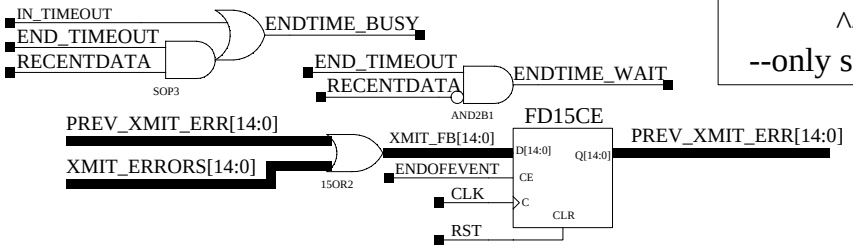


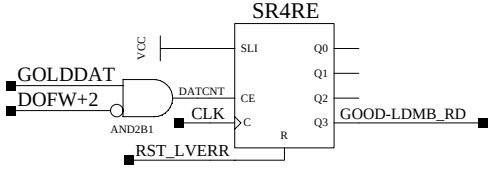
^^^^Event accumulation of valid DMB-path-Xmit errors^^^^

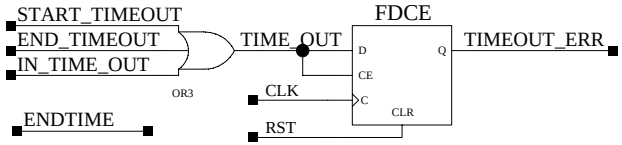
Page 11



^^^^Watch for multiple DMB-FIFO-path errors on current path^^^^
--only sets errors for separate-event case or InMultXmit case



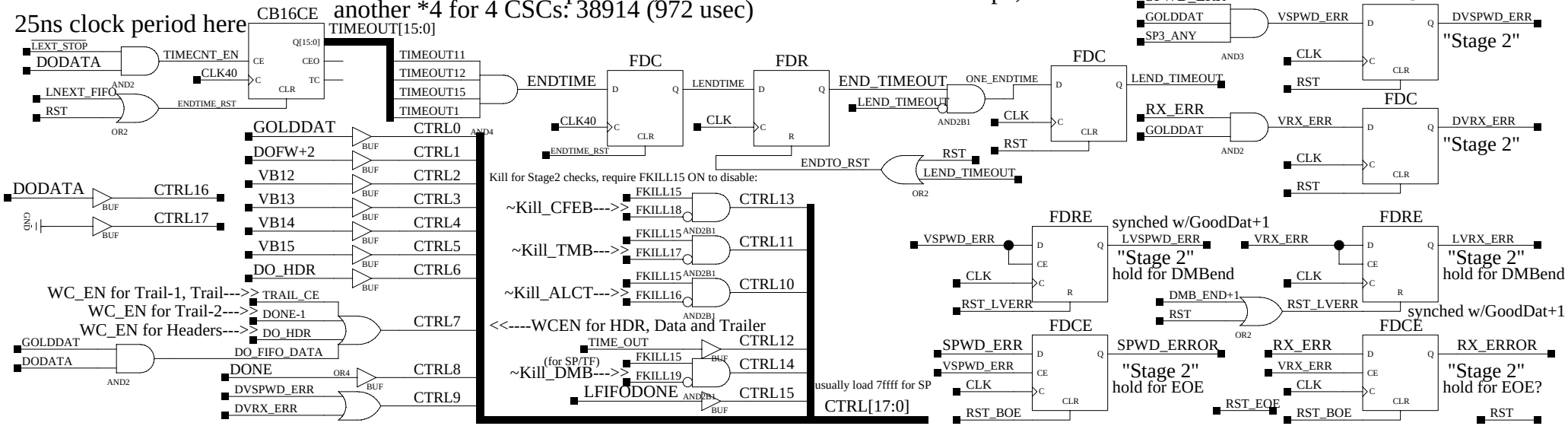




^^^^Permanent accumulation of DMB-path-Xmit errors^^^^

FIFO Done Timeout: 132 usec=5281 is the worst case per CSC, add about 100 usec w/TMB scope, then another *4 for 4 CSCs: 38914 (972 usec)

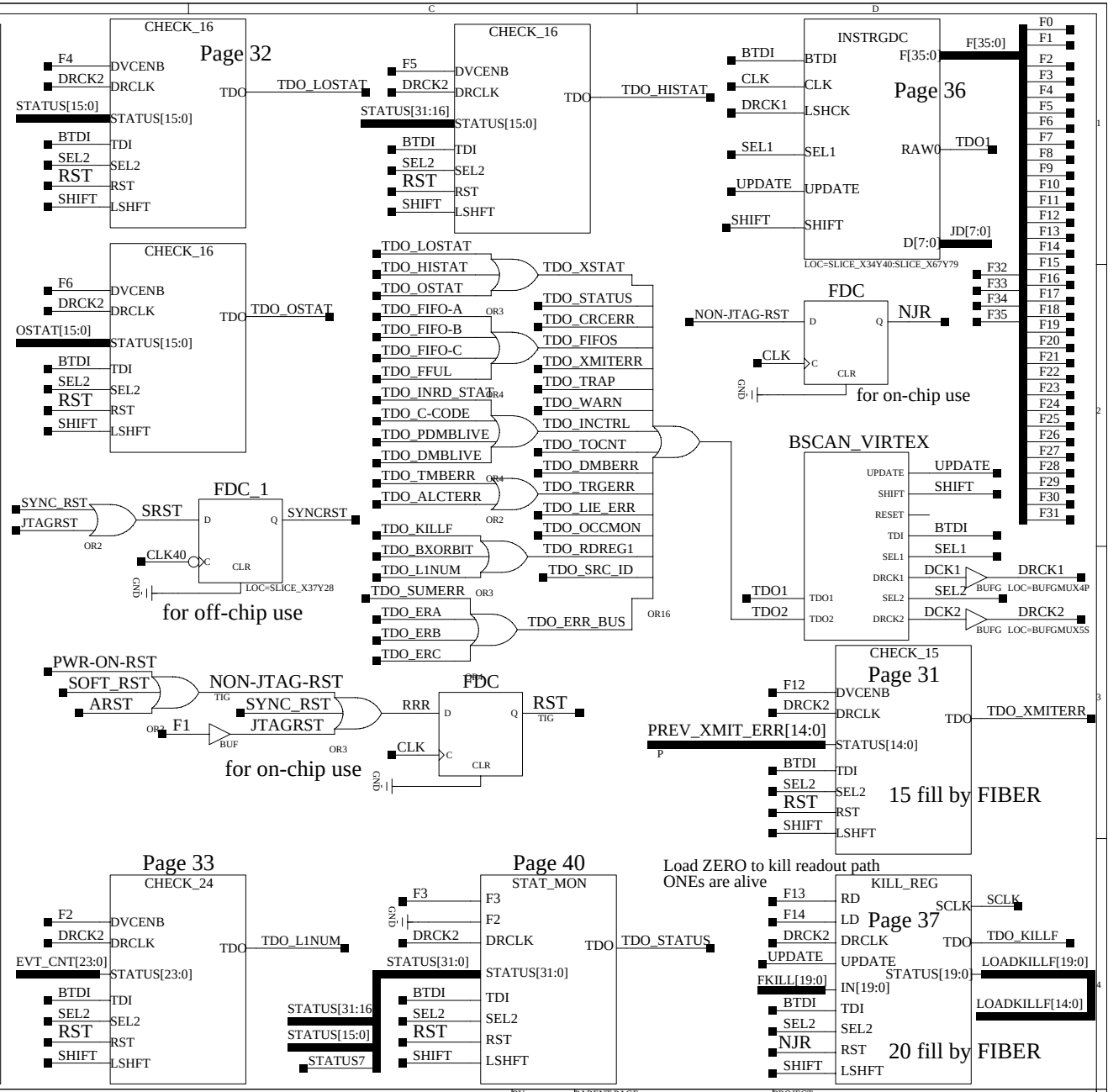
25ns clock period here



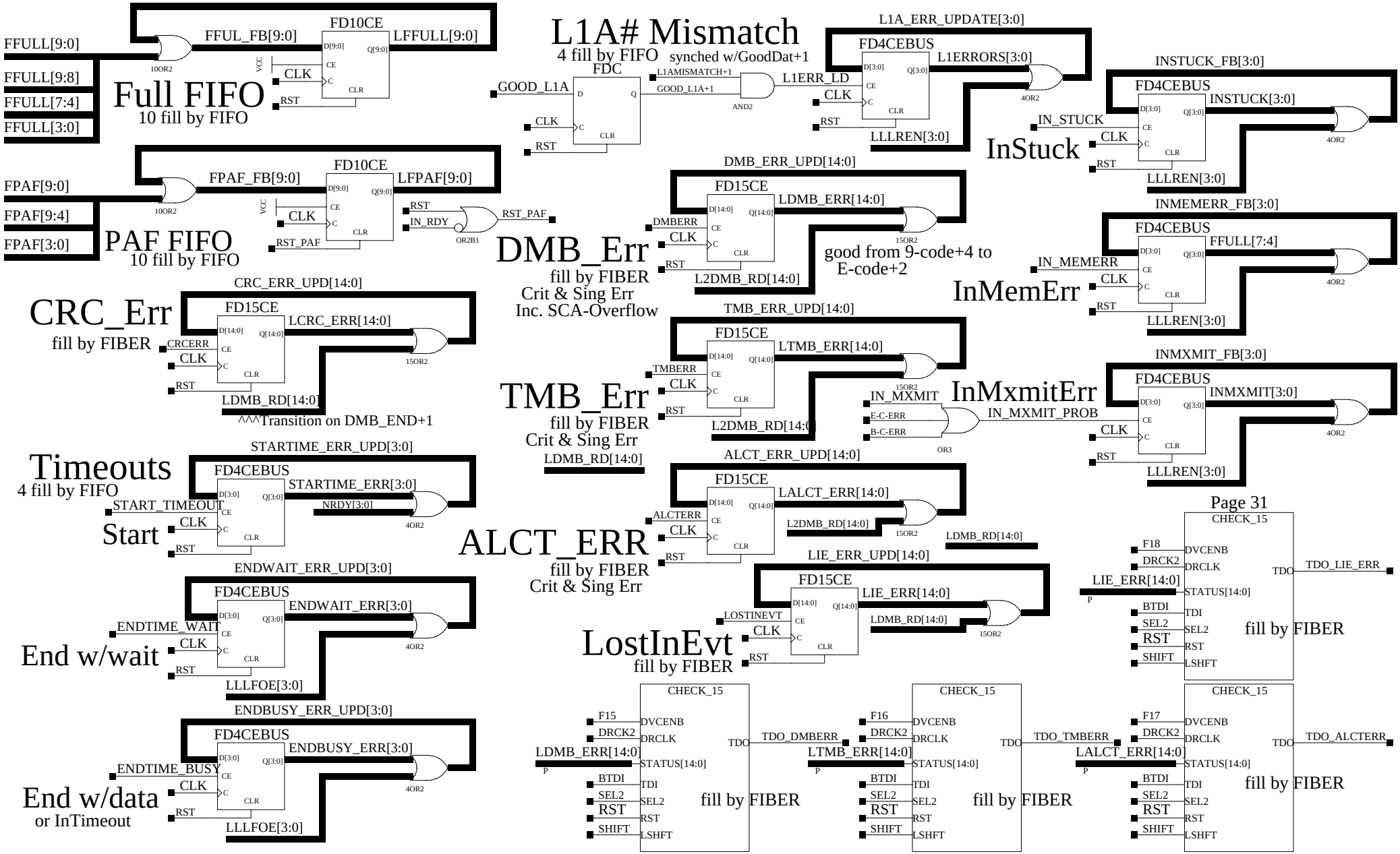
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 6-19-2009_13:50	FILE: FIFOCTRL . 4	PAGE: 3C

JTAG Instruction Decode

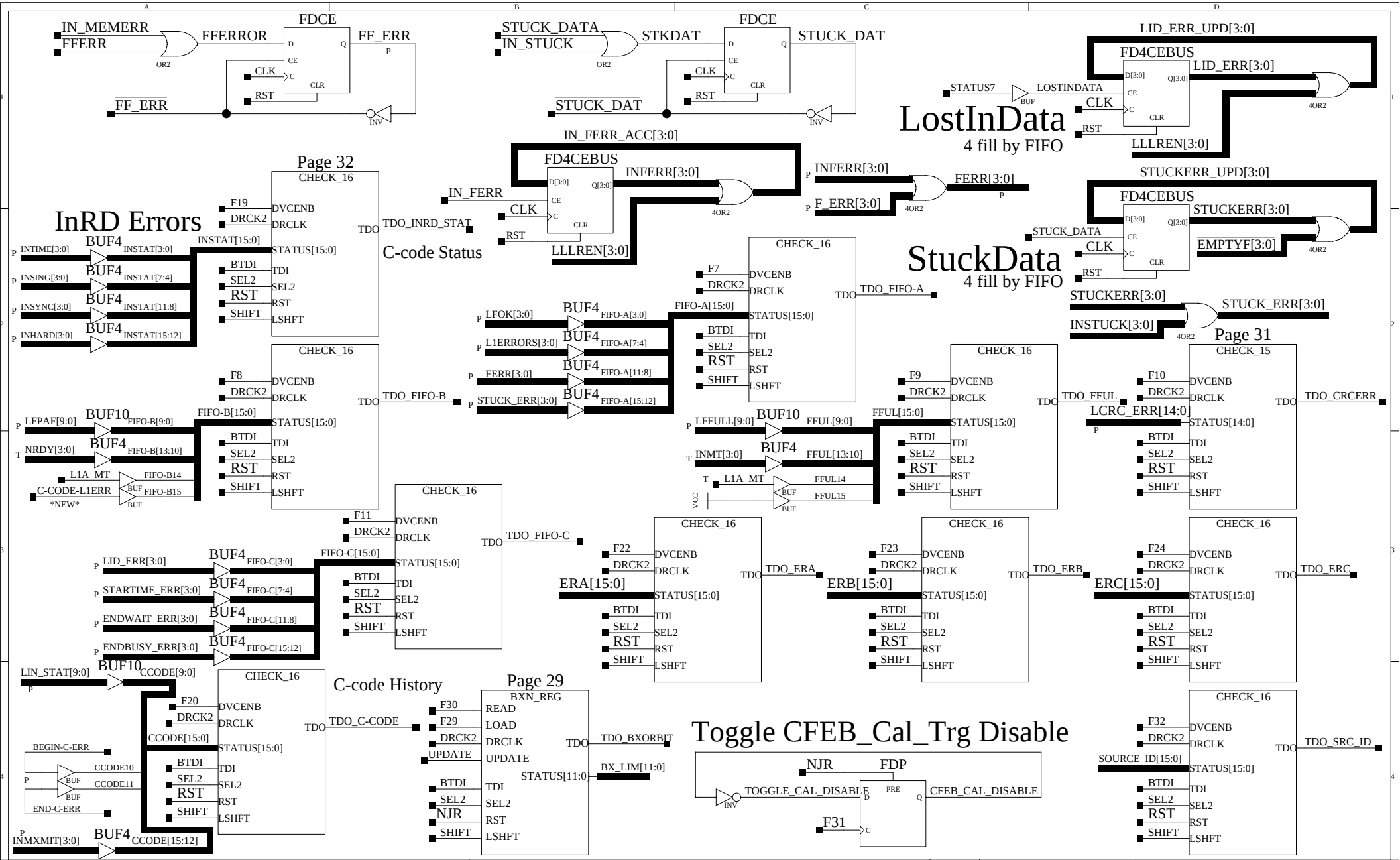
OpCode	Function [OpName]	
0	No Operation [NOOP]	
1	FPGA Reset [toggle]	
2	Read Current DDU L1A Number (24-bit scaler)	
3	Check status (capture and shift) [32 bits]	
4	Check status, low-word [16 bits]	
5	Check status, high-word [16 bits]	
6	Output Path Status [16-bits]	
7a	Check FOK (active input FIFOs) [lowest 4 bits]	
7b	L1A Mismatch (FIFO headers) [4-bits]	check FIFO-A
7c	Check FIFO Err (active FIFO change) [4 bits]	
7d	Stuck Data Errors (input FIFOs) [highest 4-bits]	
8a	Almost Full FIFOs [lowest 10-bits]	check FIFO-B
8b	FIFO Empty/GE2 Status [highest 6-bits]	
9a	Full FIFOs [lowest 10-bits]	FIFO Full/MT (raw)
* 9b	Raw FIFO Empty [highest 6-bits]	
10	CRC Errors [15-bits]	
11a	Lost In Data [lowest 4-bits]	check FIFO-C
11b	Timeout: start [4-bits]	
11c	Timeout: end-wait [4-bits]	
11d	Timeout: end-active [highest 4-bits]	
12	Data Xmit Errors [15-bits]	
13	Check KILL_Register [20 bits]	
14	Load KILL_Register [20 bits]	
15	DMB Errors [15-bits]	
16	TMB Errors [15-bits]	
17	ALCT Errors [15-bits]	
18	Lost In Event [15-bits]	
* 19	InRD Status [16-bits]	
* 20	InRD C-code & MxmitErr History [16-bits]	
* 21	Critical Error Trap Reg. [192 bits]	
22	Error Register A [16-bits]	
23	Error Register B [16-bits]	
24	Error Register C [16-bits]	
25	Read DMB_LIVE [15-bits]	
26	Read P_DMB_LIVE [15-bits]	
27	Read WARN_MON [16-bits]	
* 28	Max Timeout Count [16-bits]	
29	Set BX per Orbit [12-bits]	
30	Read BX per Orbit [12-bits]	
31	Toggle CFEB_Cal Auto_L1 [default enable]	
32	Read DDU Source ID [16-bits]	
33	DDU-only VME_L1A	
* 34	Read CSC Board Occupancy scalers (loops for 60 words, 32-bit)	
35	Sum of Errors for each CSC [15-bits]	



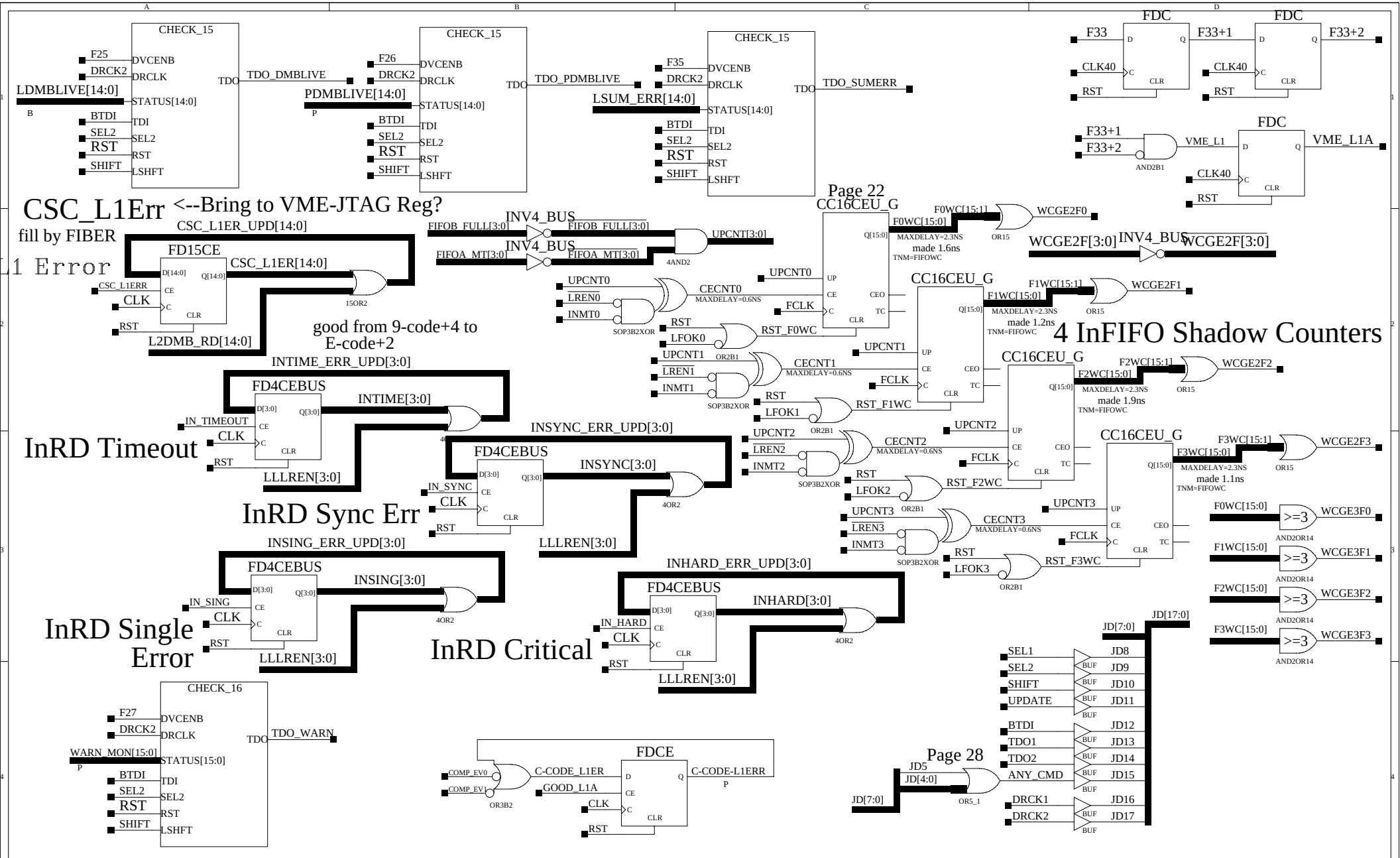
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Signals DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 6-30-2009_13:35	FILE: FIFOCTRL . 5	PAGE: 3D



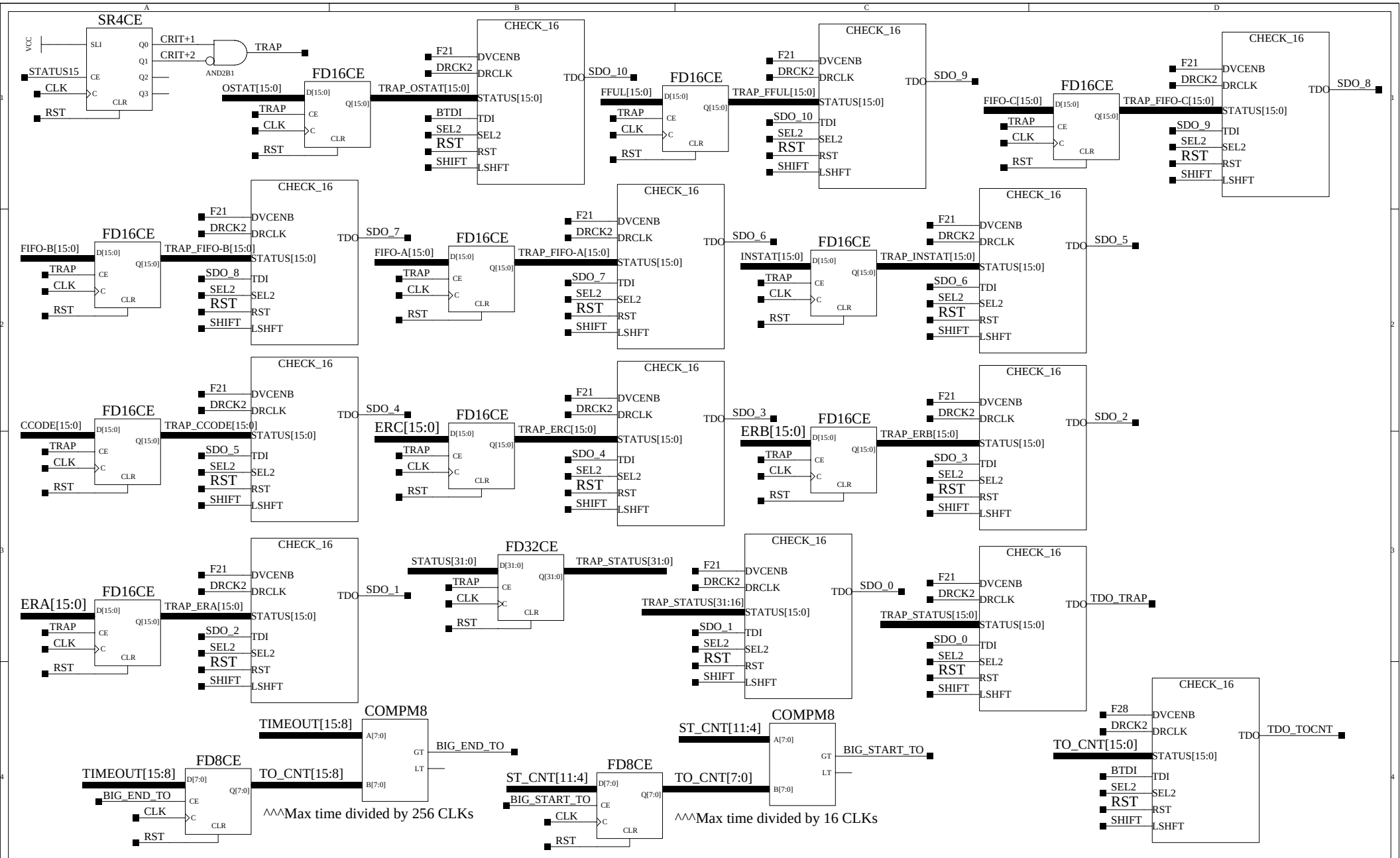
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-9-2006_15:30	FILE: FIFOCTRL . 6	PAGE: 3E



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG DATE: 8-14-2008_16:21	PARENT PAGE: 2 FILE: FIFOCTRL . 7
		PROJECT: D785C	PAGE: 3F

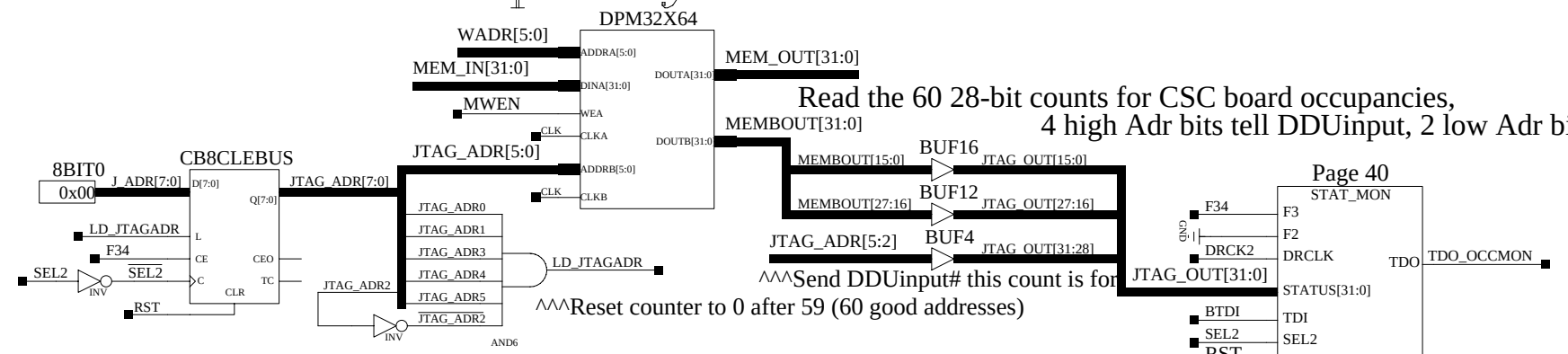


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 8-14-2008_16:14	FILE: FIFOCTRL . 8	PAGE: 3G



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Critical Error Trap DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 5-23-2006_14:23	FILE: FIFOCTRL . 9	PAGE: 3H

CSC Board Occupancy Tracker: 15 fibers x 4—boards each

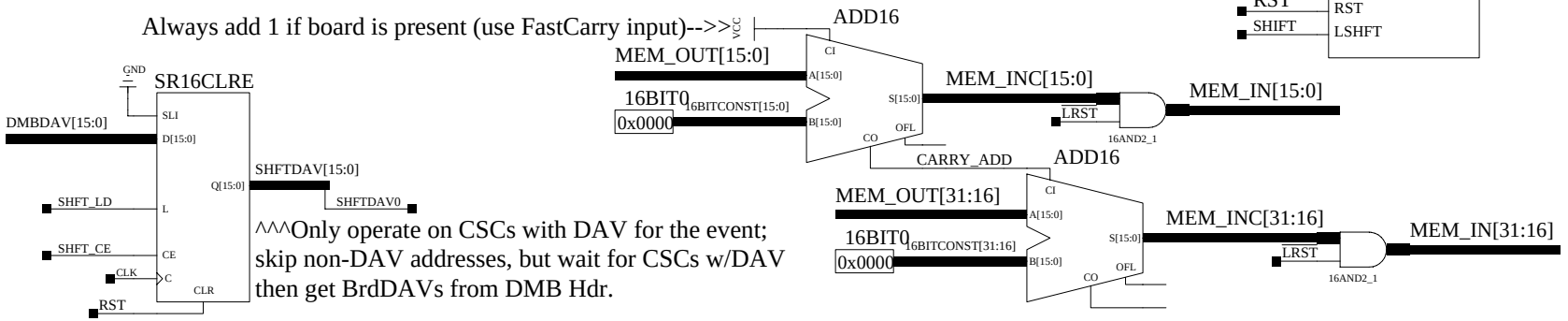


Read the 60 28-bit counts for CSC board occupancies,
4 high Adr bits tell DDUinput, 2 low Adr bits specifiy Board Type:
0 = DMB
1 = ALCT
2 = TMB
3 = CFEB

^^^Send DDUinput# this count is for

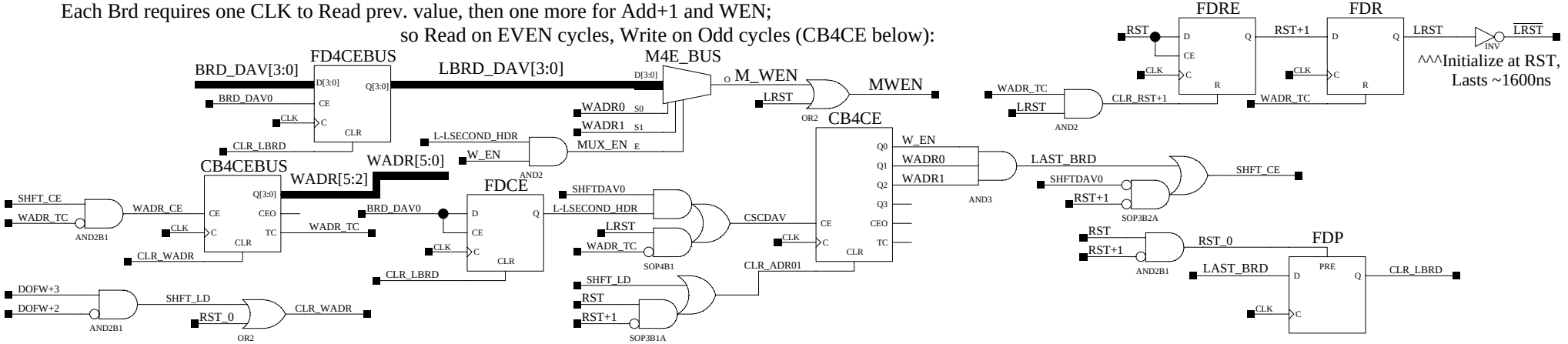
^^^Reset counter to 0 after 59 (60 good addresses)

Always add 1 if board is present (use FastCarry input)-->>>



^^^Only operate on CSCs with DAV for the event; skip non-DAV addresses, but wait for CSCs w/DAV then get BrdDAVs from DMB Hdr.

Each Brd requires one CLK to Read prev. value, then one more for Add+1 and WEN;
so Read on EVEN cycles, Write on Odd cycles (CB4CE below):



^^^Initialize at RST, Lasts ~1600ns

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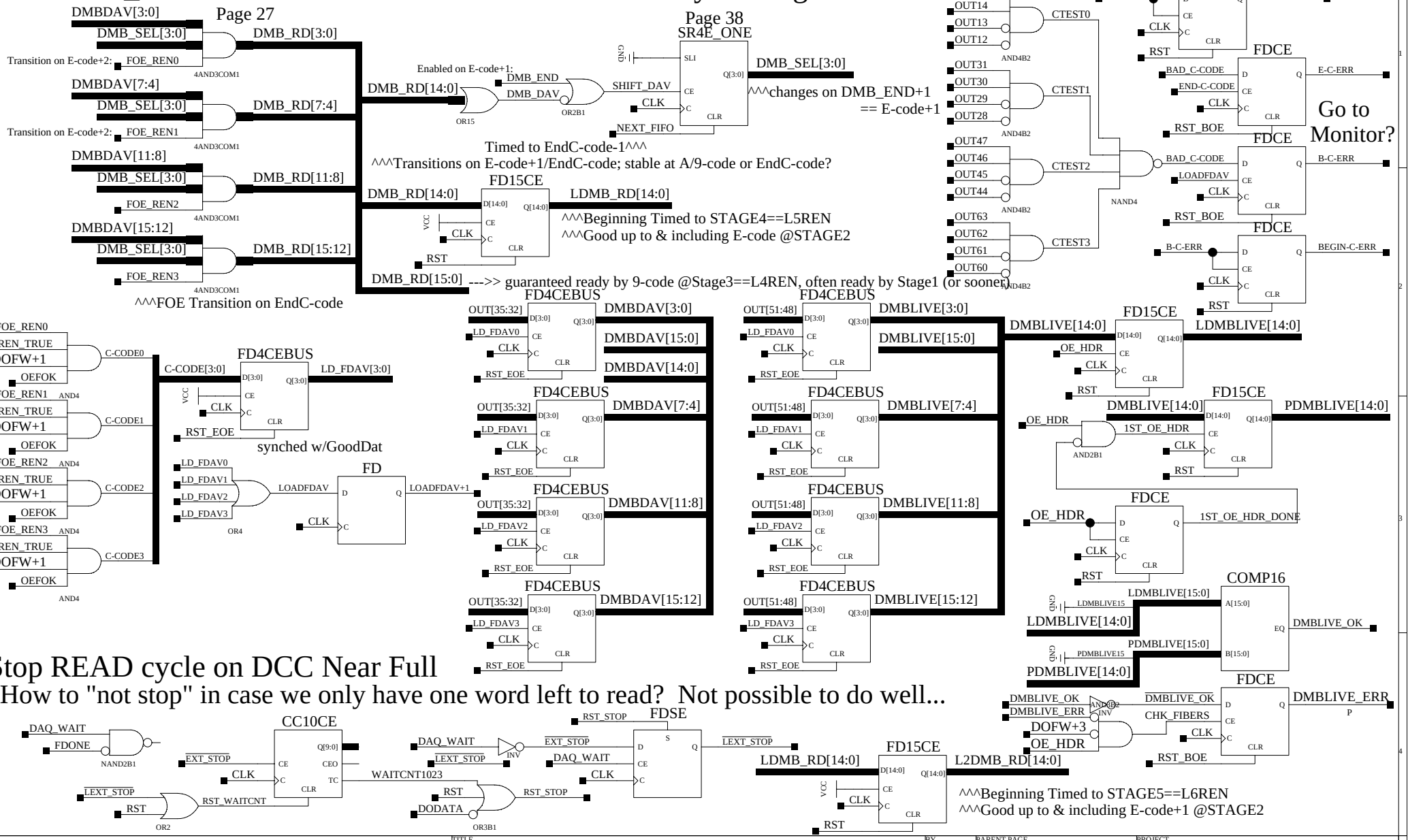
TITLE: DDU Occupancy Monitor
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
5-23-2006_14:23	FIFOCTRL . 10	3I

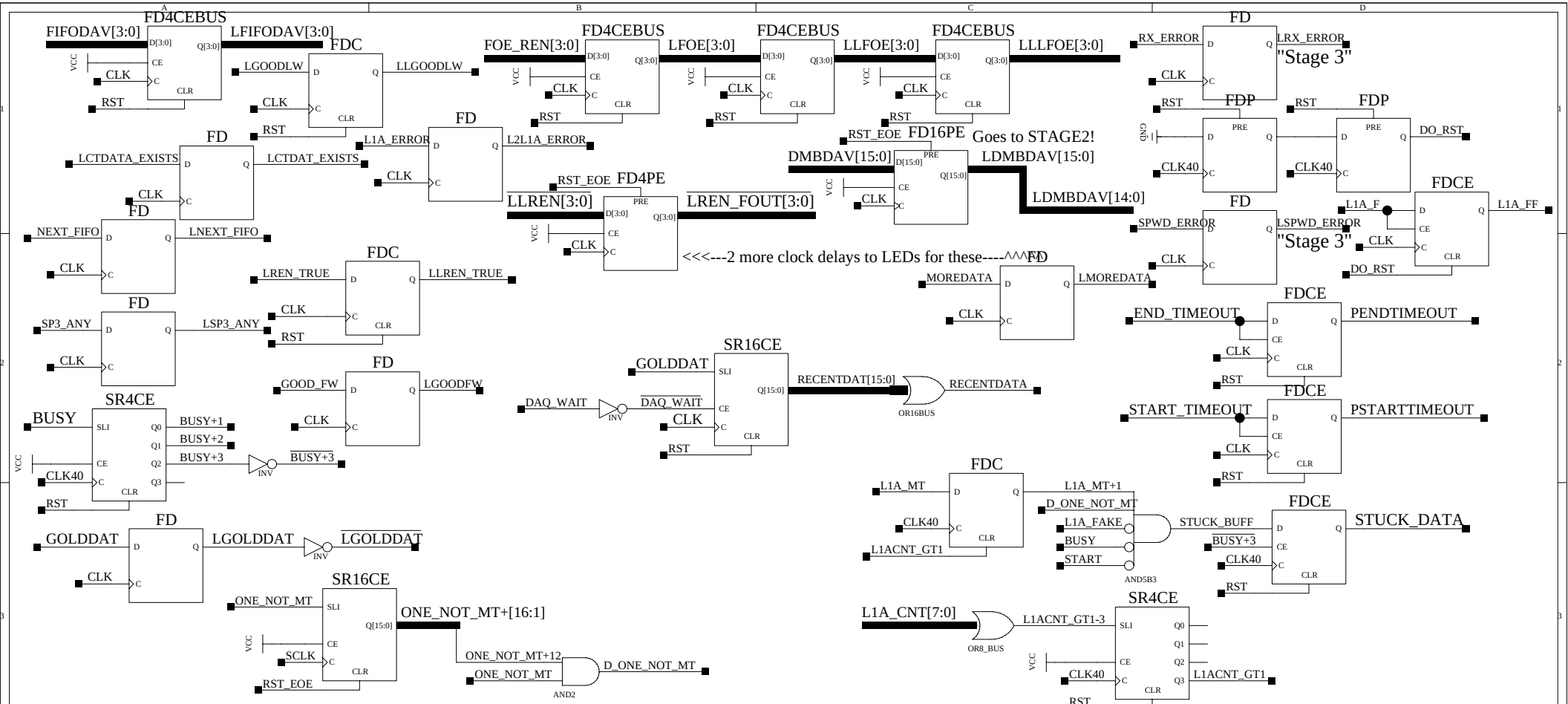
Use DMB_RD to determine which FIBER we're currently reading



Stop READ cycle on DCC Near Full

How to "not stop" in case we only have one word left to read? Not possible to do well...

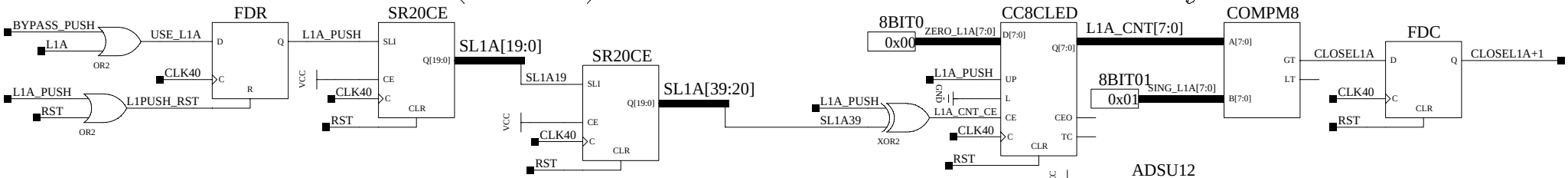
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG DATE: 5-23-2006_14:23	PARENT PAGE: 2 FILE: FIFOCTRL . 11
		PROJECT: D785C	PAGE: 3J



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 11-8-2006_11:11	FILE: FIFOCTRL . 12	PAGE: 3K

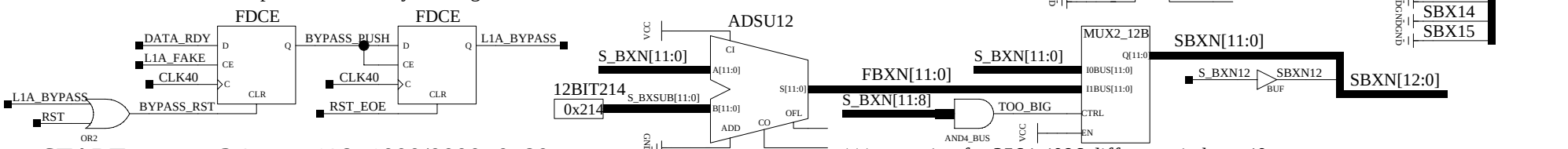
L1A Proximity Tracker: 1000ns Close L1A Monitor (40 BX) closer than 950ns is Tricky for DMBs

END



Pipe all L1As for 1000ns, if more than 1 then set CloseL1A bit^^^

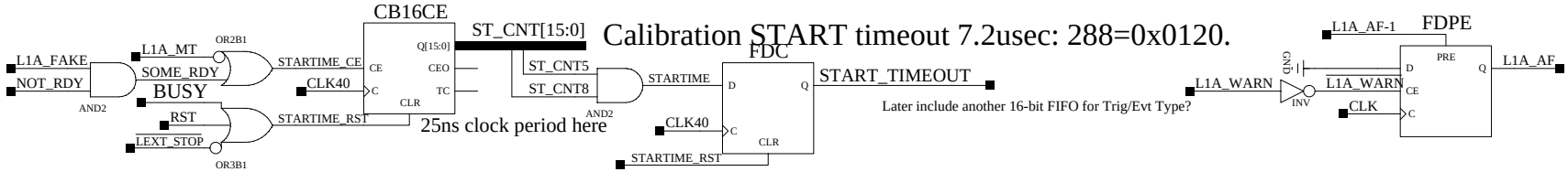
Finally, perform BX-40 to correct BXN and store CloseL1A as BXN bit-12 (& correct for BX<40 case).
Then use SBXN12 output (Close_L1A) for Stage2 DMB checks: 1000+ ns L1As means
that first 2 CFEB samples should always have good L1A#



Event START timeout 3.2usec: 128=1000/0000=0x80....

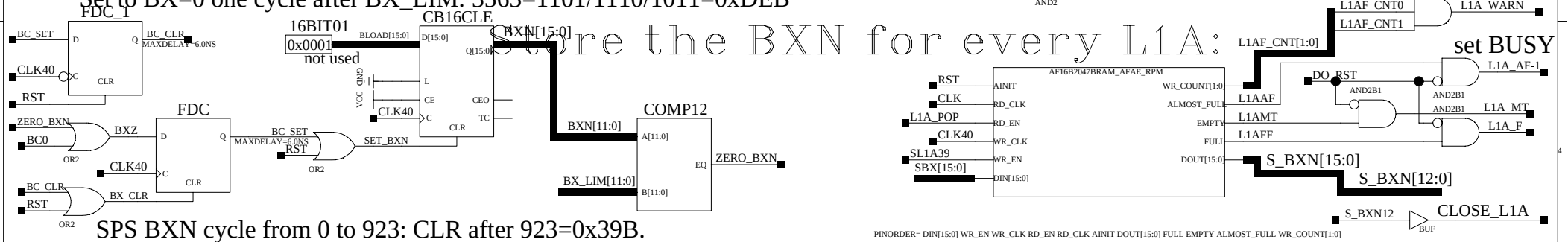
^^^correction for 3564-4096 difference in bxn<40 case

Calibration START timeout 7.2usec: 288=0x0120.



LHC BXN cycles from 0 to 3563

Set to BX=0 one cycle after BX_LIM: 3563=1101/1110/1011=0xDEB



SPS BXN cycle from 0 to 923: CLR after 923=0x39B.

PINORDER= DIN[15:0] WR_EN WR_CLK RD_EN RD_CLK AINIT DOUT[15:0] FULL EMPTY ALMOST_FULL WR_COUNT[1:0]

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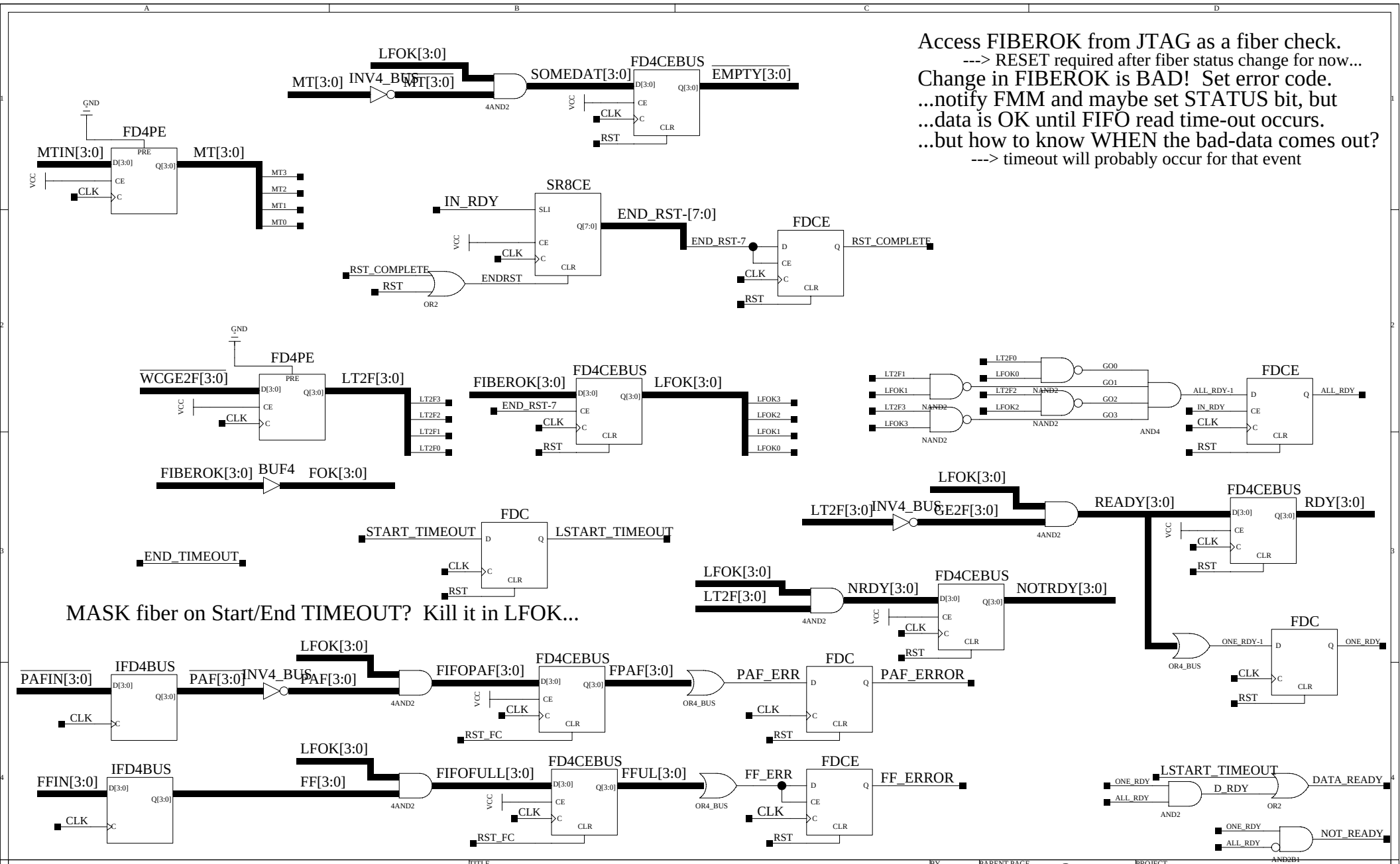
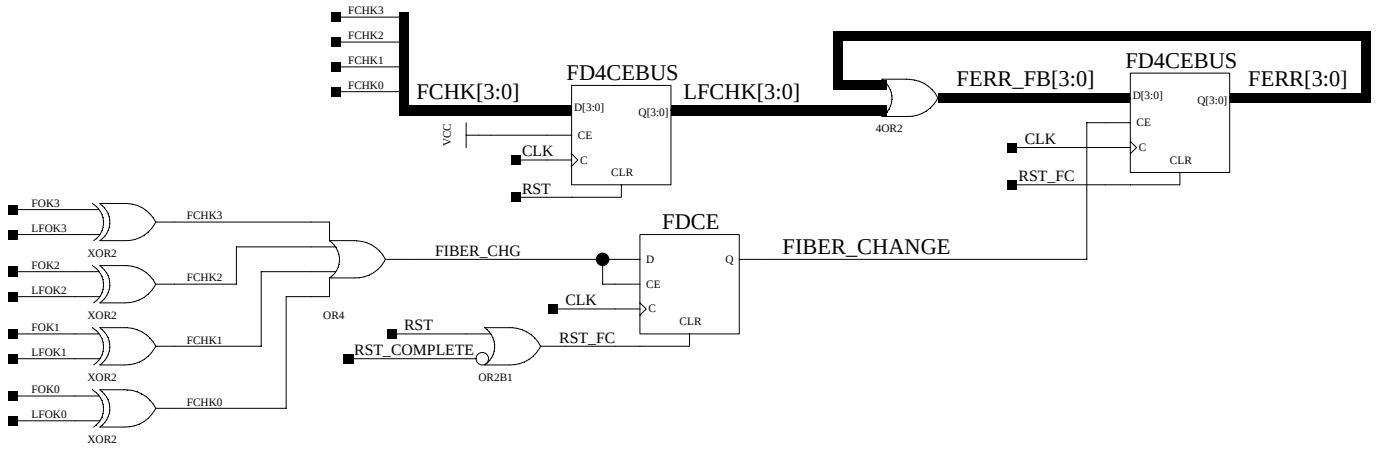
TITLE	DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785C
		DATE 7-31-2007_13:43	FILE FIFOCTRL . 13	PAGE 3L

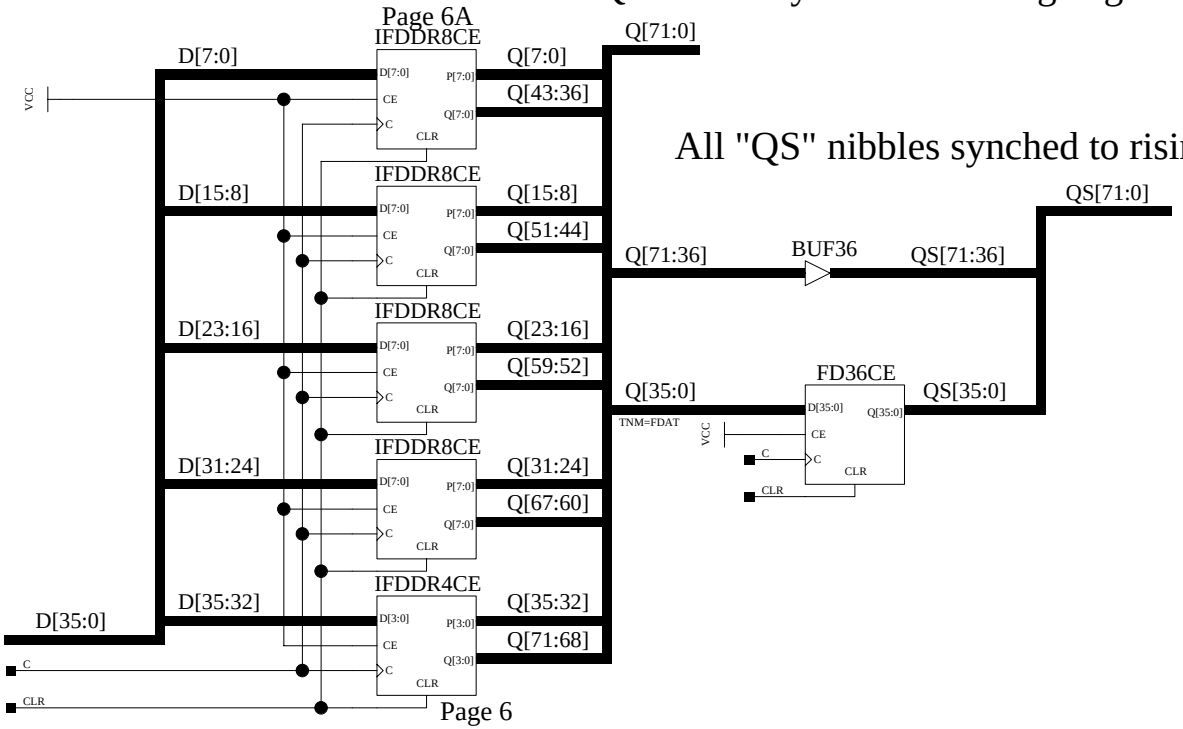


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Input FPGAs Available for DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 9-12-2006_10:43	FILE: FIFO_RDY . 1	PAGE: 4



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Inputs from DMB FIFOs to DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 9-12-2006_10:43	FILE: FIFO_RDY . 2	PAGE: 4A

Lowest 9 "Q" nibbles synched to falling edge of CLK



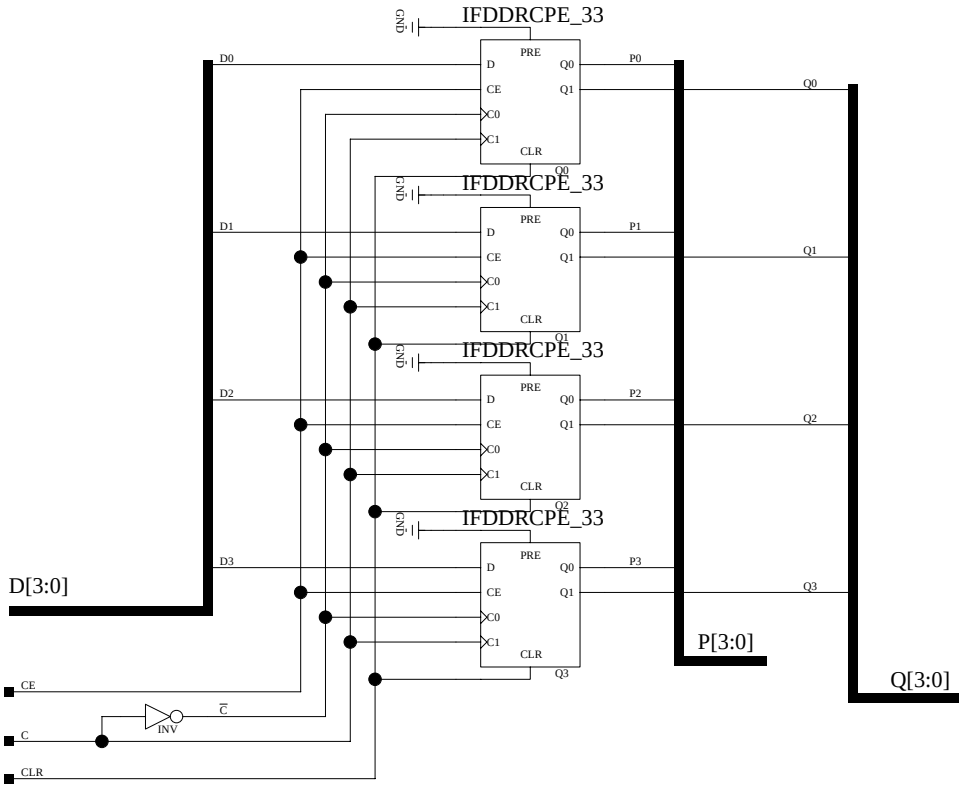
All "QS" nibbles synched to rising edge of CLK

CLK/\ -- DIN[35:0] -- CLK\/ -- Q[35:0] DIN[71:36] -- CLK/\ -- Q[71:36] QS[35:0]

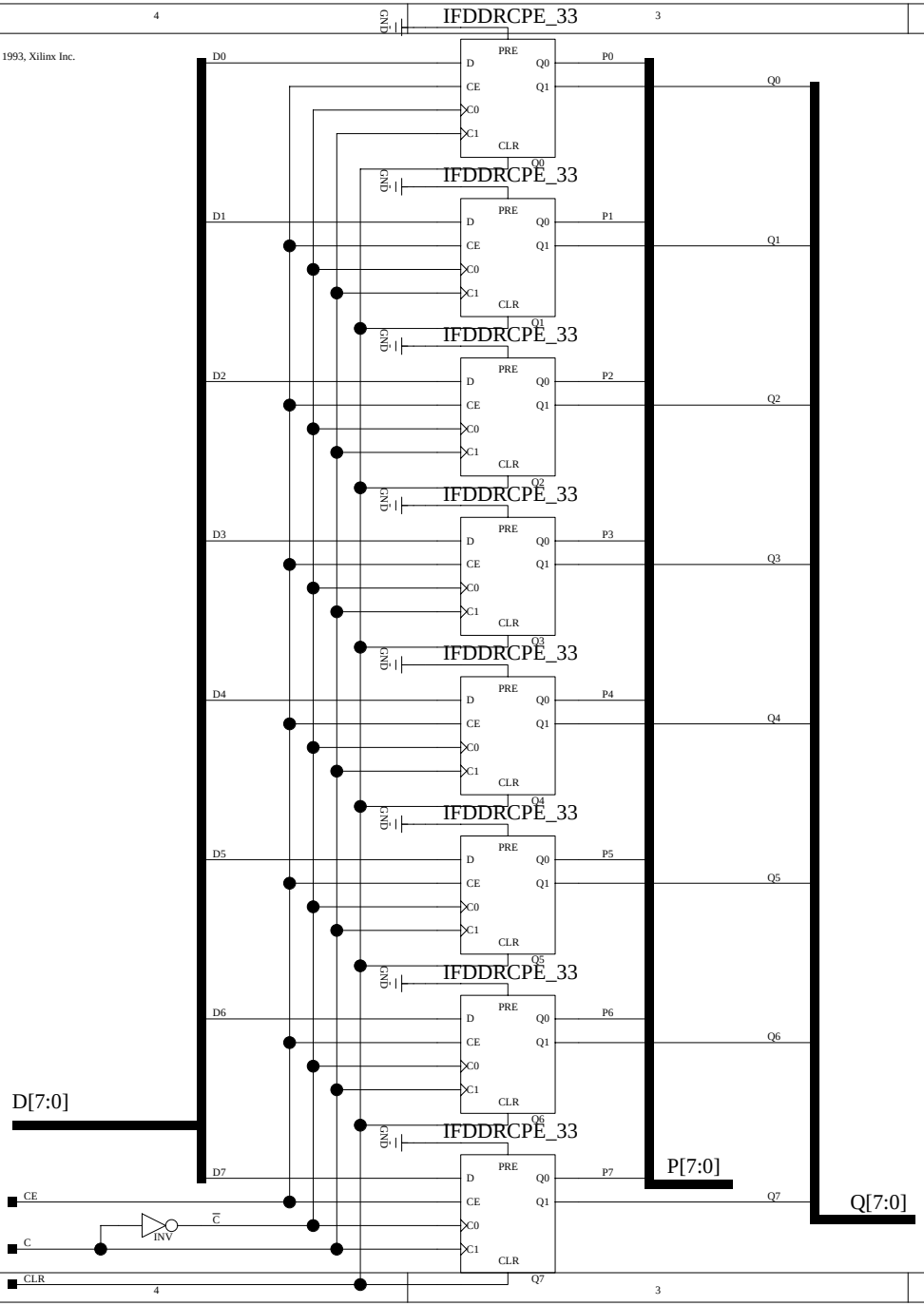
XILINX

Title:	VIRTEX Family IFDDR36C Macro, LVCMOS33		
Comments:	36-Bit DDR Input Flip-Flop with asynchronus clear	JRG	
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A

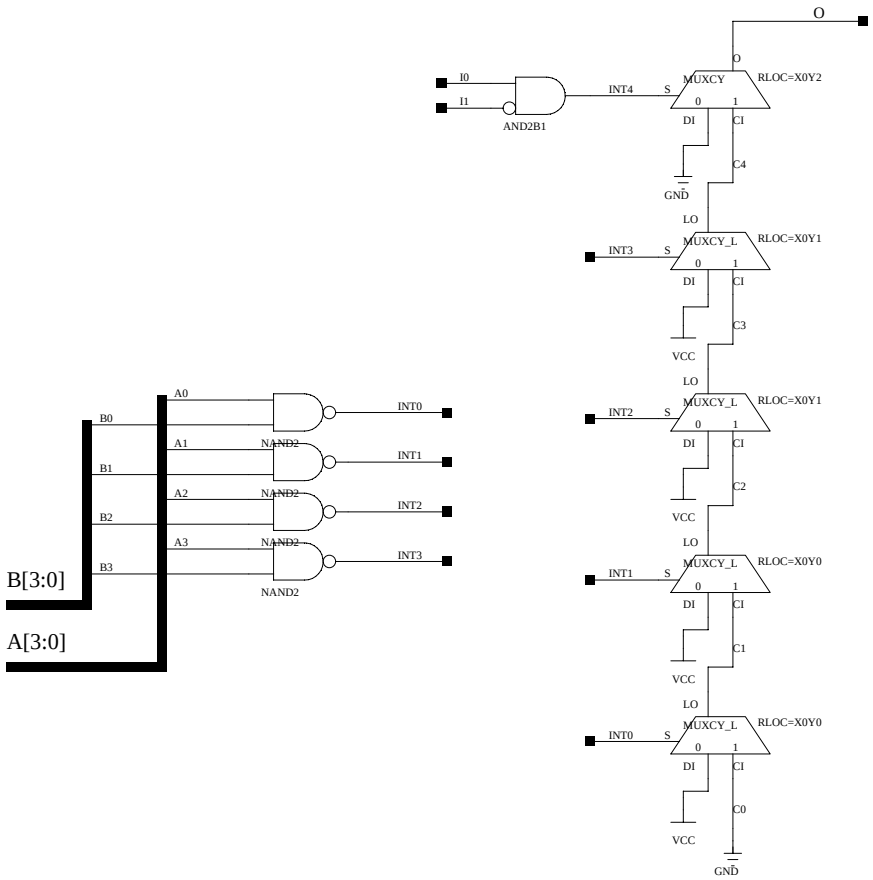
drawn by KS



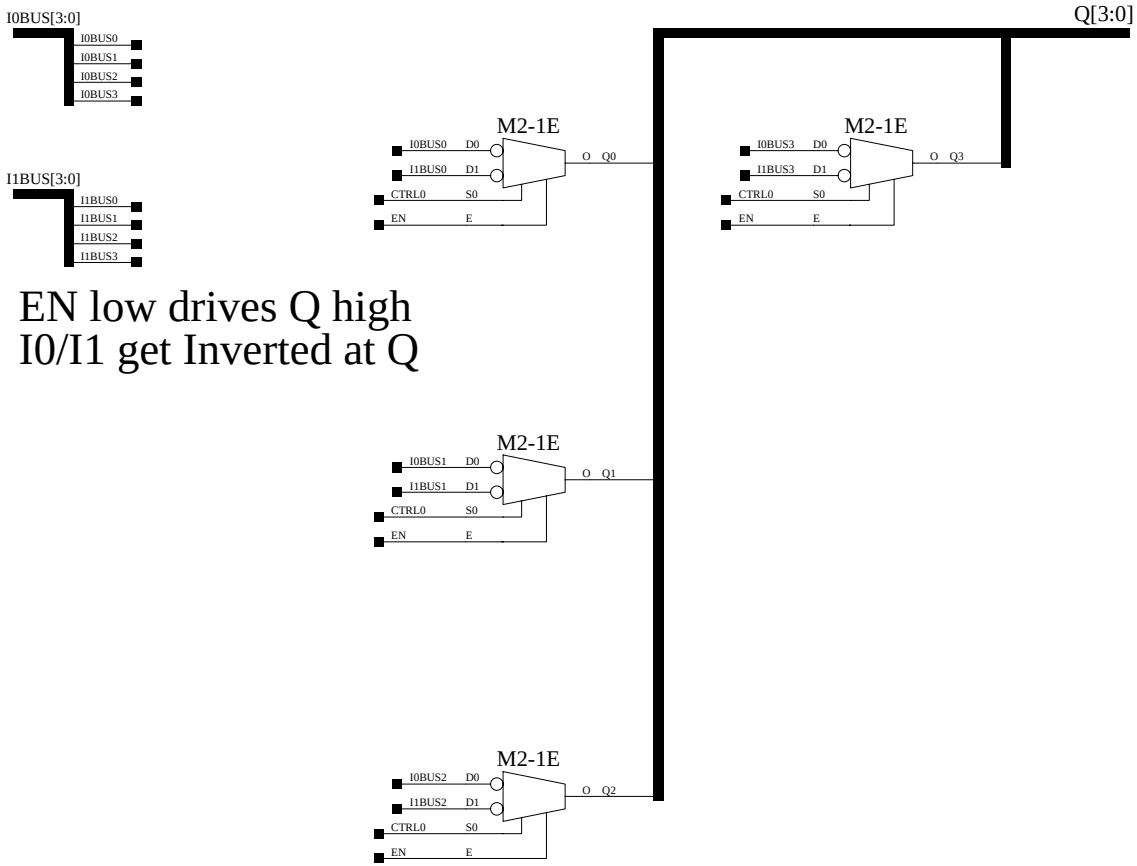
Title:	VIRTEX Family IFDDR4CE Macro, LVCMOS33		JRG
Comments:	4-Bit Double-Data-Rate Input Register w/ Clock Enable & Asynchronous Clr		
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A



Title:	VIRTEX Family IFDDR8CE Macro, LVCMOS33		
Comments:	8-Bit Double-Data-Rate Input Register w/ Clock Enable & Asynchronous Clr	JRG	
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A



XILINX			JRG
Title:	FAST10B1		
Comments:	Custom Fast, Complex Logic for DDU, use 4 MUXCY as OR, 1 as AND similar to: OR of 4 AND2 .AND. AND2B1		
Date:	15th October 2003	Ver:	1
Sheet Size: B		Rev:	A

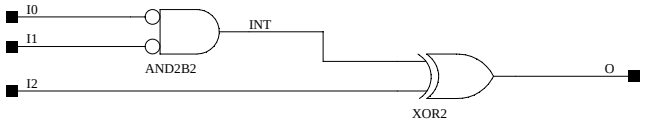


EN low drives Q high
I0/I1 get Inverted at Q

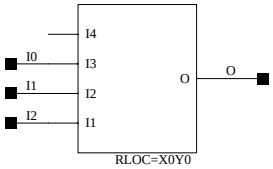
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: 4-bit MUX for 2 4-bit Inputs, w/Enable, invert selected DIN
DDU Input Controller Logic
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	3	D785C
DATE	FILE	PAGE
5-24-2005_14:02	MUX2_4B_INV . 1	8

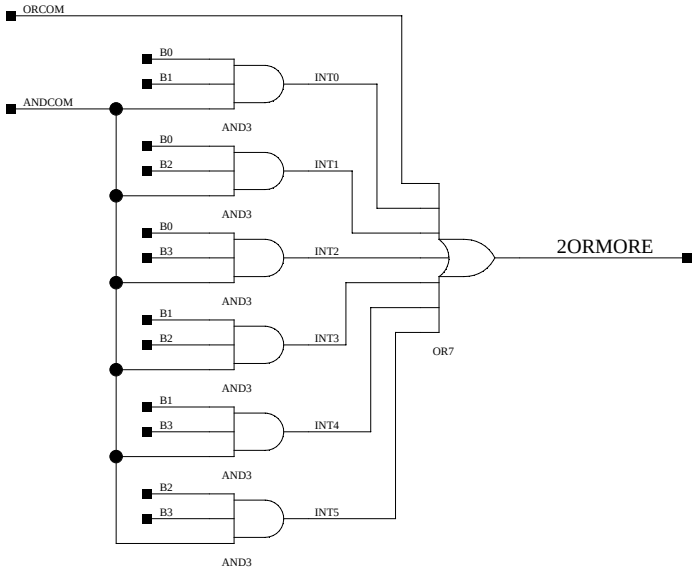


FMAP

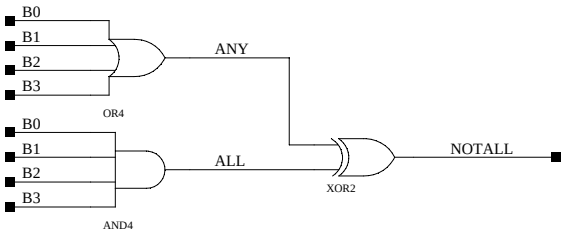


Title:	VIRTEX Family SOP3B2XOR Macro	
Comments:	SOP3B2XOR Gate	JRG
Date:	11th December 2003	Ver: 1
Sheet Size: A		Rev: A

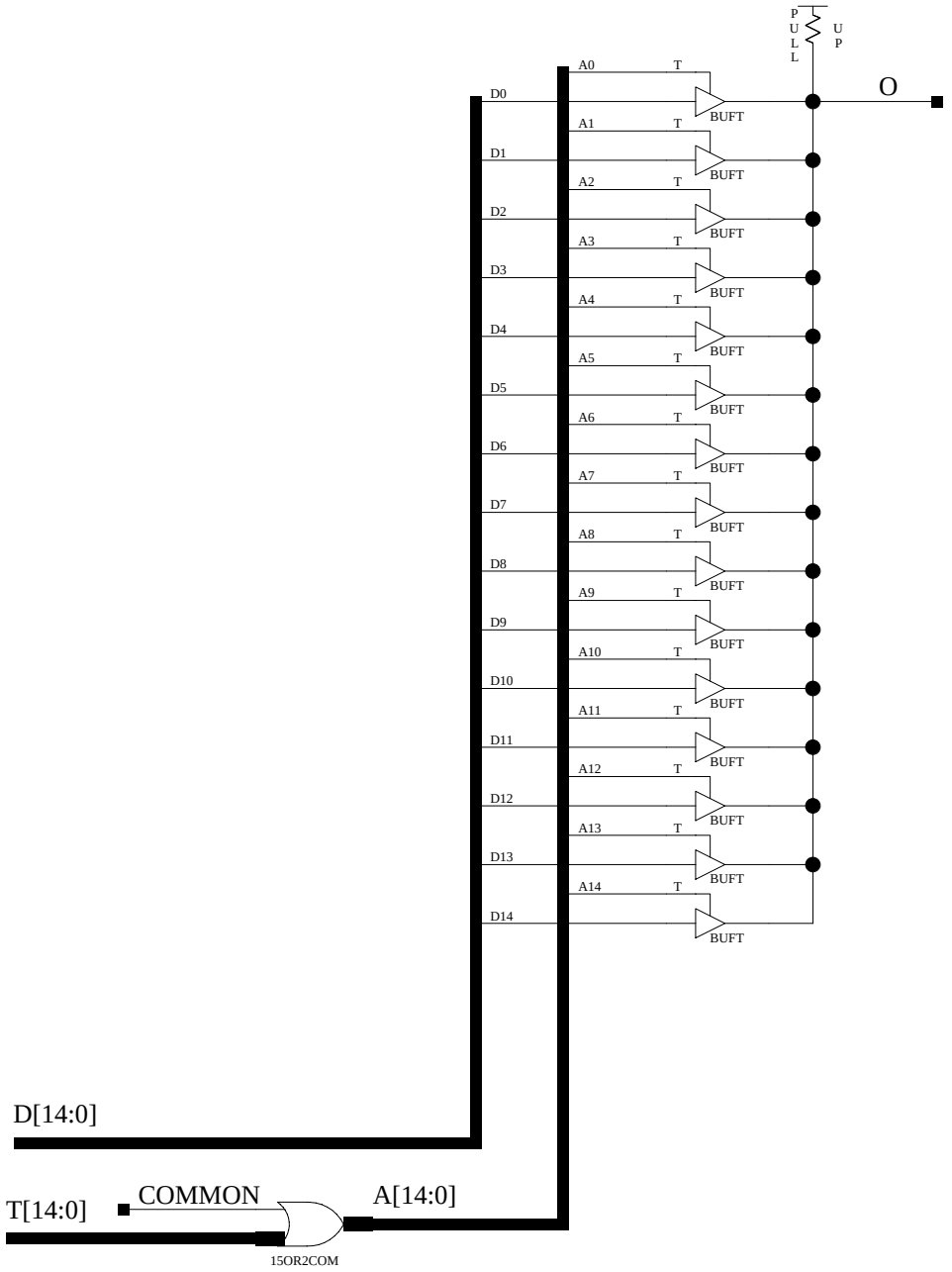
drawn by KS



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Check for 2 Or More Bits Set Out of 4, PLUS common AND and OR bits DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 3	PROJECT D785C
			DATE 7-18-2005_17:01	FILE 2ORMOREP . 1	PAGE 10



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Check for ALL bits set, ANY bits set and NOTALL bits set DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 7-18-2005_17:01	FILE: ANYORALL . 1	PAGE: 10A



XILINX

Title: VIRTEX Family 15-BufTOR Macro

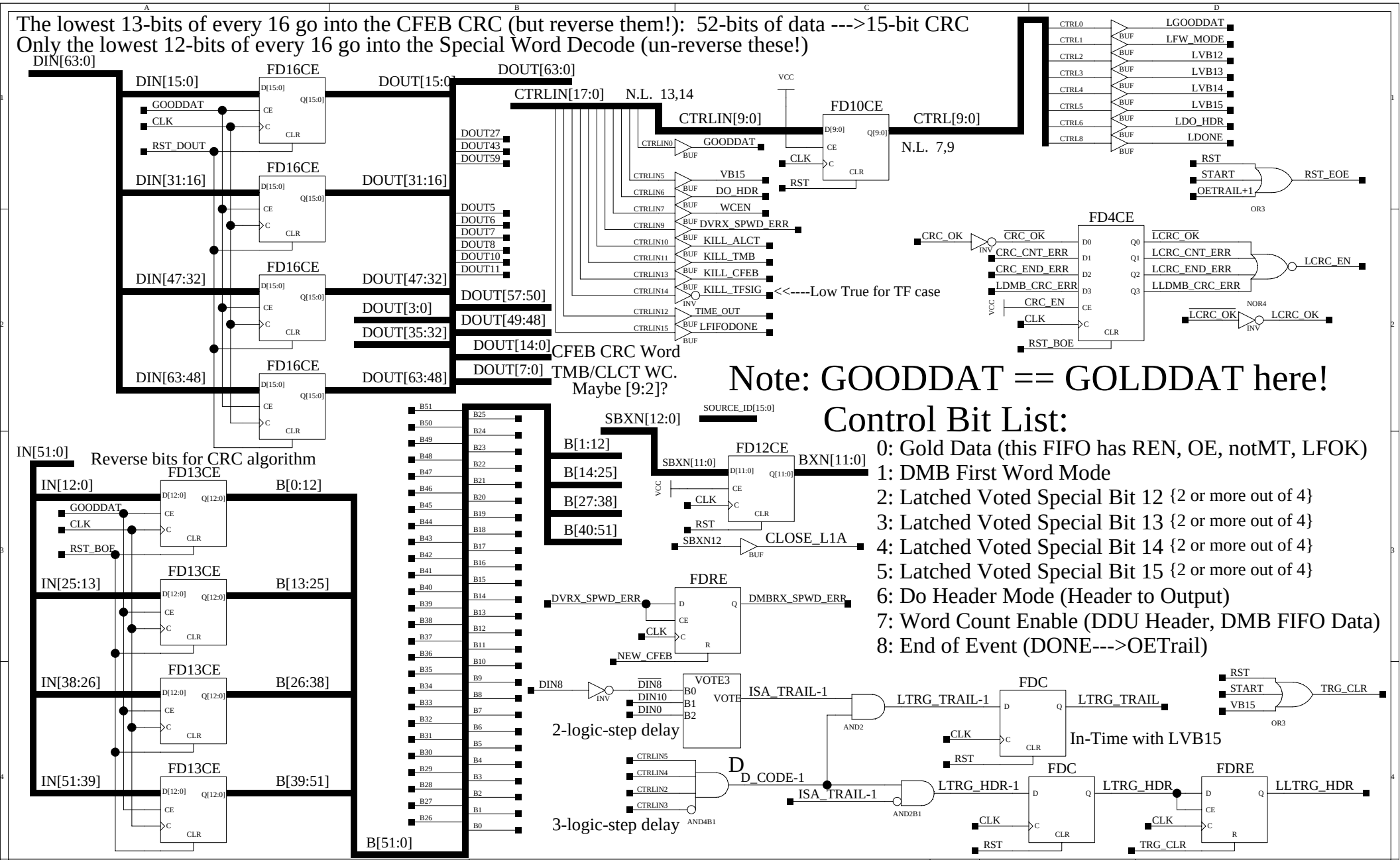
Comments: 15-BufT Bus Gate with Bus-OR-Common control

JRG

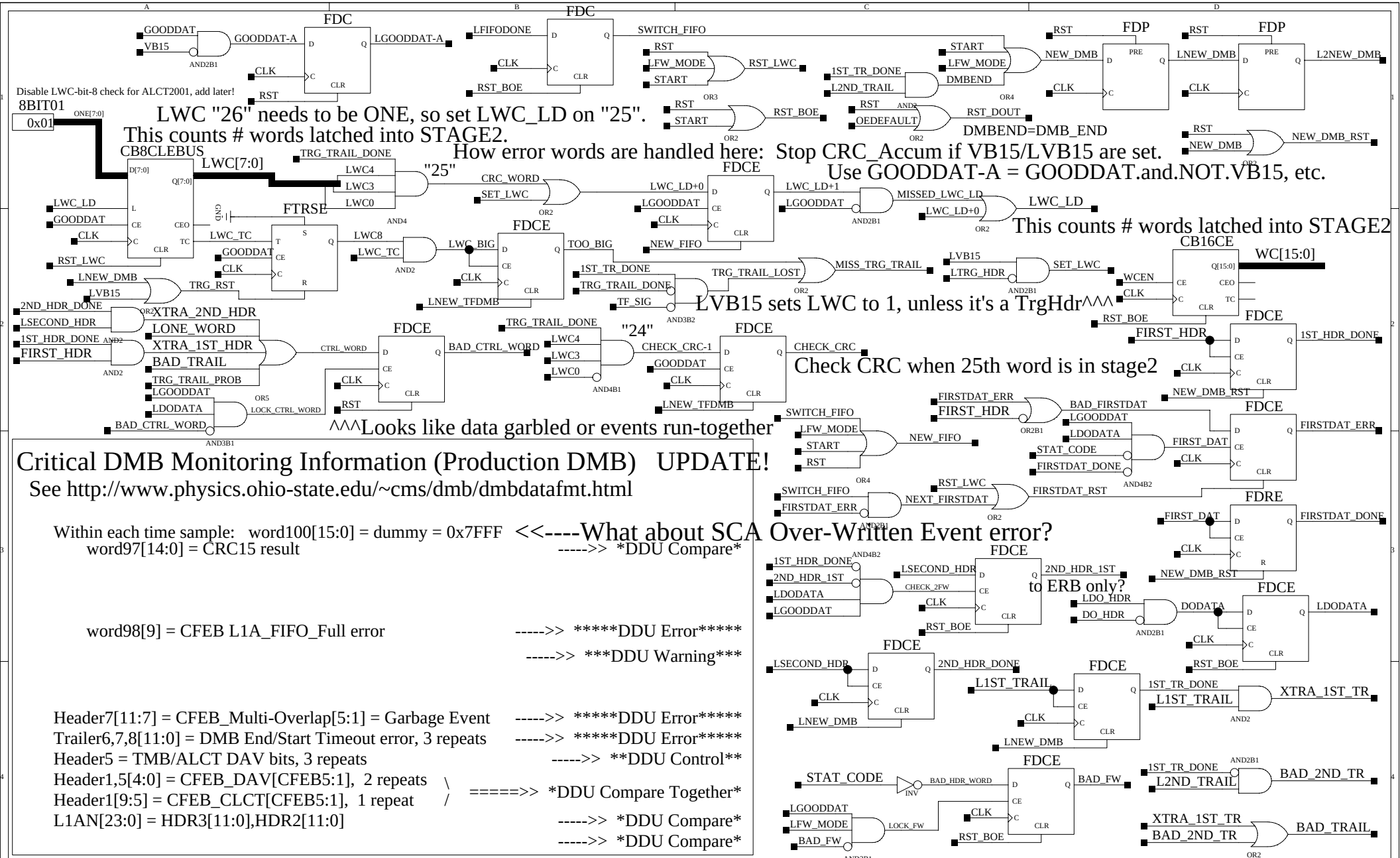
Date: 27th December 2001 Ver: 1

Sheet Size: A Rev: A

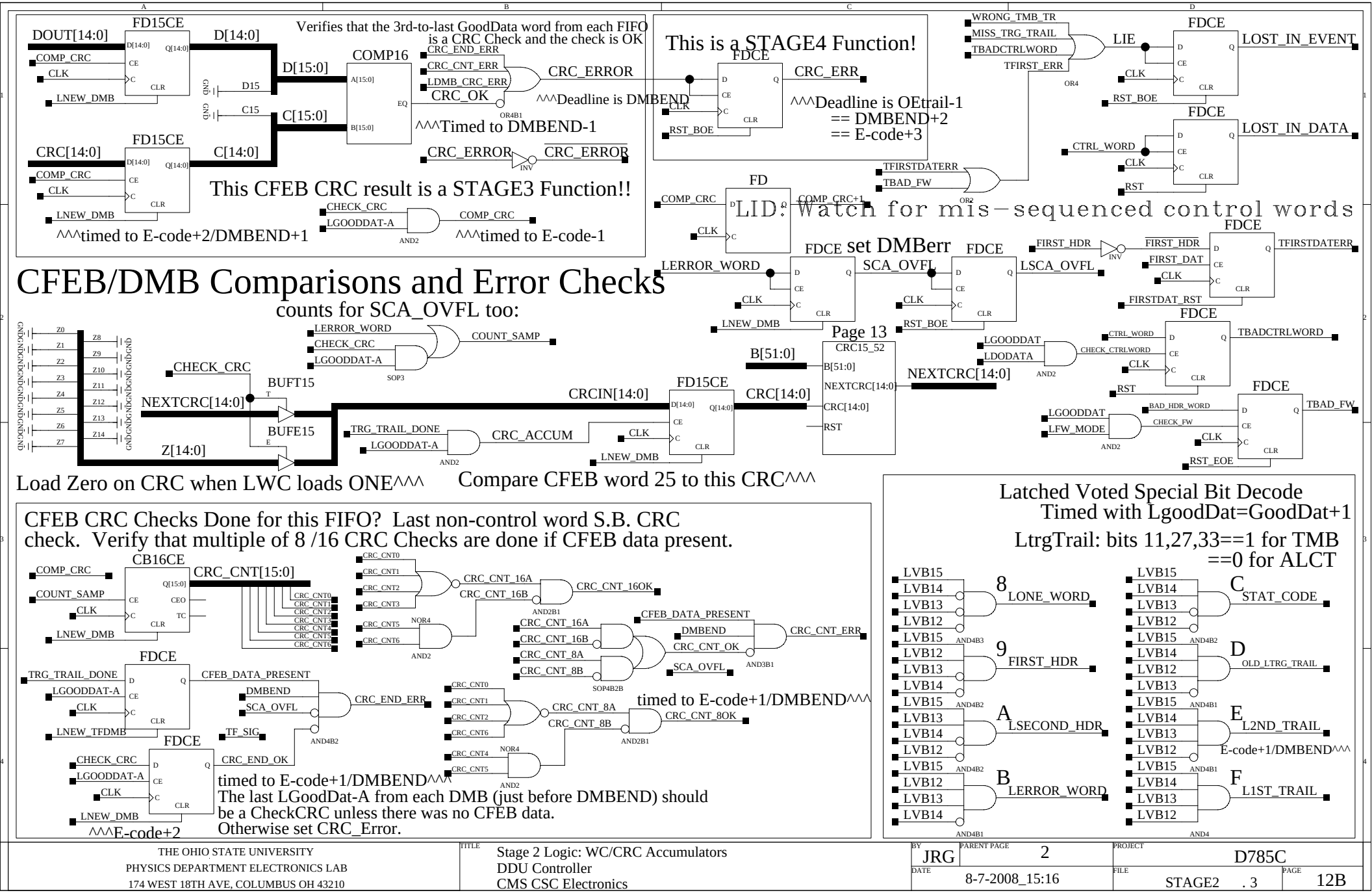
drawn by KS



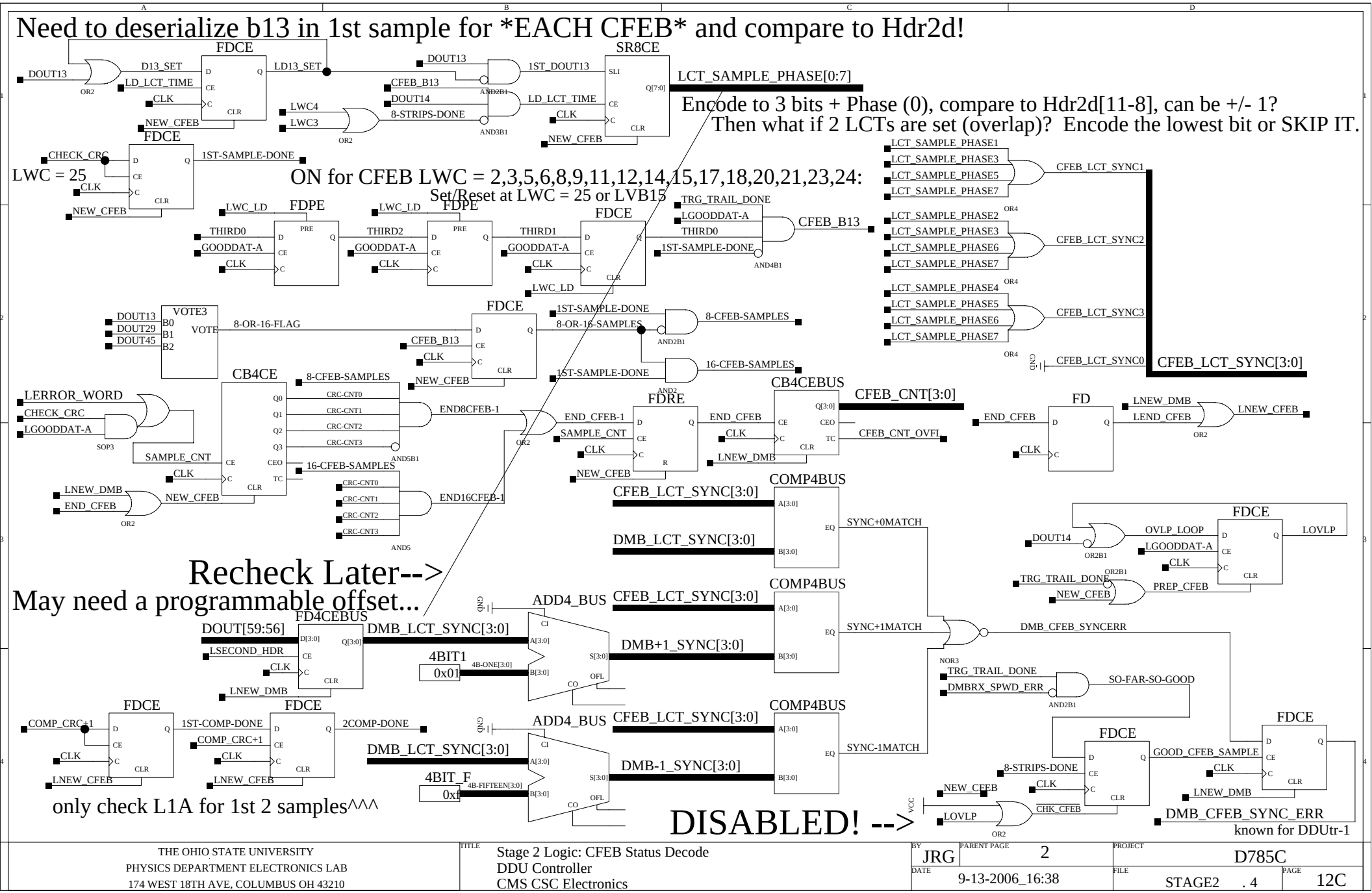
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG PARENT PAGE: 2 DATE: 6-19-2009_13:23	PROJECT: D785C FILE: STAGE2 . 1 PAGE: 12



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-17-2007_16:35	FILE: STAGE2 . 2	PAGE: 12A

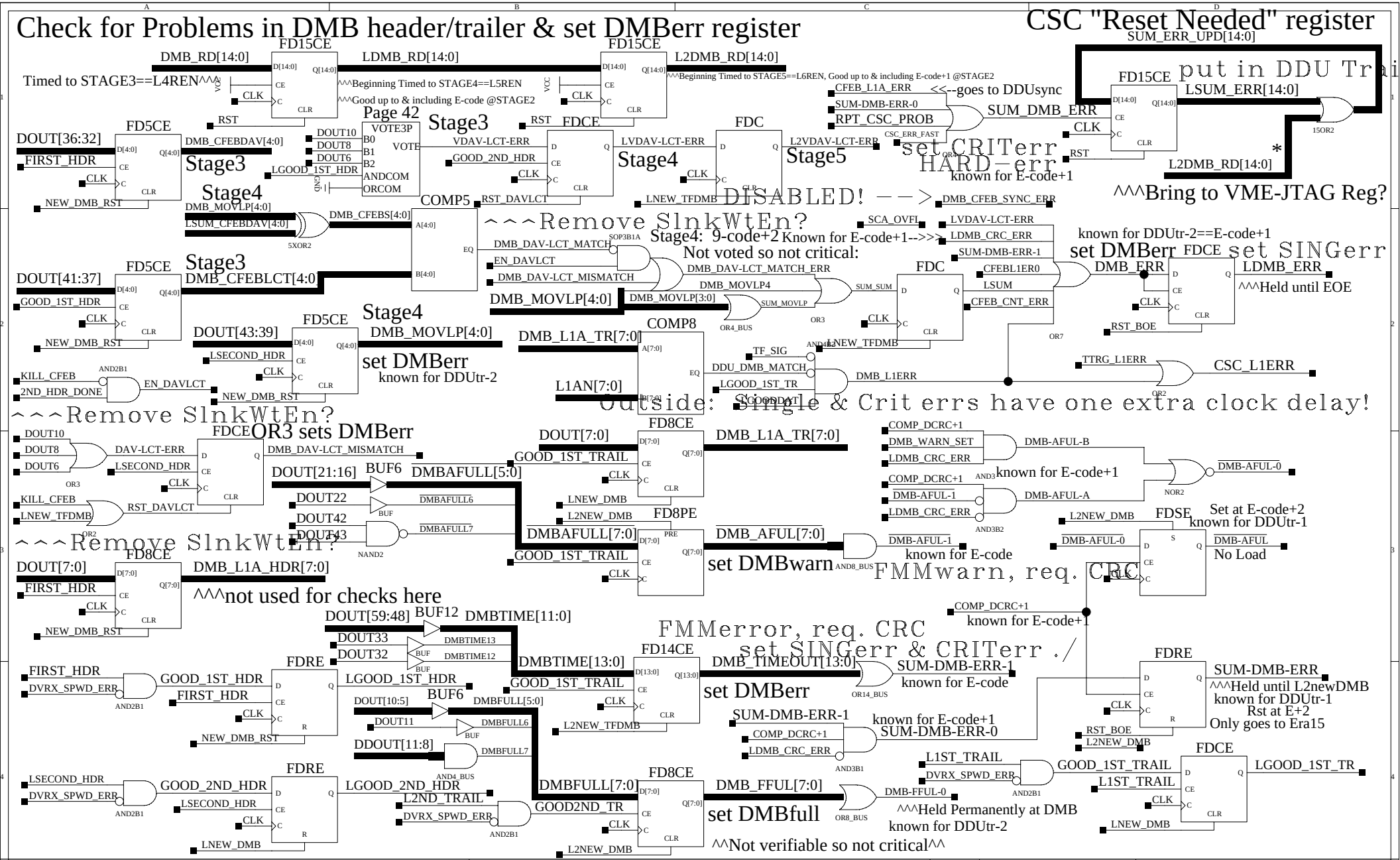


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 8-7-2008_15:16	FILE: STAGE2 . 3	PAGE: 12B



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: CFEB Status Decode DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 9-13-2006_16:38	FILE: STAGE2 . 4	PAGE: 12C

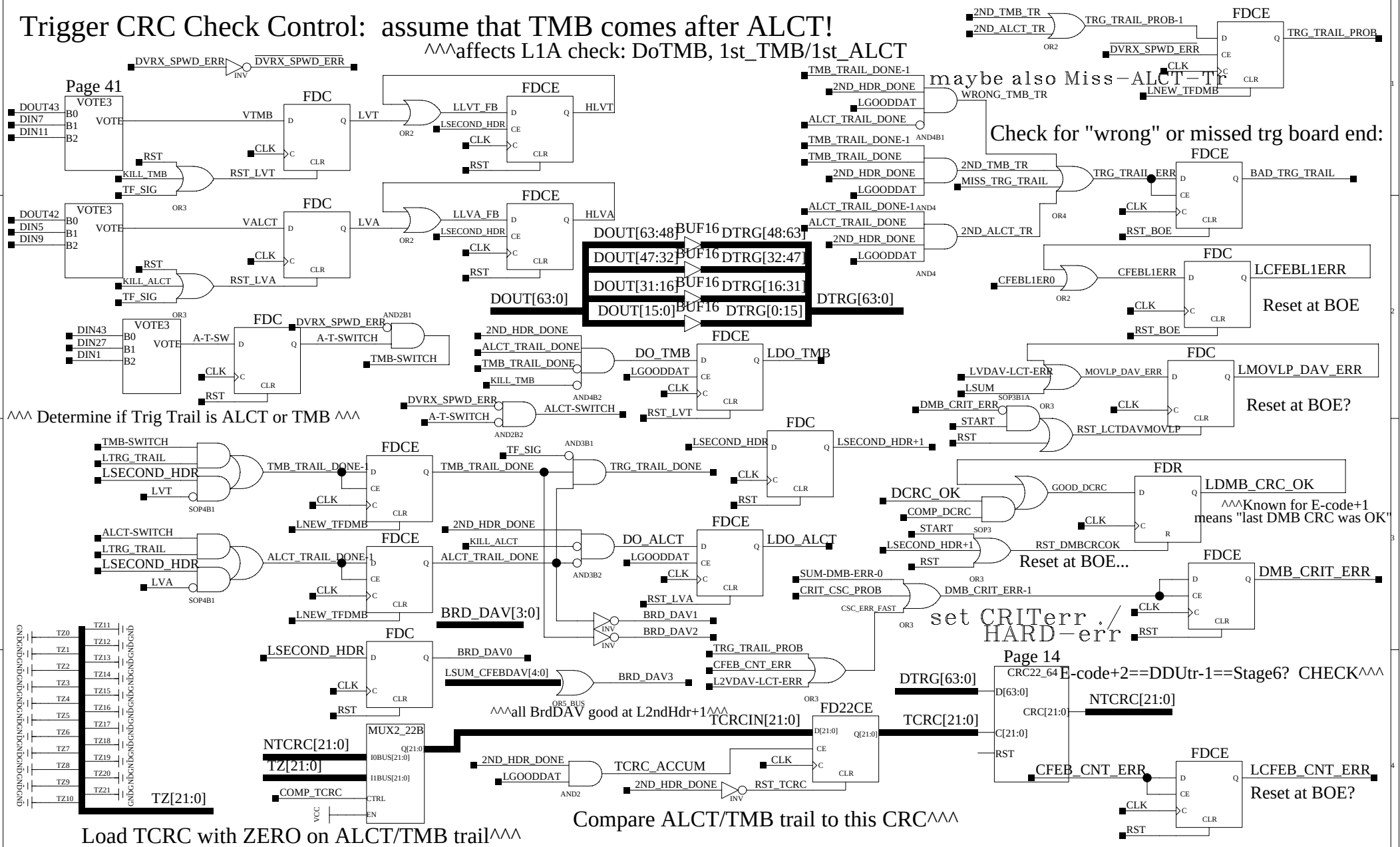
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: CFEB Count & DMB CRC Check DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C	
		DATE: 8-7-2008_15:16		FILE: STAGE2 . 5	PAGE: 12D



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: DMB Status Checks DDU Controller CMS CSC Electronics	BY: JRG DATE: 8-12-2008_17:20	PARENT PAGE: 2 FILE: STAGE2 . 6
		PROJECT: D785C	PAGE: 12E

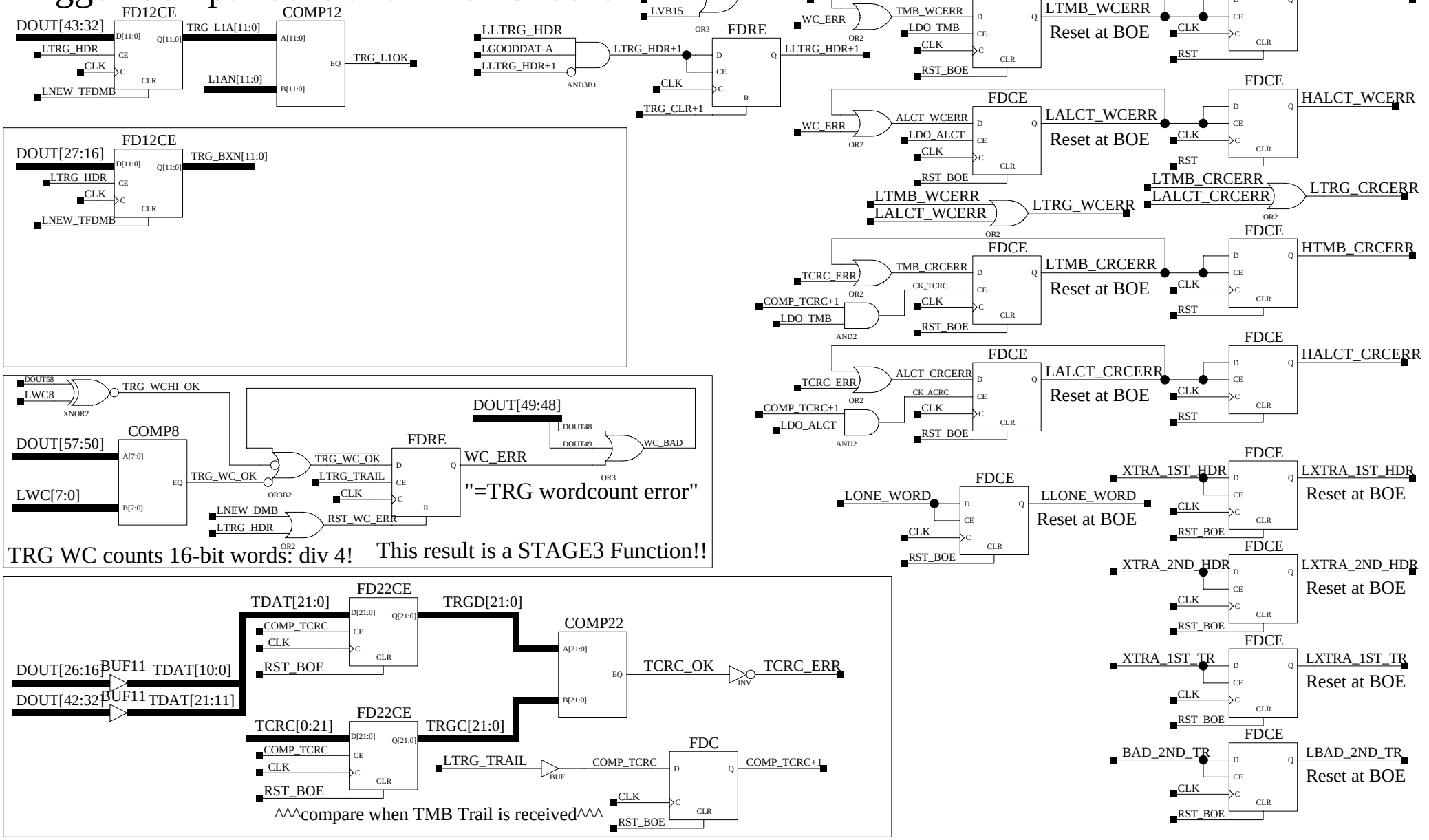
Trigger CRC Check Control: assume that TMB comes after ALCT!

^^^affects L1A check: DoTMB, 1st_TMB/1st_ALCT



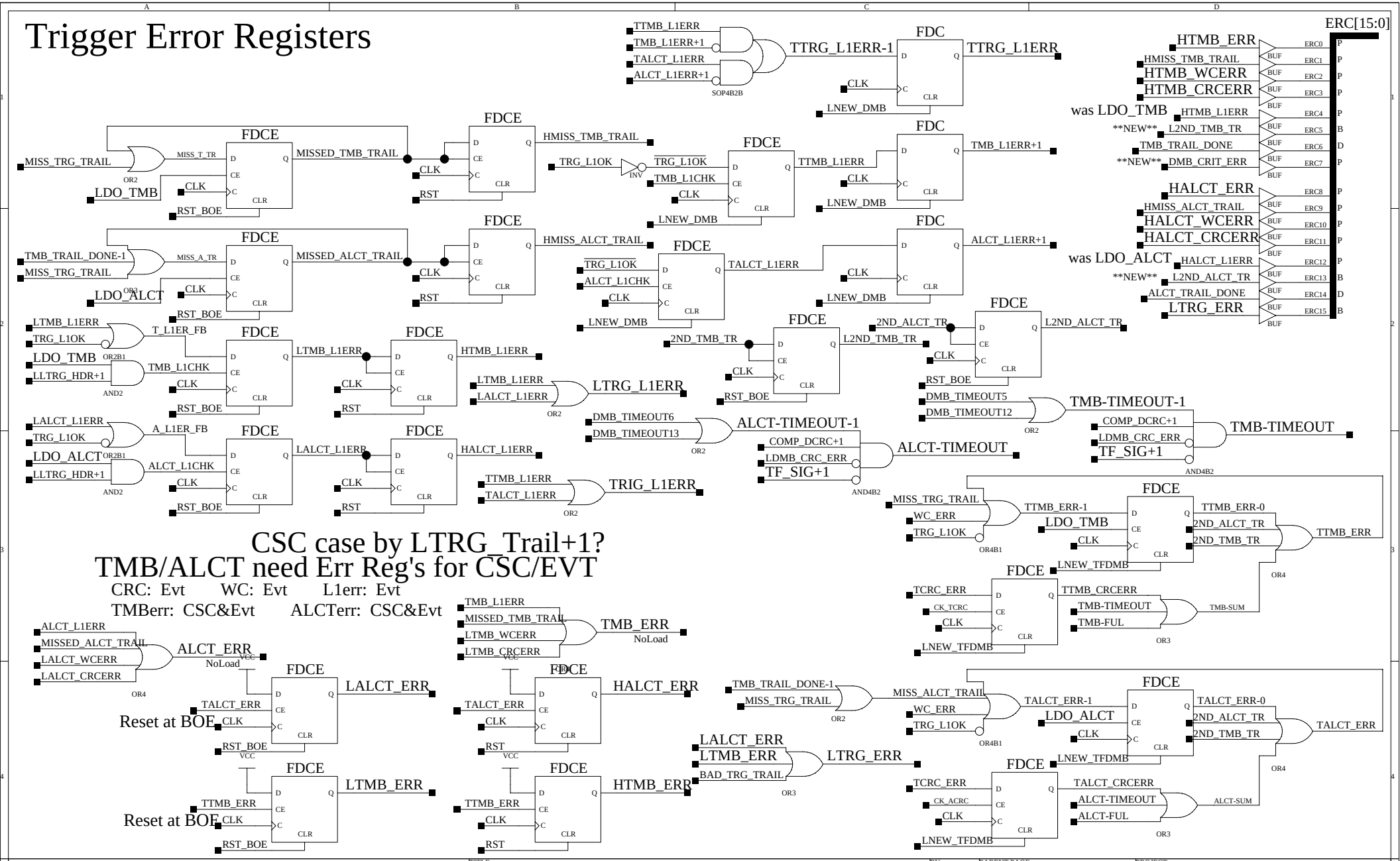
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: Trigger Board Flags DDU Controller CMS CSC Electronics	BY: JRG DATE: 8-12-2008_17:18	PARENT PAGE: 2 FILE: STAGE2 . 7
		PROJECT: D785C	PAGE: 12F

Trigger Comparisons and Error Checks



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: Trigger Error Checks DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-3-2007_15:07	FILE: STAGE2 . 8	PAGE: 12G

Trigger Error Registers



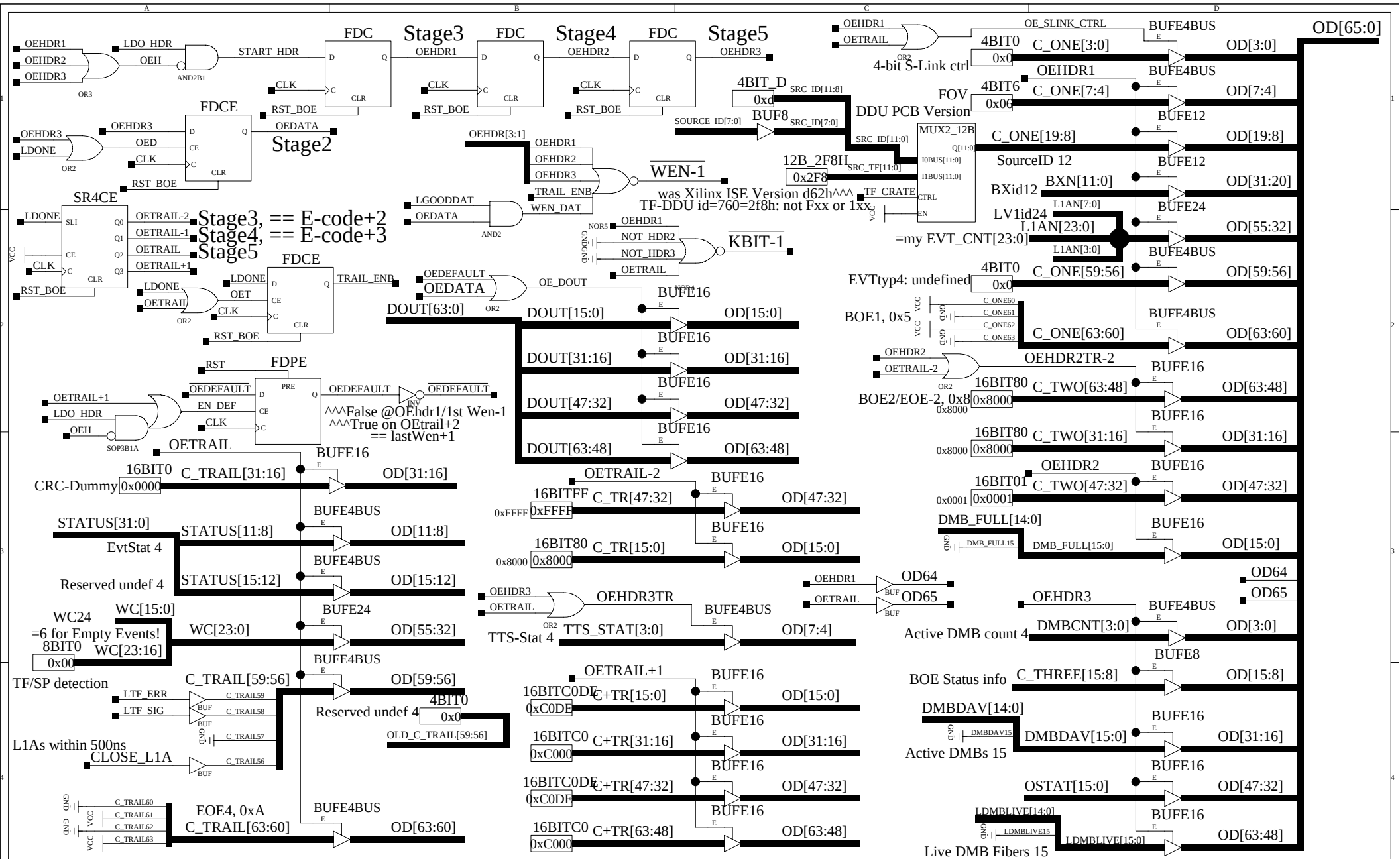
CSC case by LTRG_Trail+1?

TMB/ALCT need Err Reg's for CSC/EVT

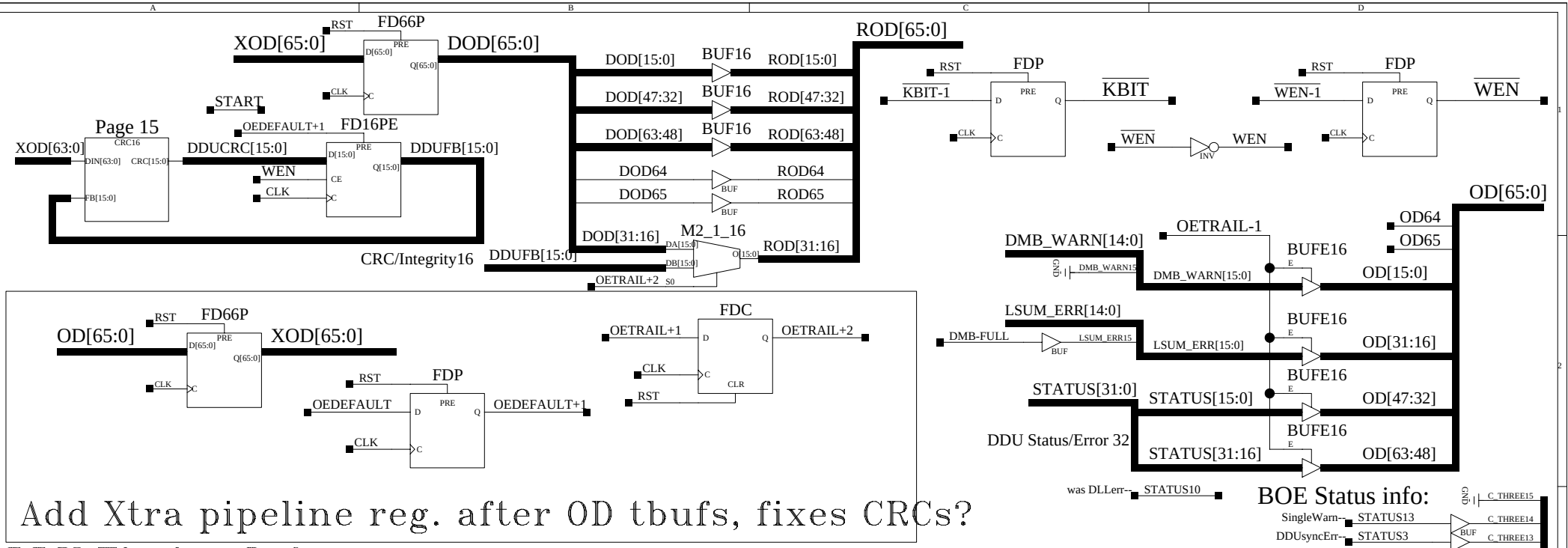
CRC: Evt WC: Evt L1err: Evt

TMBerr: CSC&Evt ALCTerr: CSC&Evt

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: Trigger Error Registers DDU Controller CMS CSC Electronics	BY: JRG DATE: 8-12-2008_15:27	PARENT PAGE: 2 FILE: STAGE2 . 9
		PROJECT: D785C	PAGE: 12H



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: DDU Header/Trailer Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2
		DATE: 8-14-2008_16:22	PROJECT: D785C
		FILE: STAGE2 . 10	PAGE: 12I



Add Xtra pipeline reg. after OD tbufs, fixes CRCs?

DDU Timing Info

DDUctrl to InFIFO signals: 2" – 4", .3ns – .6ns

IRCLK has 4 loads, may slow signal by 0.1–0.5ns?

CKFBout has normal drive, IRCLK has ~1.1ns Faster drive

FPGA I/O Delays (lvcmos33, ns)

IBUF: 0.92

IFD set/hold: 0.92/–0.12 Clk to Q: 0.65

OBUF: 2.33

OFD set/hold: 0.26/0.14 Clk to Q: 2.41

*modifiers for drive/slew settings:

6mA: add 2.60 for Slow, 1.28 for Fast
8mA: add 1.69 for Slow, 0.46 for Fast
12mA: add 1.18 for Slow, 0.26 for Fast
16mA: add 0.52 for Slow, 0.02 for Fast
24mA: +0.44 for Slow, –0.08 for Fast

FPGA CLB Delays (ns)

4–FG: 0.32 5–FG: 0.65

FD set/hold: 0/0.14 Clk to Q: 0.38

Sync. set–rst setup: 0.60

Async. pre–clr to Q: 1.25

SR16 Clk to Q: 3.12

SR32 Clk to Q: 3.49

SI set/hold: 0.34/0.01 Clk to Q11 (low state) 3.22–3.34 3.28

TI FIFO I/O Delays (ns)

Measured on FIFO test board

RCLK to Empty (low state) Vcc: 3.38V 3.04V

Max: 3.6, Min: 2.5 3.02–3.18 3.20–3.29

to Not Empty (high state) 3.22–3.34 3.23–3.31

RCLK to Q11 False (low state)

Max: 4.3, Min: 2.5 3.32–3.62 3.40–3.64

to Q11 True (high state) 3.31–3.87 3.51–4.06

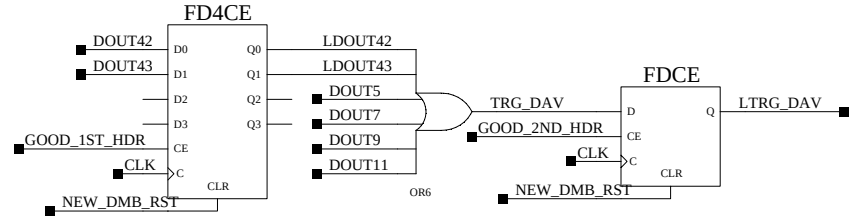
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

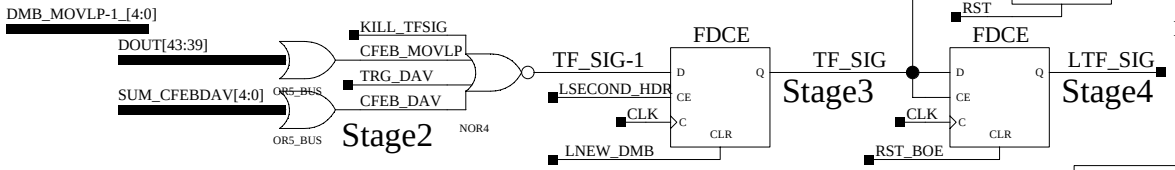
TITLE: DDU CRC Logic for SLINK/C.D.F. Compatibility
DDU Controller
CMS CSC Electronics

BY: JRG | PARENT PAGE: 2 | PROJECT: D785C

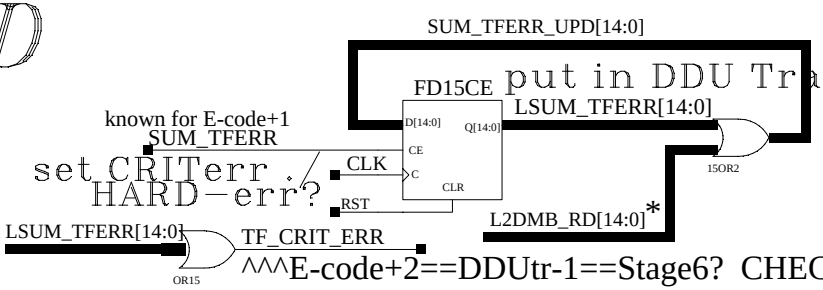
DATE: 5-15-2009_13:47 | FILE: STAGE2 . 11 | PAGE: 12J

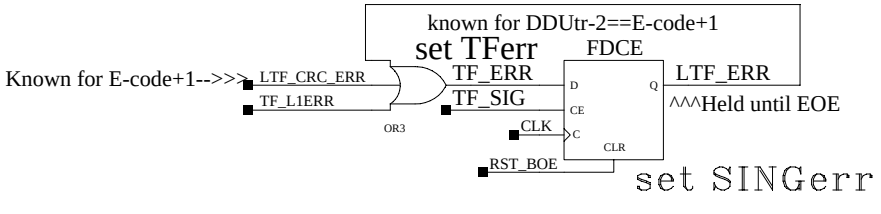
Check for Track Finder signal, record TF errors

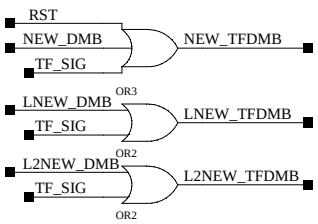


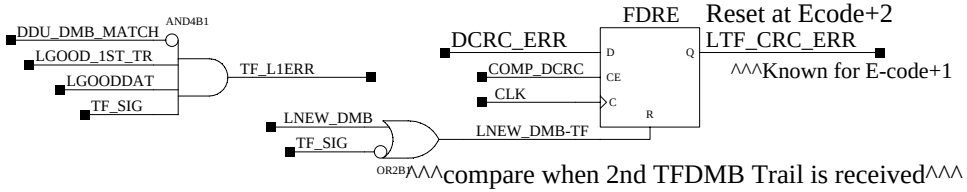


END

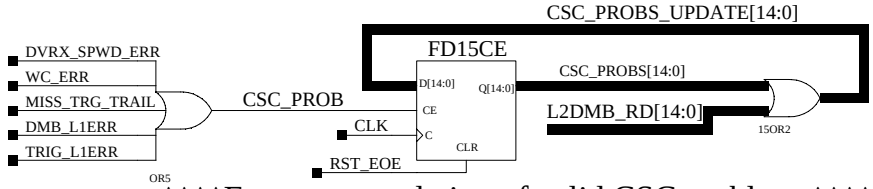


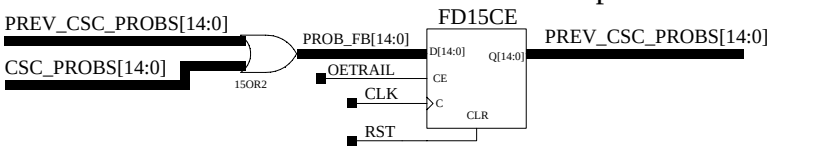


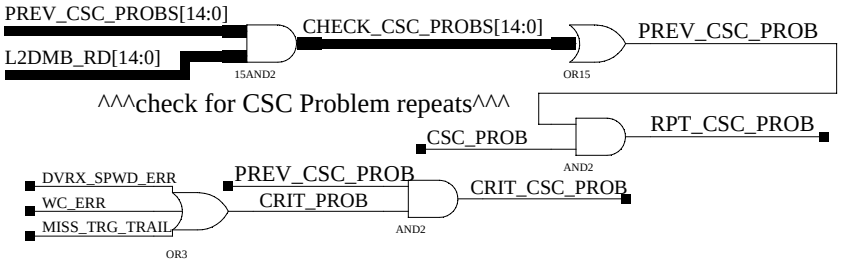




CSC Problem Repeat checking



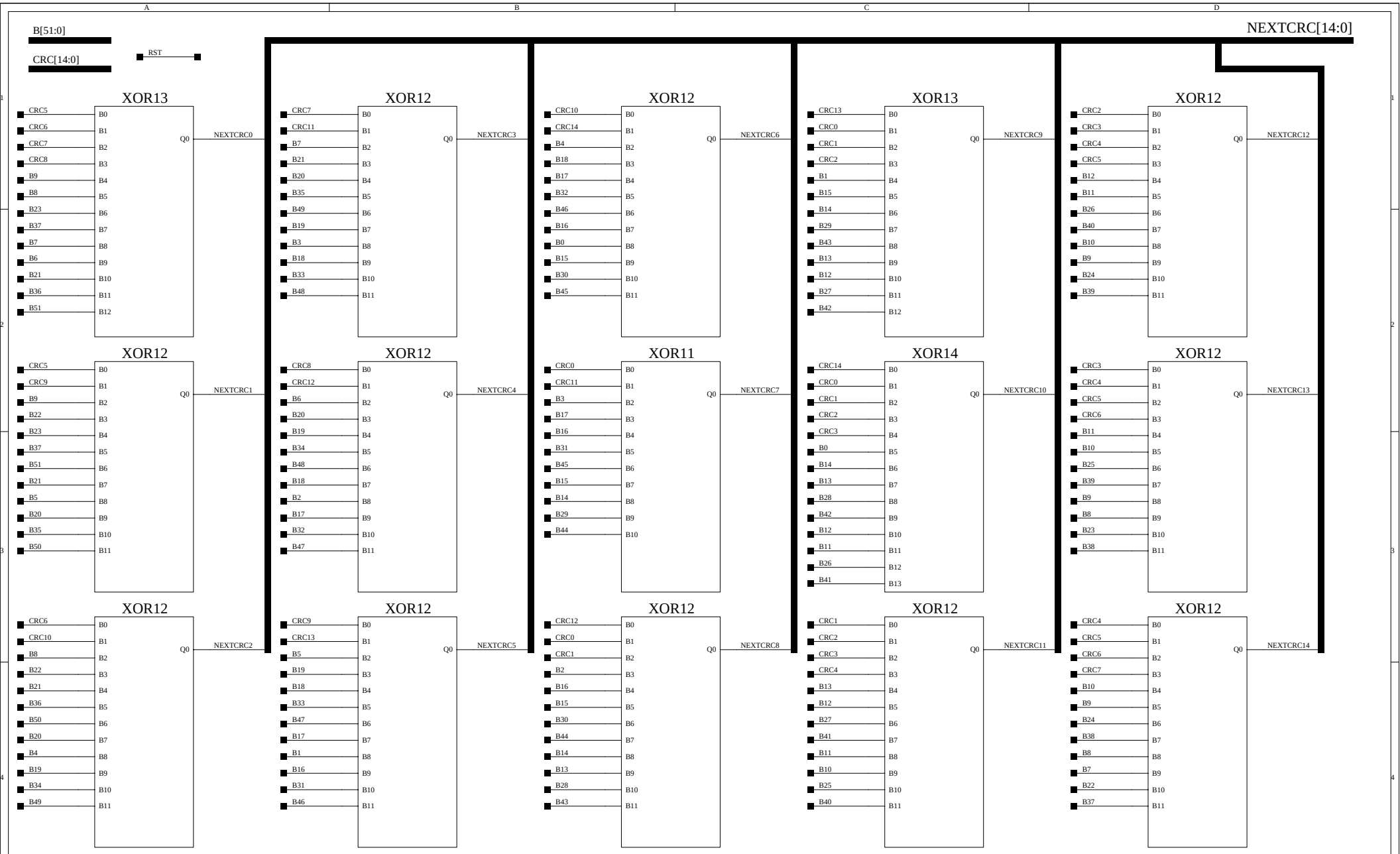




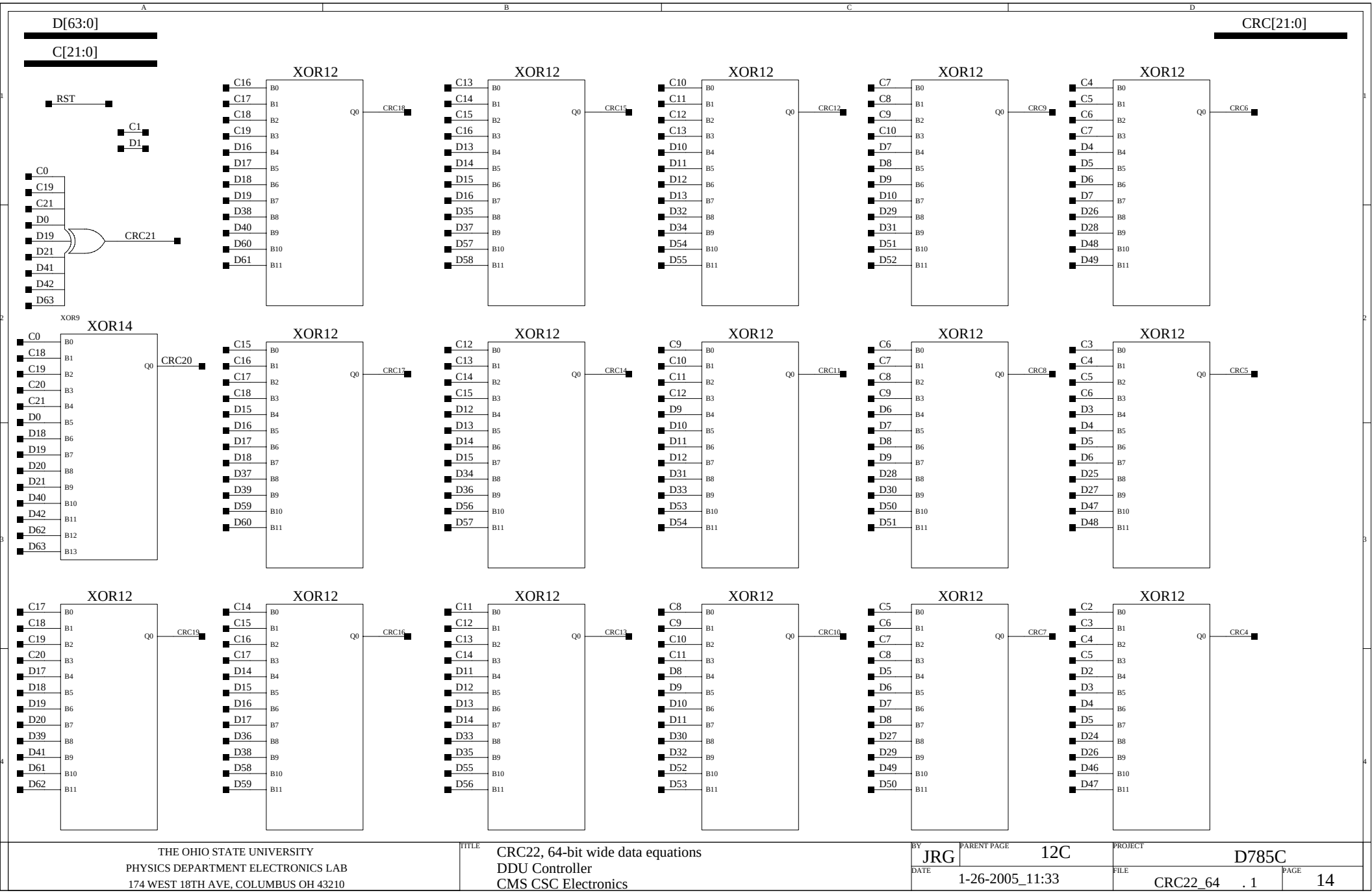
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Stage 2 Logic: DMB Status Checks
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
8-12-2008_17:18	STAGE2 . 12	12K



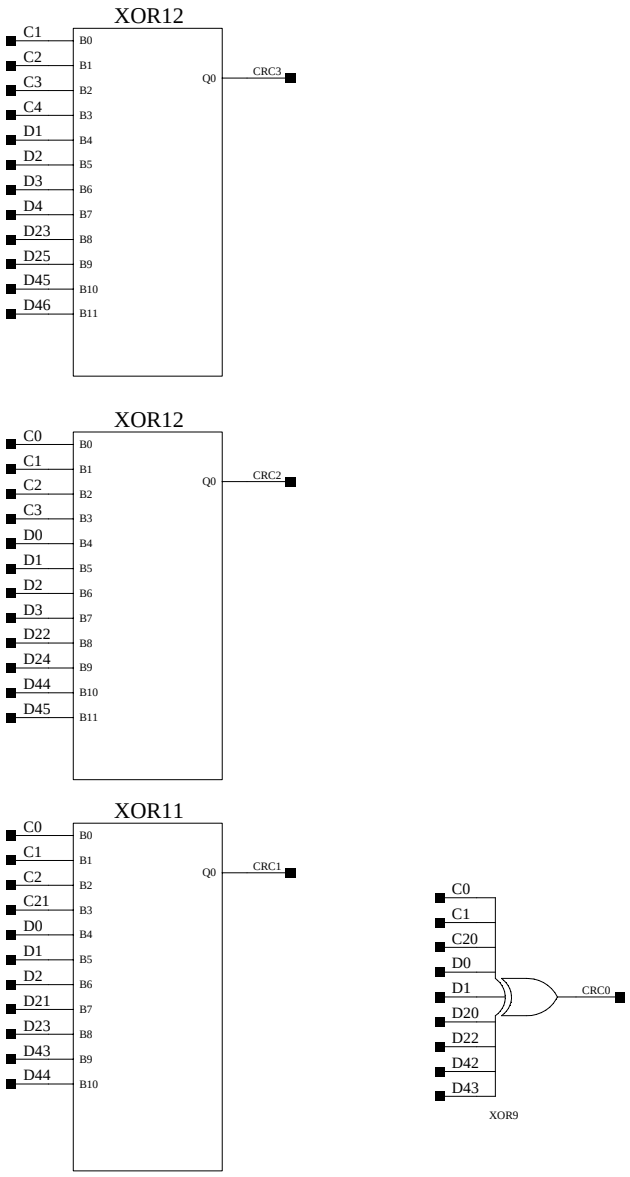
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC15, 52-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 12B	PROJECT: D785C
		DATE: 1-26-2005_11:33	FILE: CRC15_52 . 1	PAGE: 13



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

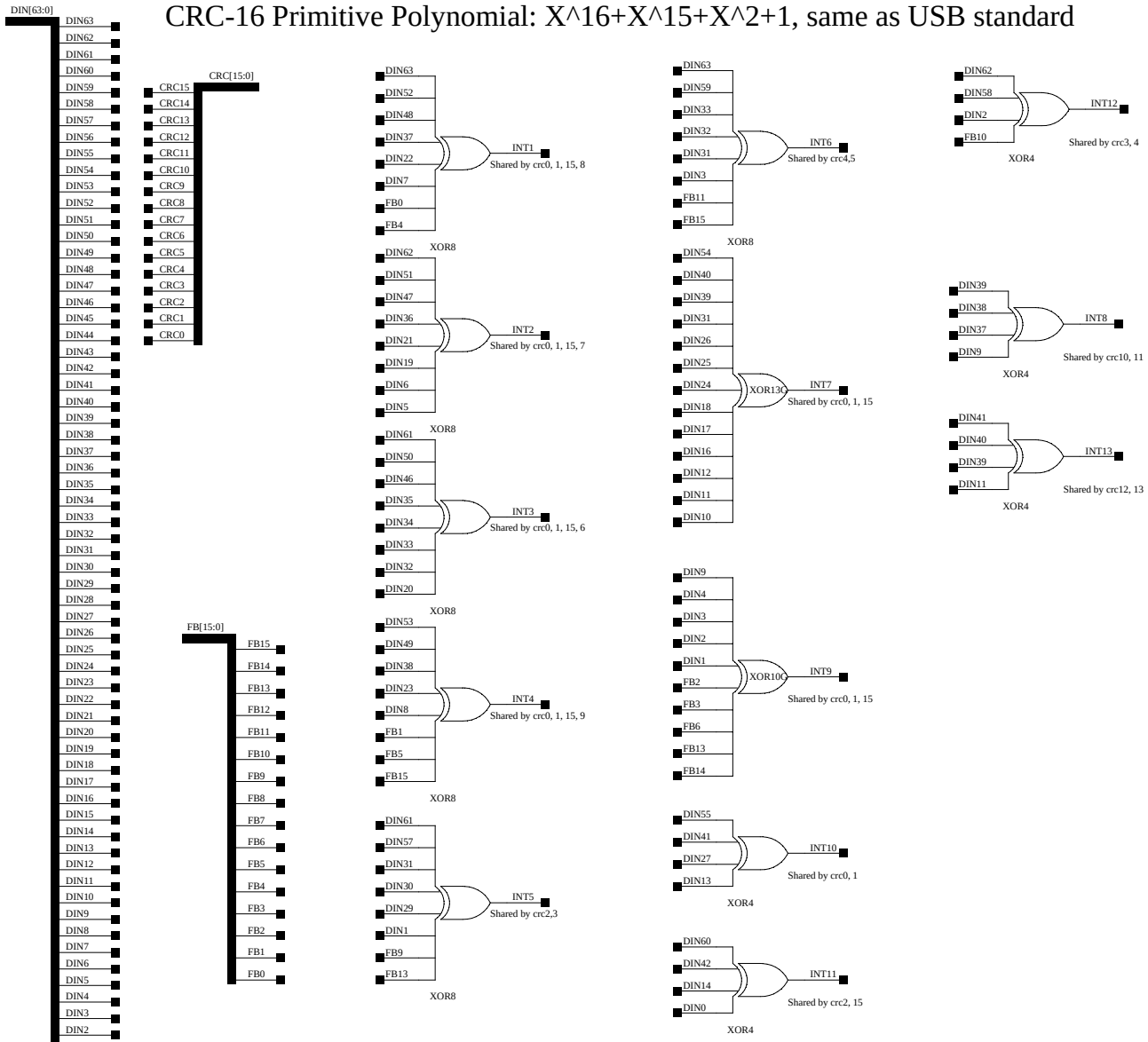
TITLE: CRC22, 64-bit wide data equations
DDU Controller
CMS CSC Electronics

BY: JRG | PARENT PAGE: 12C | PROJECT: D785C
DATE: 1-26-2005_11:33 | FILE: CRC22_64 . 1 | PAGE: 14

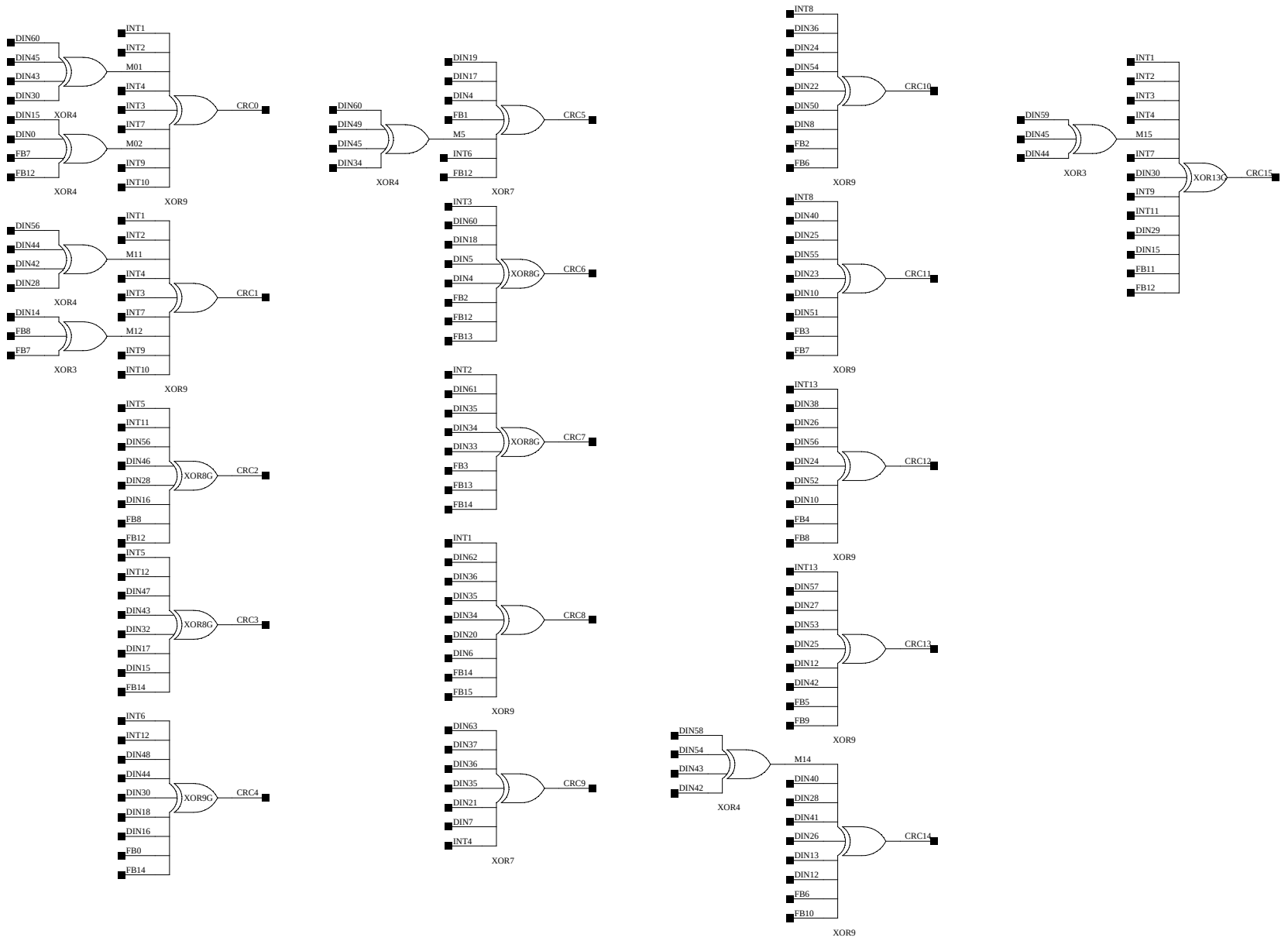


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC22, 64-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:34	PARENT PAGE: 12C FILE: CRC22_64 . 2	PROJECT: D785C PAGE: 14A

CRC-16 Primitive Polynomial: X^16+X^15+X^2+1, same as USB standard



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	SLINK CRC16 Calculation, common components DDU Slink Interface FPGA CMS CSC Electronics	BY GU	PARENT PAGE 12F	PROJECT D785C
			DATE 2-7-2005_17:50	FILE CRC16 . 1	PAGE 15



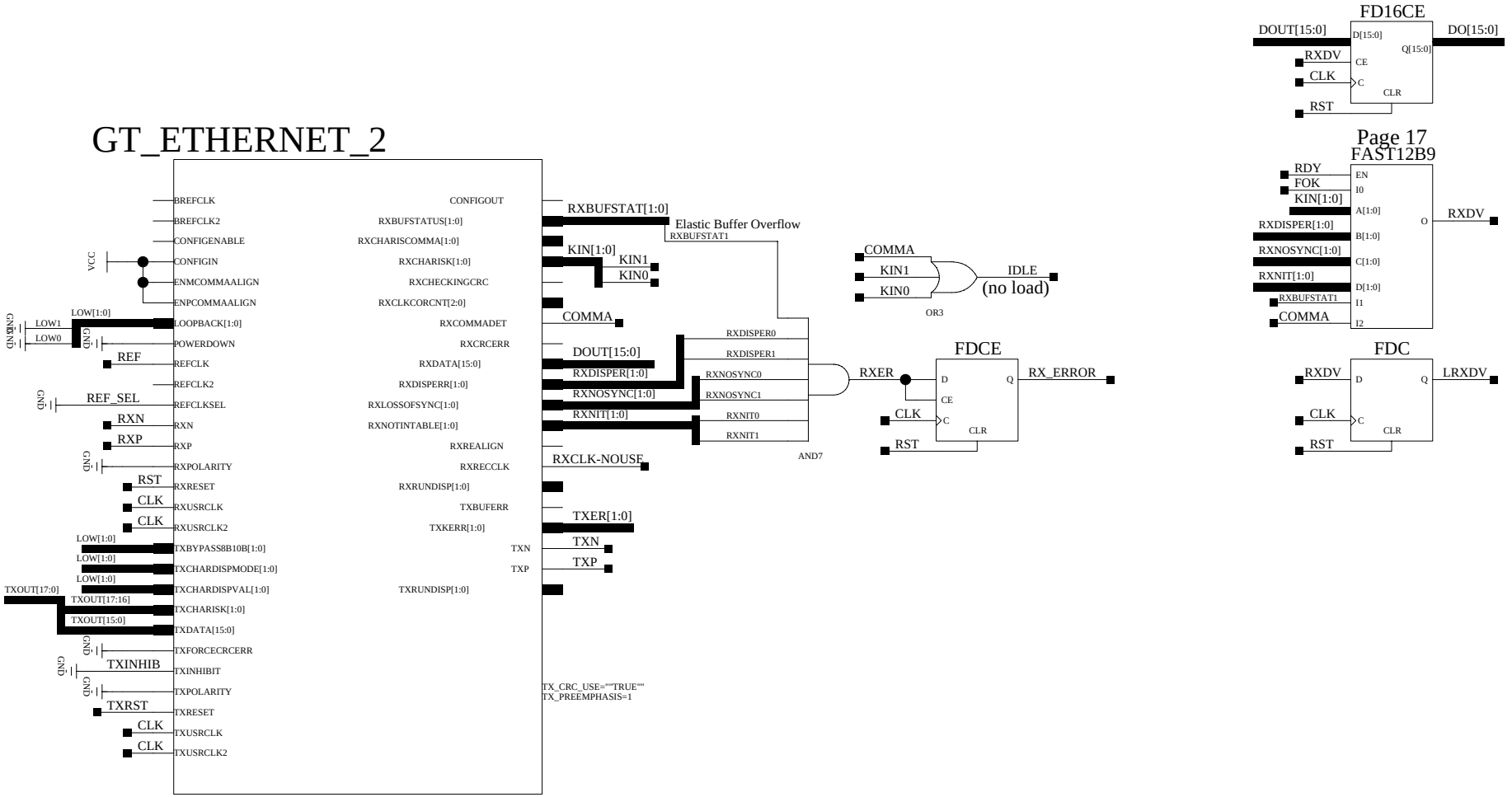
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: SLINK CRC16 Calculation
DDU Slink Interface FPGA
CMS CSC Electronics

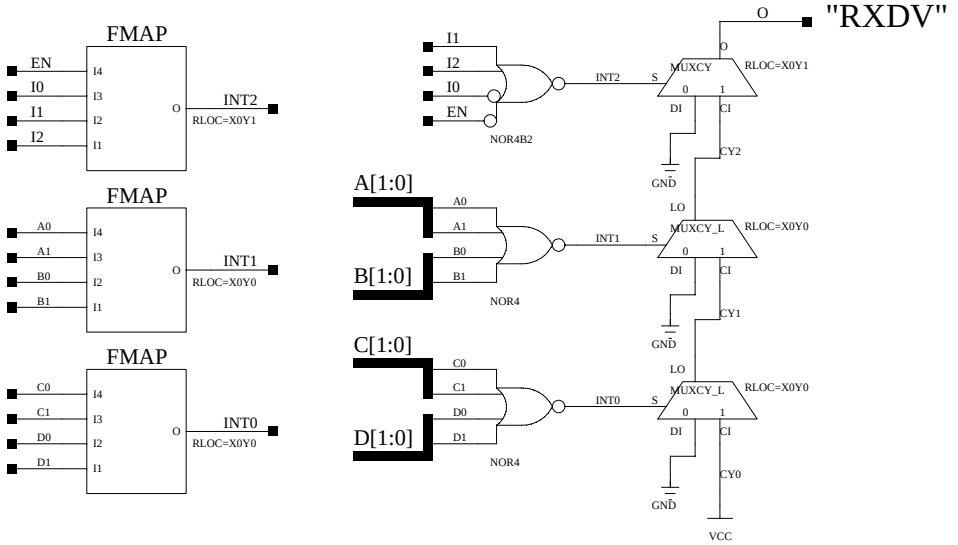
BY	PARENT PAGE	PROJECT
GU	12F	D785C
DATE		FILE / PAGE
2-7-2005_17:50		CRC16 . 2 / 15A

Outgoing packets must have 1010... preamble logic and End Packet logic.
Incoming packets must also exclude Preamble and CRC in RxDV logic.

---> Not done yet! Consider a counter to skip 1st ~12 bytes after K word. Skip 4 CRC bytes too.



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Gigabit Ethernet Tranceiver DDU Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2E	PROJECT D785C
		DATE 7-18-2005_16:14	FILE OUT_GBE . 1	PAGE 16

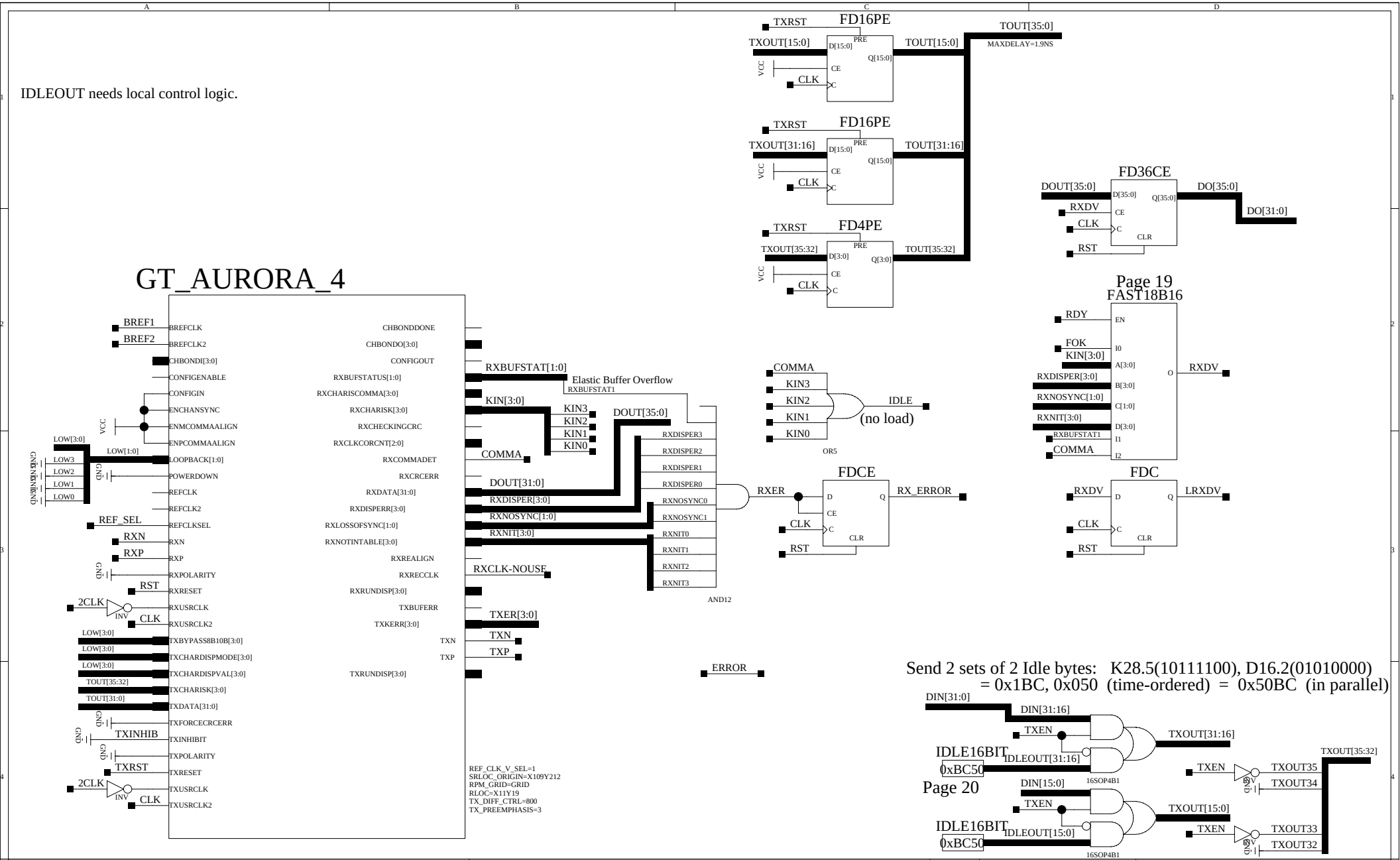


XILINX

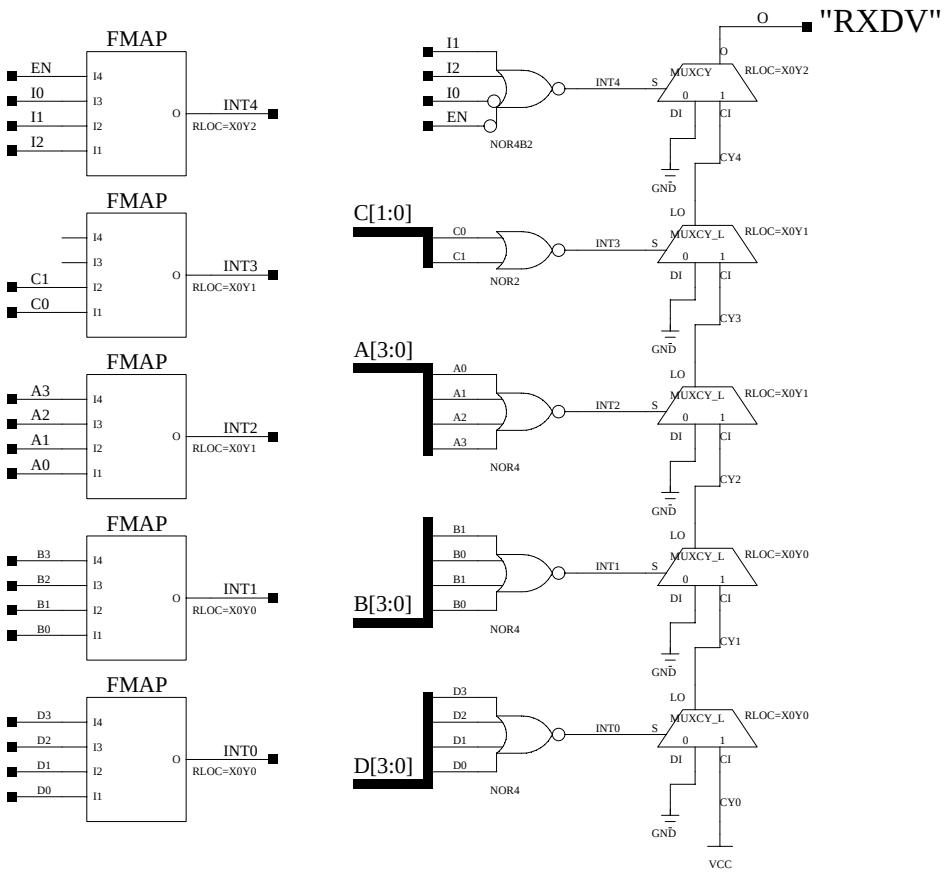
JRG

Title:	FAST12B9		
Comments:	Custom Logic for DDU similar to: AND12B9		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A

IDLEOUT needs local control logic.



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Multi Gigabit Tranceiver DDU Controller Logic CMS CSC Electronics	BY: JRG PARENT PAGE: 2E DATE: 7-18-2005_16:15	PROJECT: D785C FILE: OUT_UNIT . 1 PAGE: 18



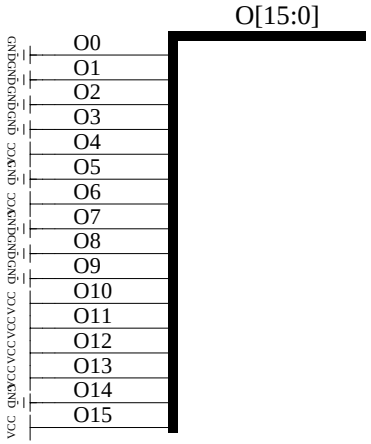
XILINX

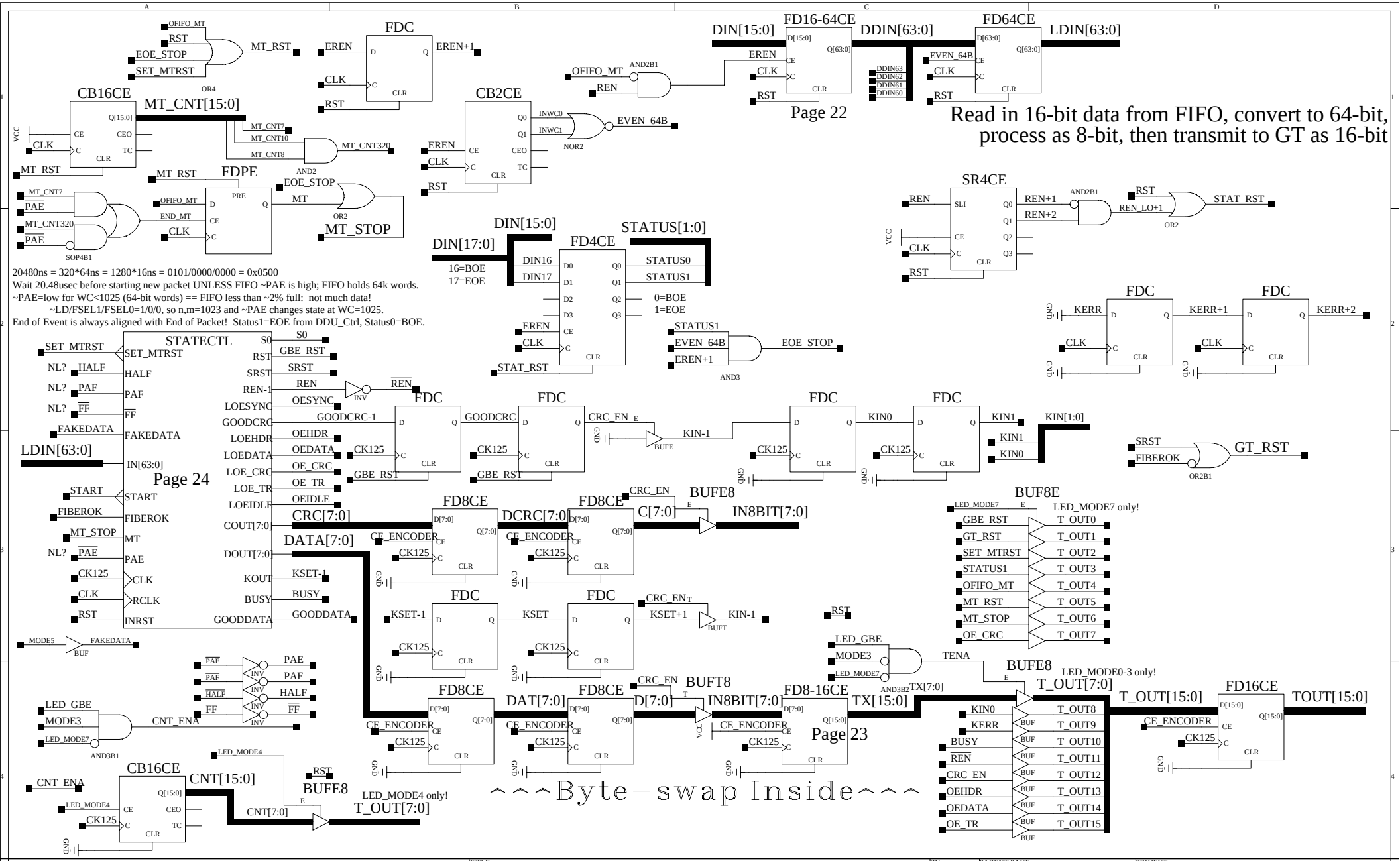
JRG

Title:	FAST13B10		
Comments:	Custom Logic for DDU similar to: AND12B10 with an OR2 (allows ON to override)		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A

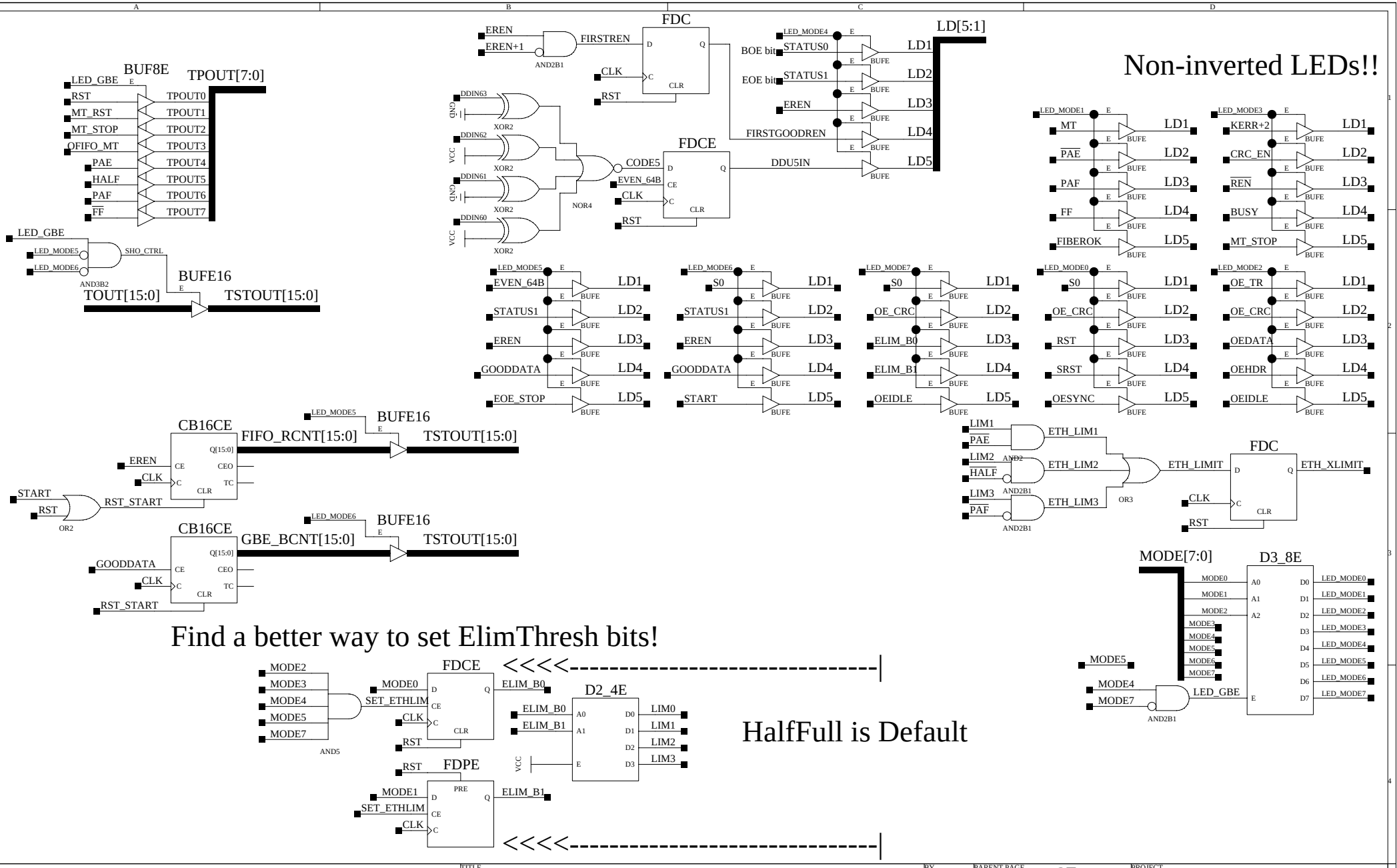
Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)
= 0x1BC + 0x050 (time-ordered)
= 0xBC50 (in parallel)

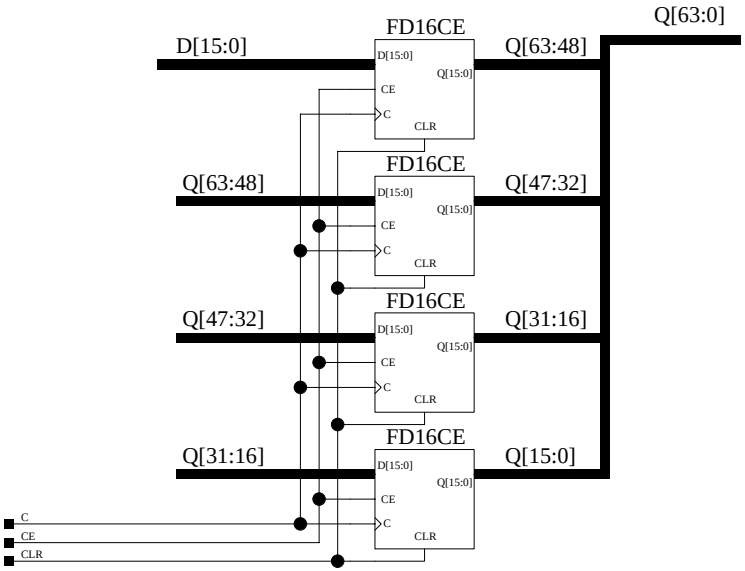




THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Ethernet Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 12-8-2006_14:29	PARENT PAGE: 2F FILE: ETHCNTRL . 1
		PROJECT: D785C	PAGE: 21



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Ethernet Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2F	PROJECT: D785C	
		DATE: 12-8-2006_14:29		FILE: ETHCNTRL . 2	PAGE: 21A

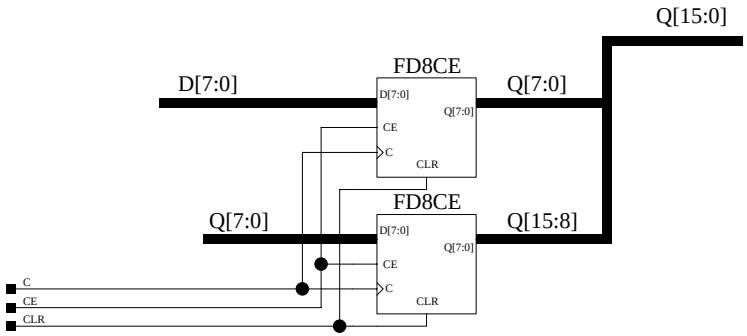


XILINX JRG

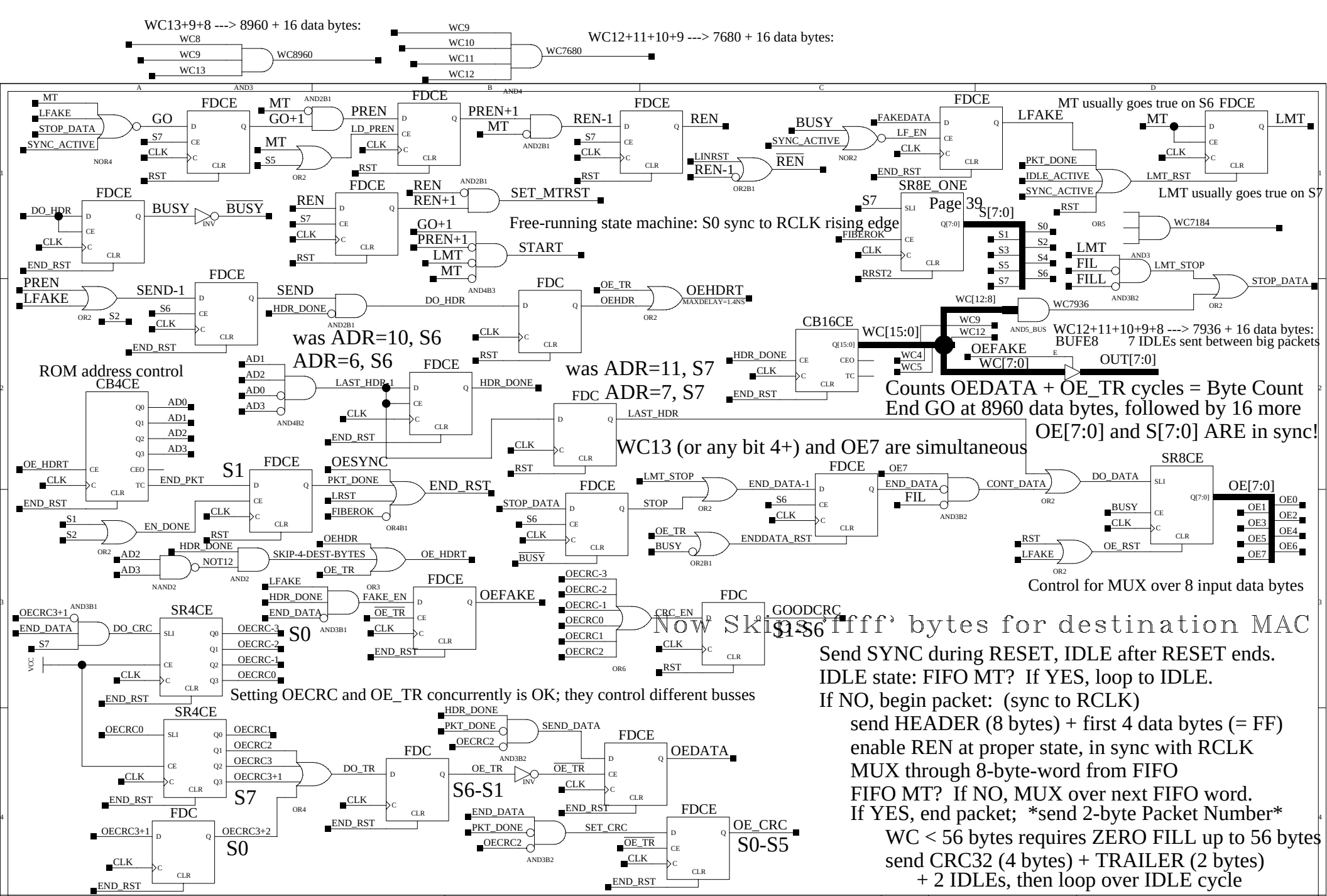
Title: VIRTEX Family FD16-64CE Macro

Comments: 16-64 Bit Bus Matching Register with Asynchronus Clear and Chip Enable

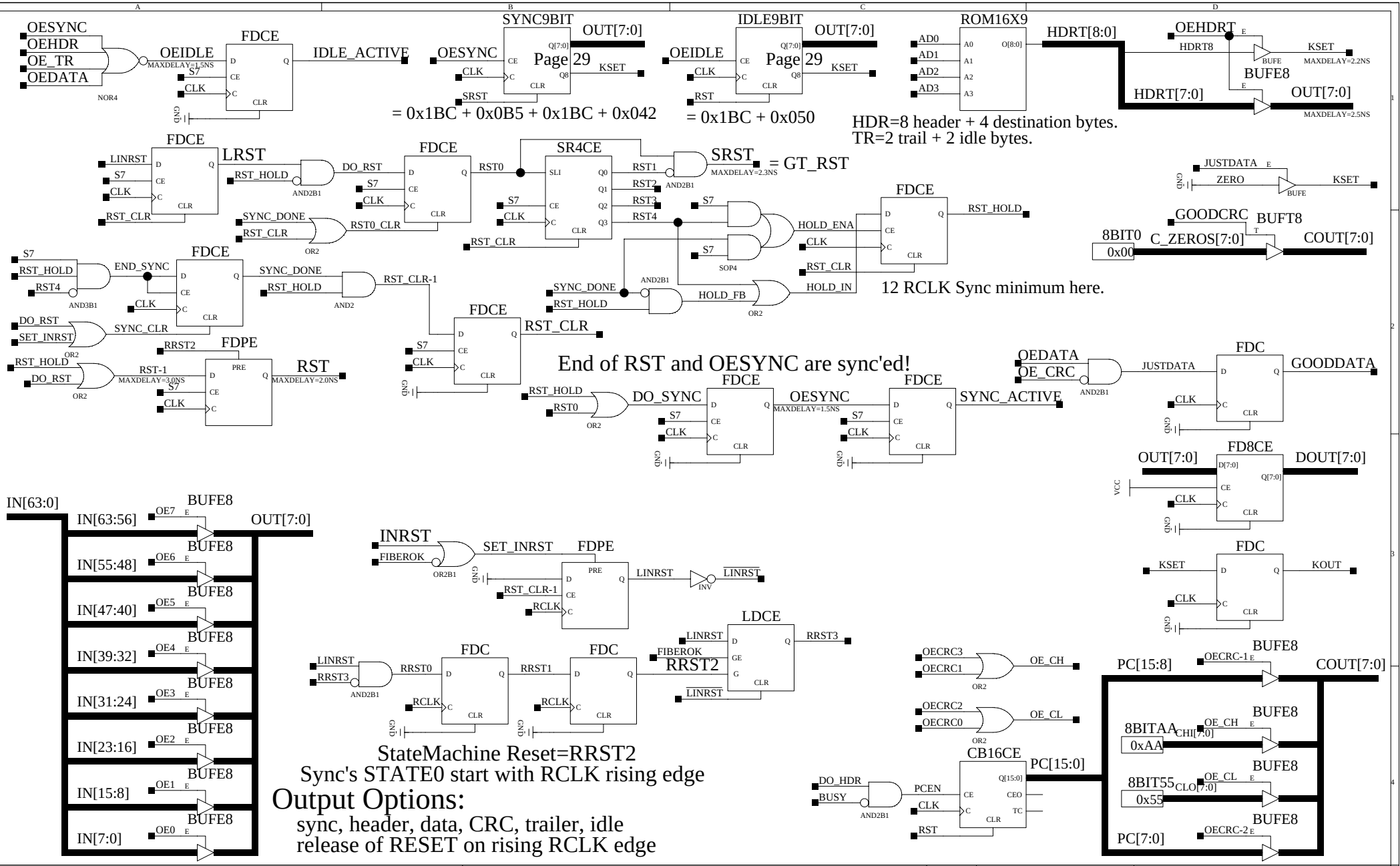
Date:	2nd February 2004	Ver:	1
Sheet Size: B		Rev:	A



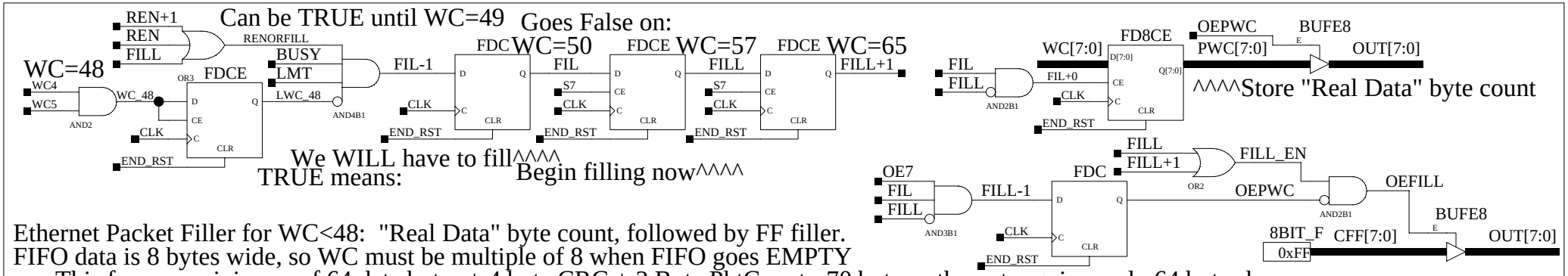
XILINX	JRG	
Title:	VIRTEX Family FD8-16CE Macro	
Comments:	8-16-Bit Bus Matching Register with Asynchronus Clear and Chip Enable	
Date:	4th February 2004	Ver: 1
Sheet Size: B		Rev: A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 7-29-2005_13:26	PARENT PAGE: 21A FILE: STATECTL . 1 PROJECT: D785C PAGE: 24



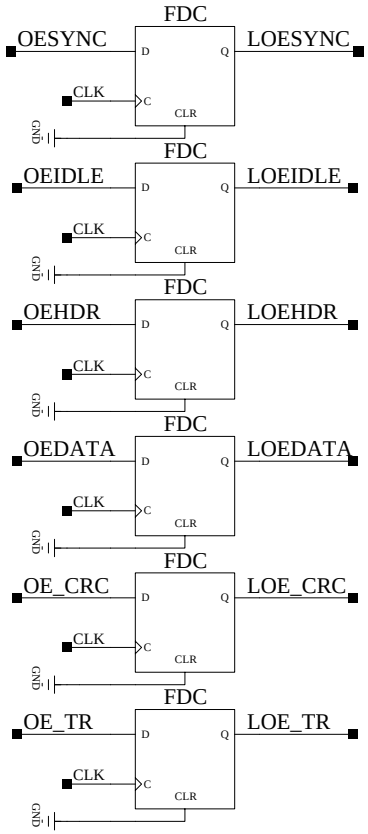
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 7-18-2005_16:19	PARENT PAGE: 21A FILE: STATECTL . 2
		PROJECT: D785C	PAGE: 24A



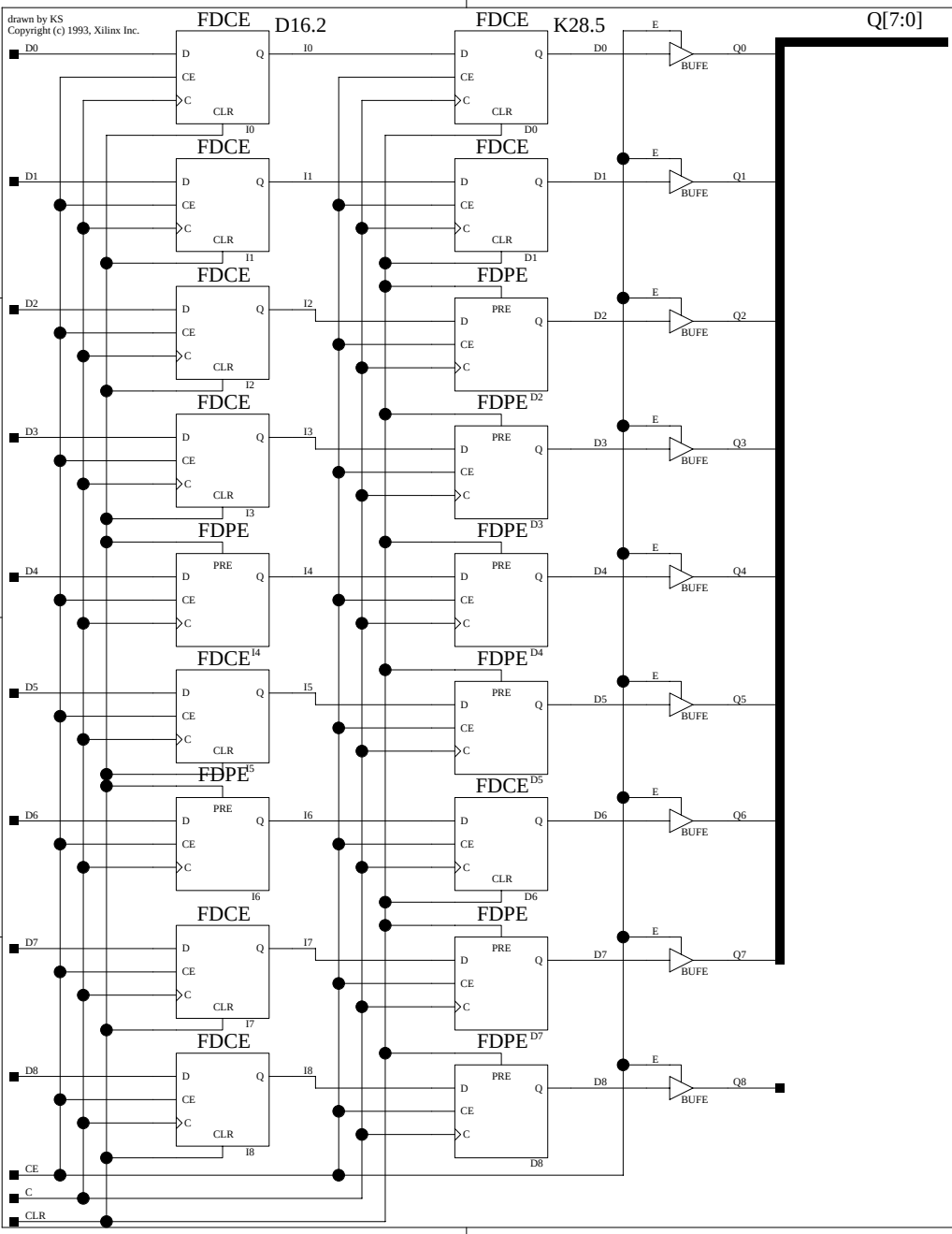
Ethernet Packet Filler for WC<48: "Real Data" byte count, followed by FF filler.
FIFO data is 8 bytes wide, so WC must be multiple of 8 when FIFO goes EMPTY
This forces a minimum of 64 data bytes + 4 byte CRC + 2 Byte PktCount= 70 bytes; ethernet requires only 64 bytes here.
Overfill ensures at least 15 FF bytes (after the "Real Data" byte count) in a "filled" packet.

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE	State Machine Control DDU Ethernet Logic CMS CSC Electronics
BY	JRG
PARENT PAGE	21A
PROJECT	D785C
DATE	1-26-2005_11:50
FILE	STATECTL . 3
PAGE	24B



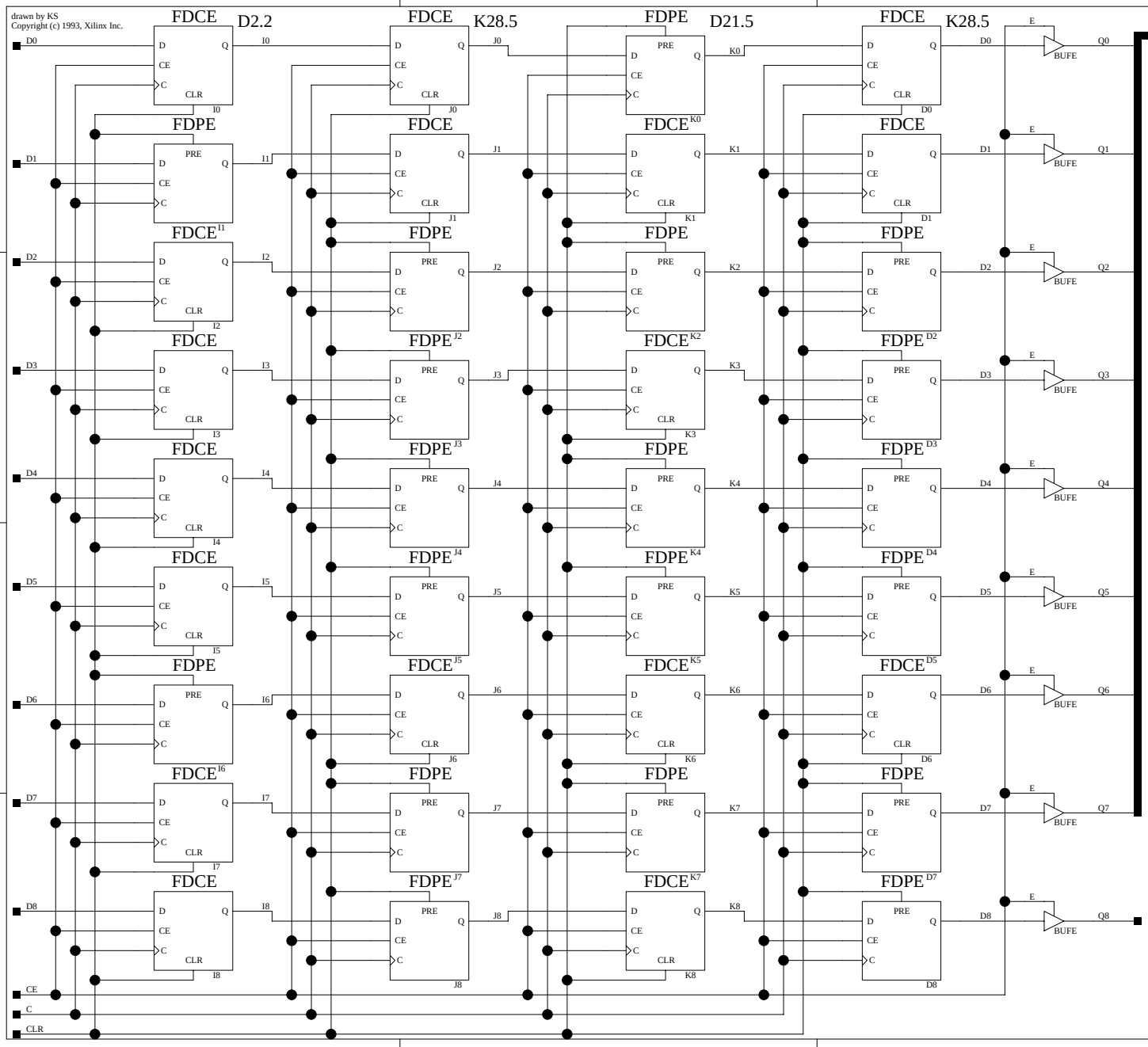
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE JTAG Control Signals DDU Ethernet Logic CMS CSC Electronics	BY JRG	PARENT PAGE 21A	PROJECT D785C
		DATE 5-25-2005_15:01	FILE STATECTL . 4	PAGE 24C



Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)
= 0x1BC + 0x050

Title:	VIRTEX Family Ethernet Idle Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Idle cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A

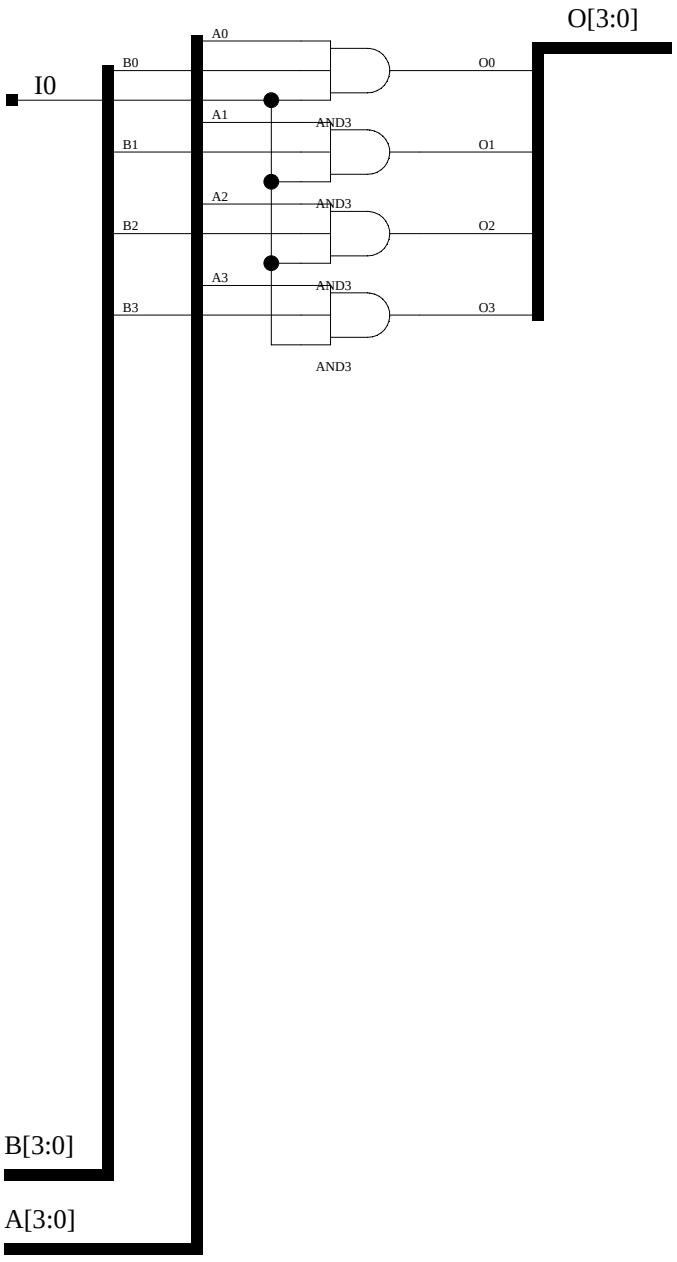


Send 4 Sync bytes:

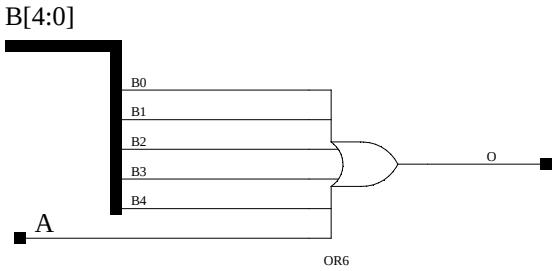
K28.5(10111100)+D21.5(010110101)
+K28.5(10111100)+D2.2(001000010)
= 0x1BC + 0x0B5 + 0x1BC + 0x042

XILINX

Title:	VIRTEX Family Ethernet Sync Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Sync cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A



Title:	VIRTEX Family 4-AND3COM1 Macro
Comments:	4-AND3 Bus Gate plus 1 common bit
	JRG
Date:	1st October 2003
Ver:	1
Sheet Size: A	
Rev:	A

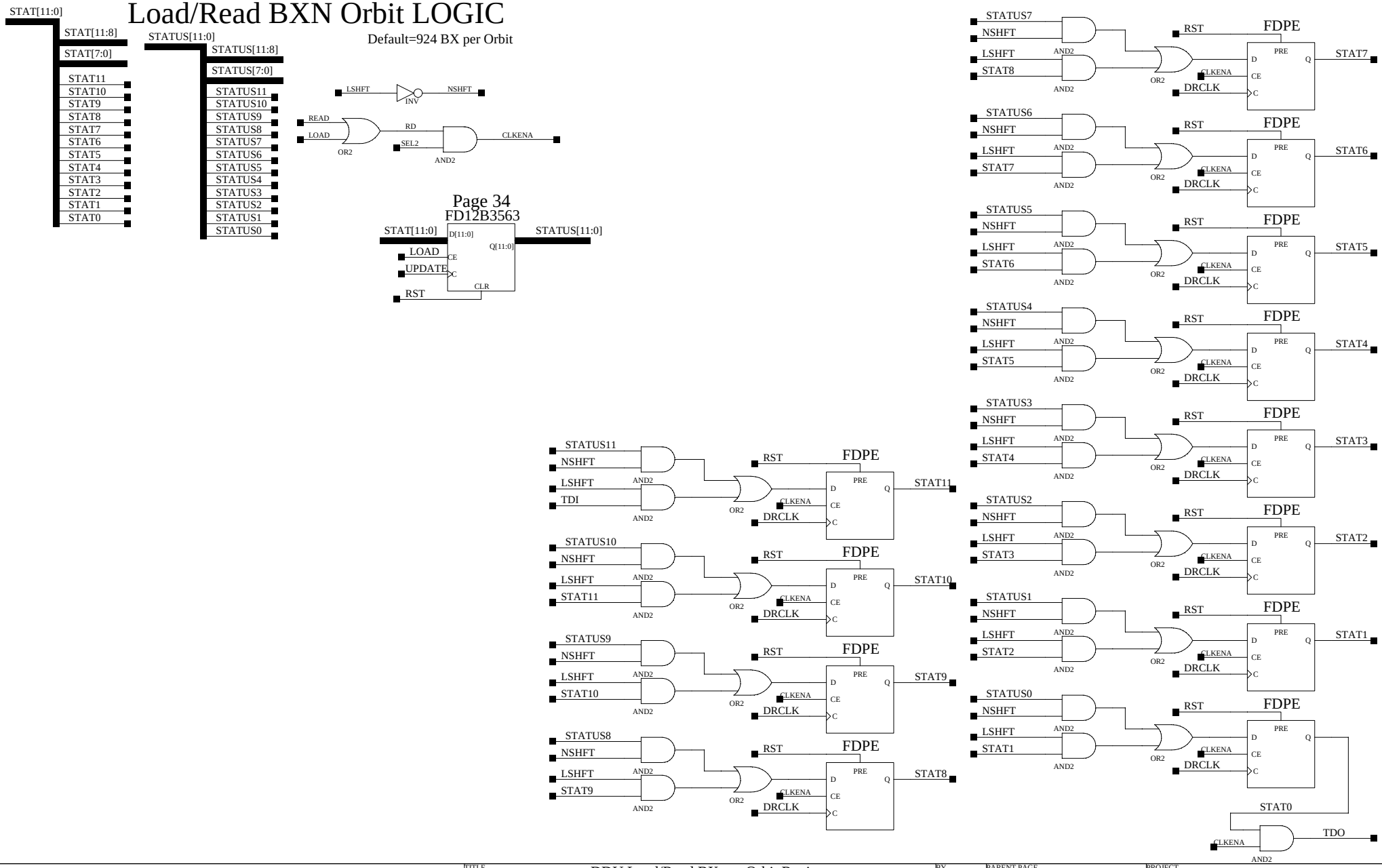


Title:	VIRTEX Family OR5+1 Macro
Comments:	OR5 Bus Gate w/Common
	JRG
Date:	27th December 2001
Ver:	1
Sheet Size: A	
Rev:	A

drawn by KS

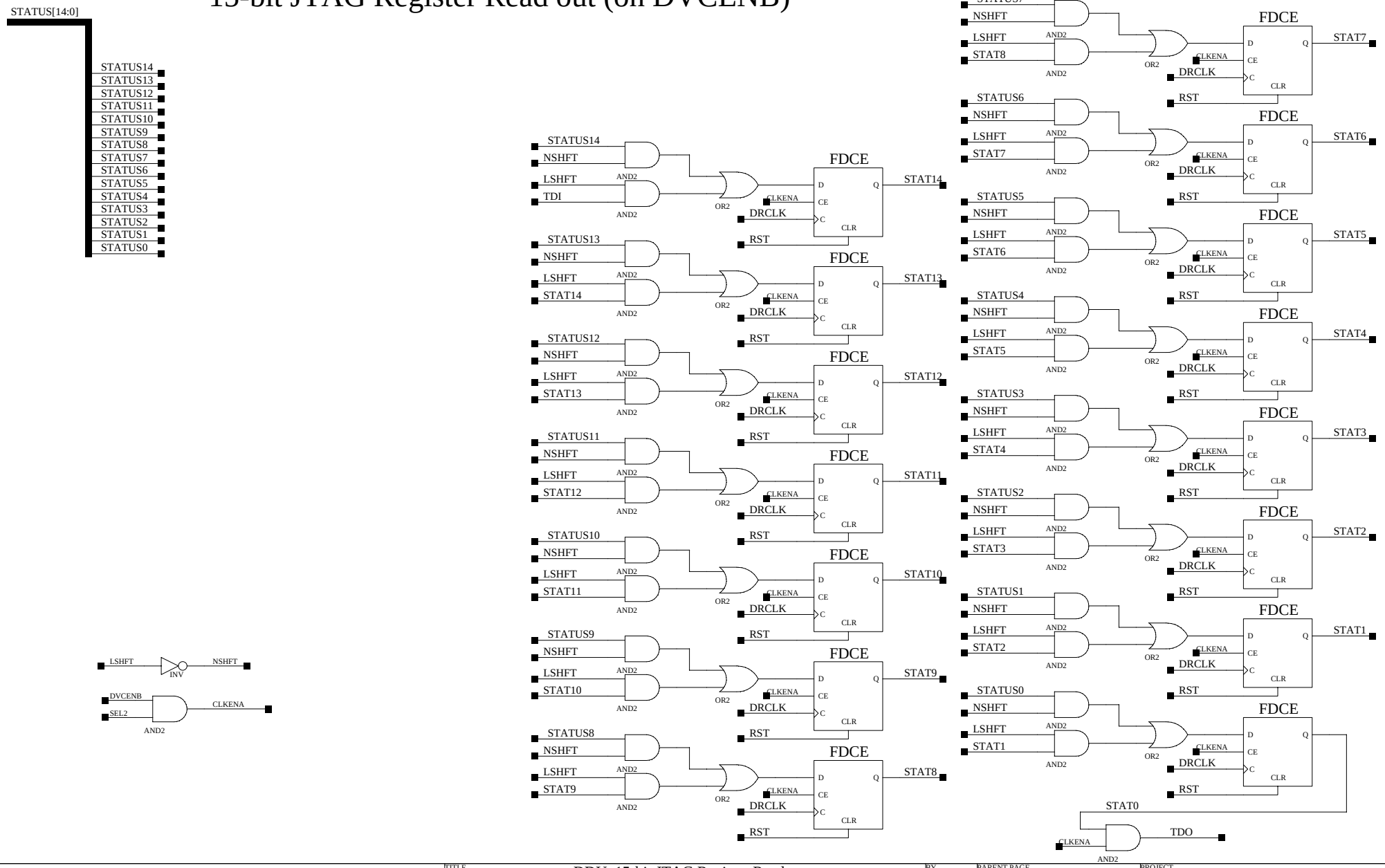
Load/Read BXN Orbit LOGIC

Default=924 BX per Orbit



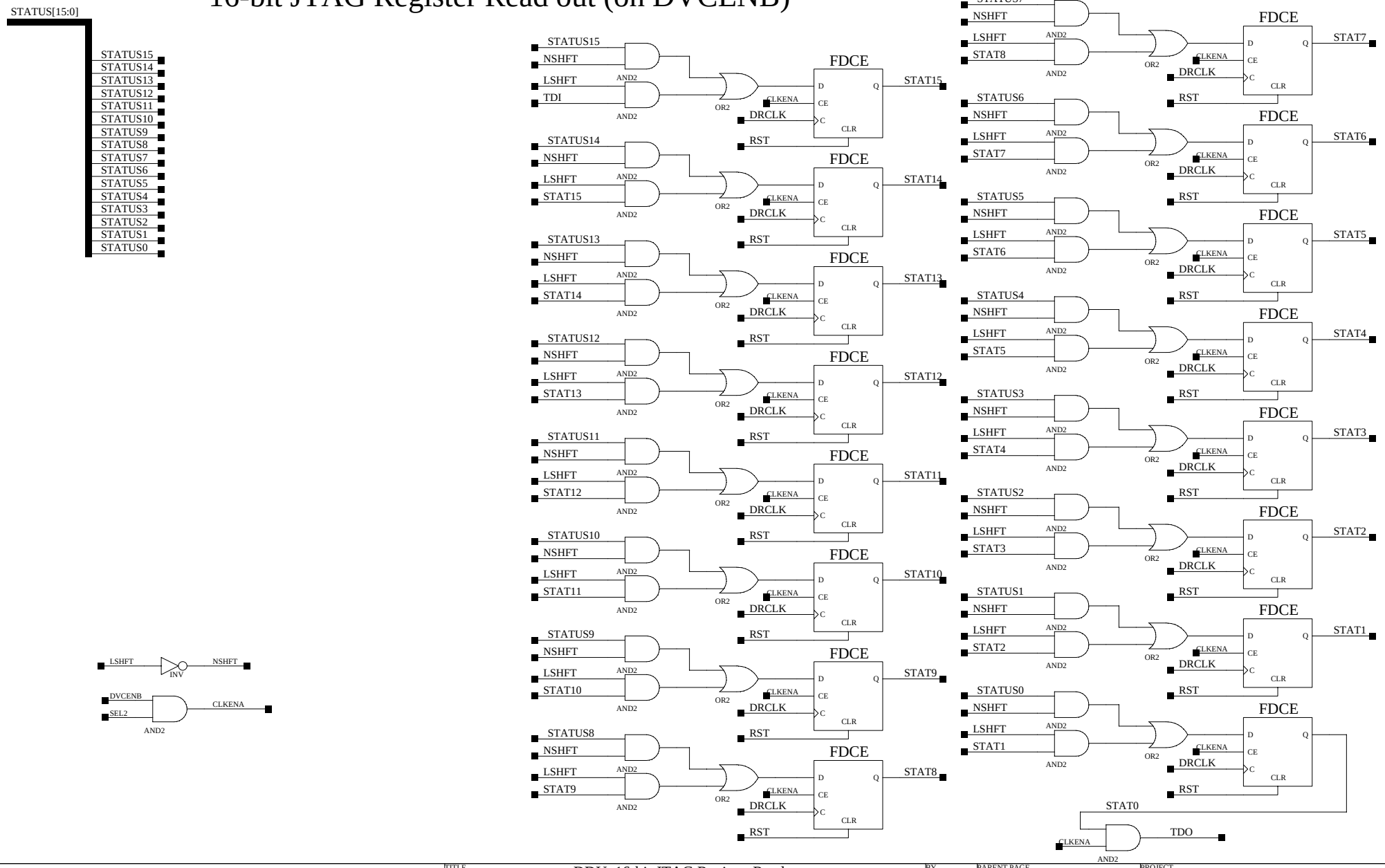
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	DDU Load/Read BX per Orbit Register DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 3F	PROJECT D785C
			DATE 9-19-2005_9:55	FILE BXN_REG . 1	PAGE 29

15-bit JTAG Register Read out (on DVCENB)



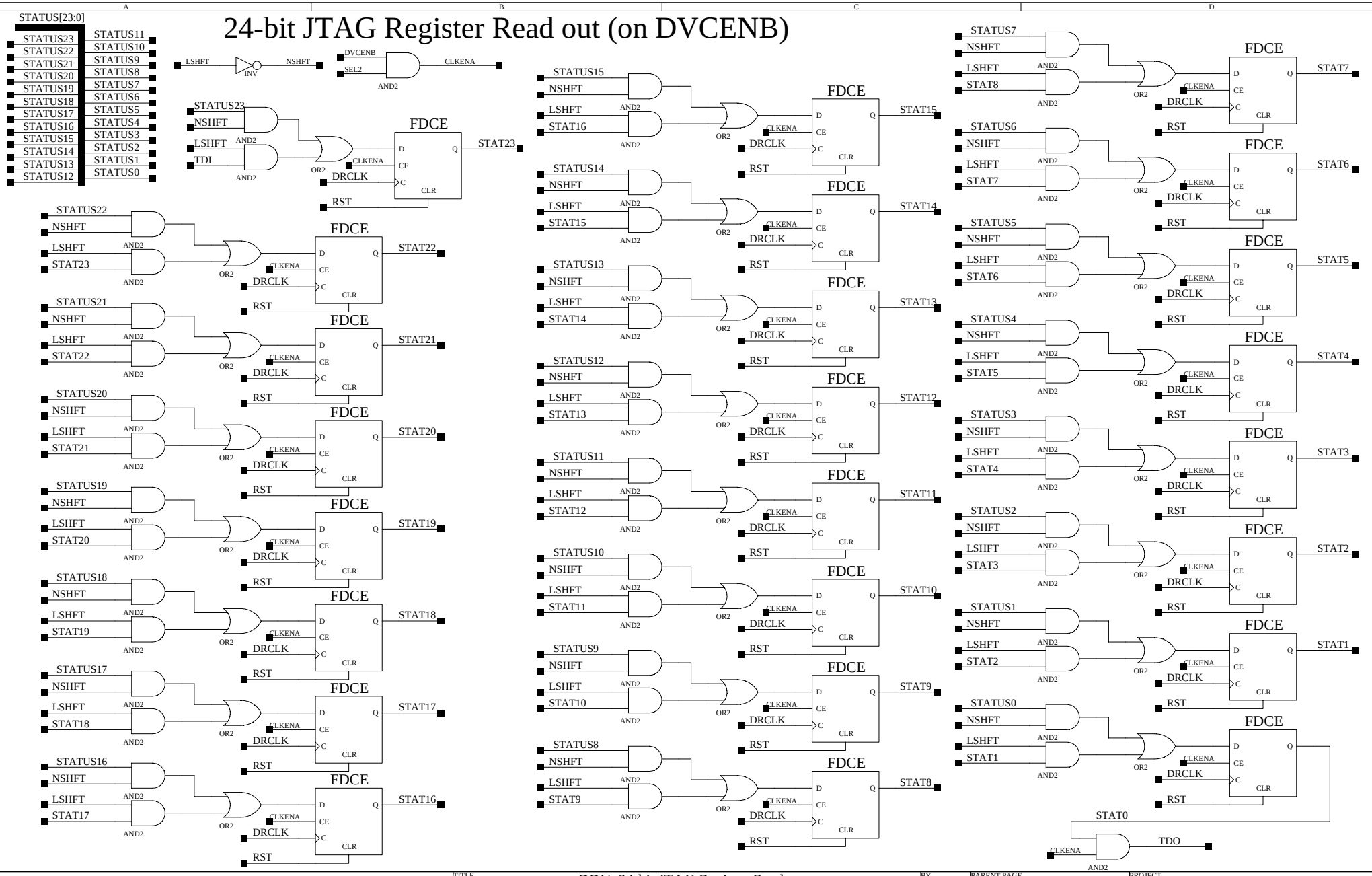
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 15-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:16	FILE: CHECK_15_1	PAGE: 31

16-bit JTAG Register Read out (on DVCENB)



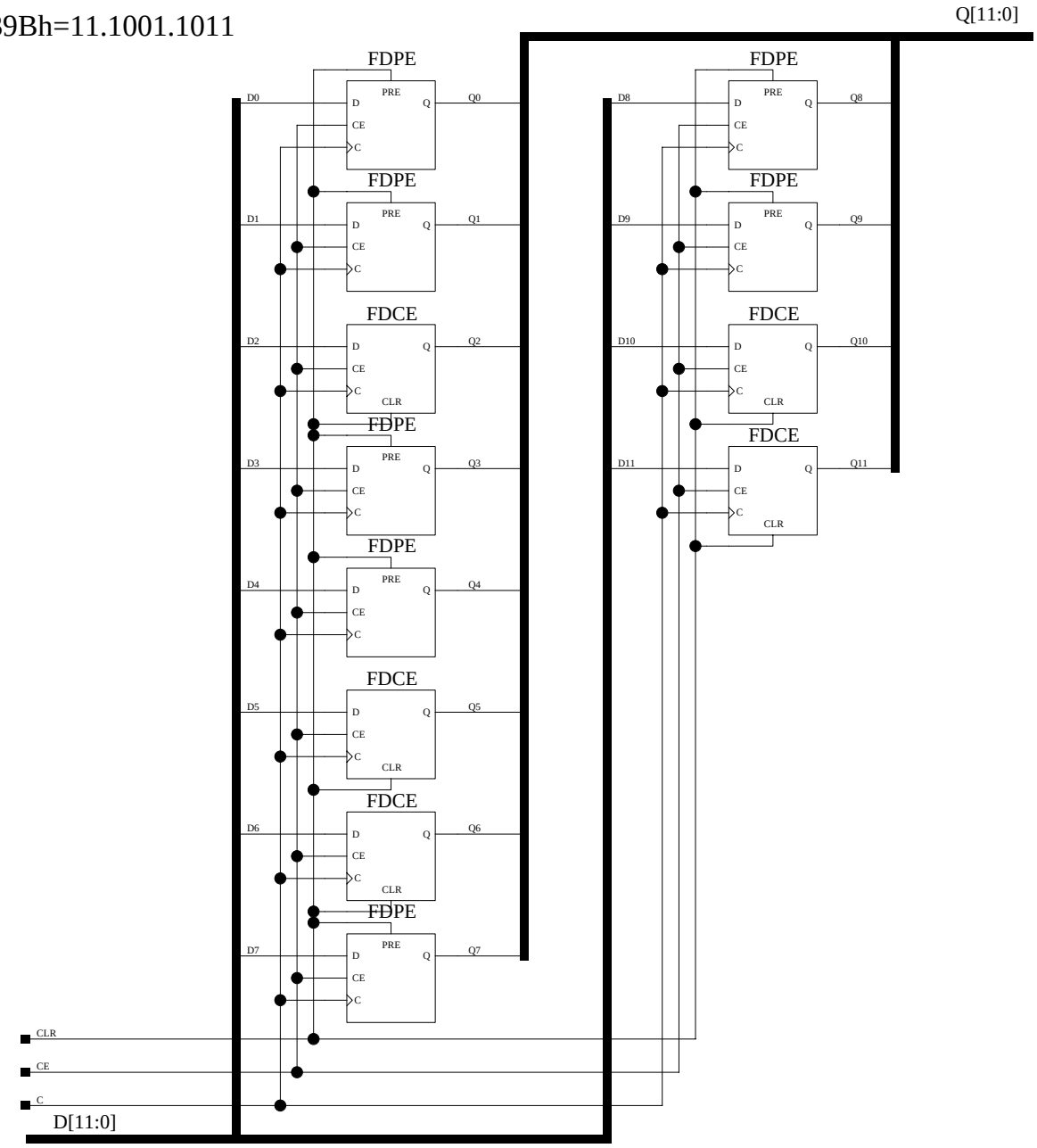
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 16-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:16	FILE: CHECK_16 . 1	PAGE: 32

24-bit JTAG Register Read out (on DVCENB)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 24-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_12:17	PARENT PAGE: 3D FILE: CHECK_24_1
		PROJECT: D785C	PAGE: 33

def=923=39Bh=11.1001.1011



XILINX

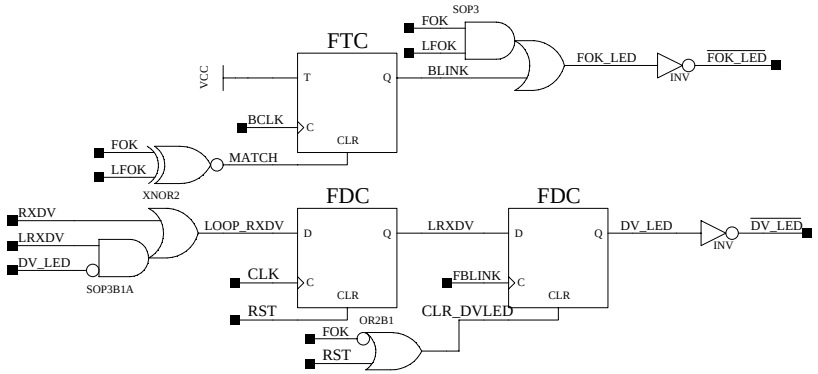
Title:	VIRTEX Family FD12b923 Macro		
Comments:	12-Bit D Flip-Flop with Preset to 923d and Enable	JRG	
Date:	8th May 2003	Ver:	1
Sheet Size: B		Rev:	A

FOK LED

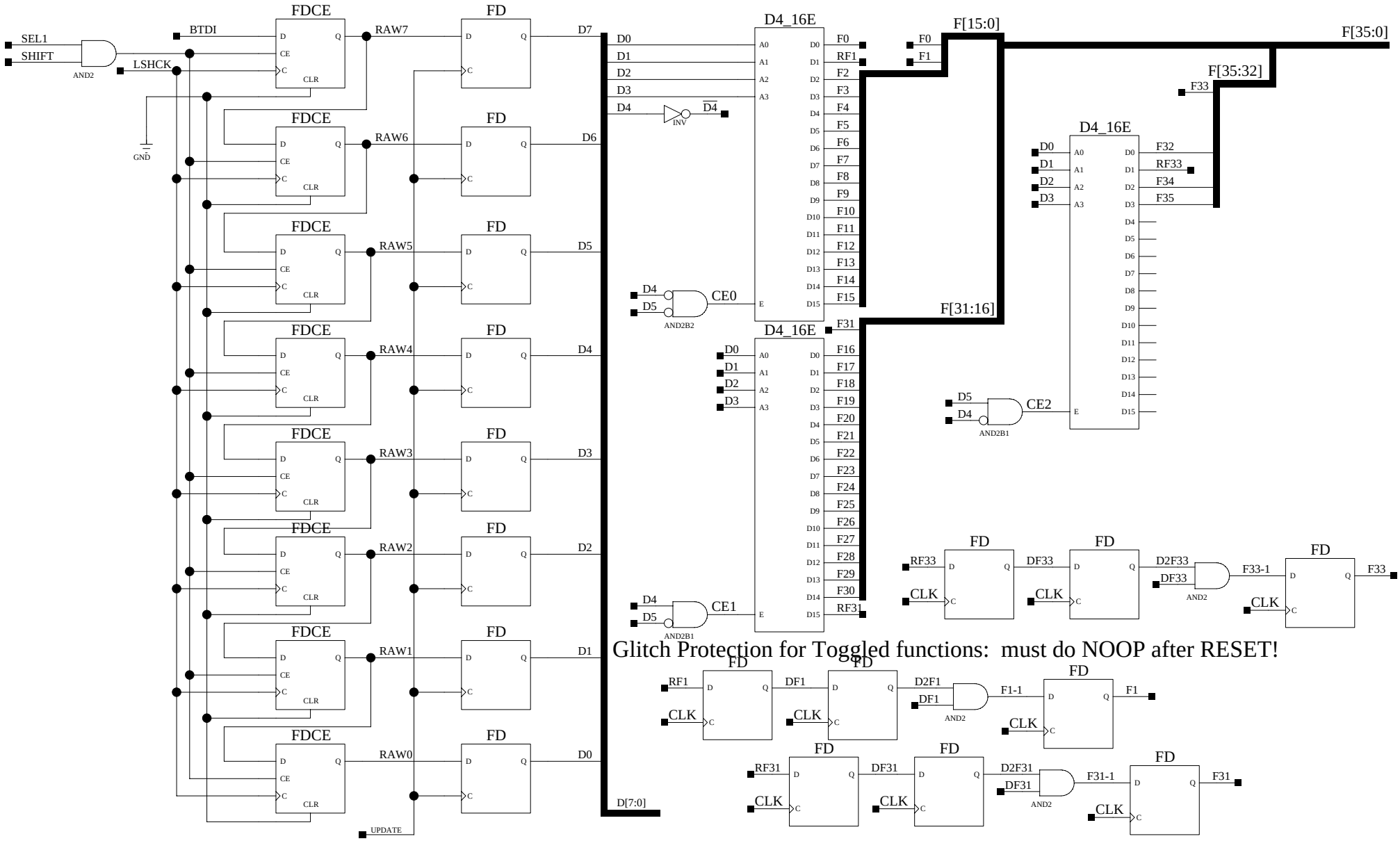
--LIT == Link is alive and well
--BLINK == Link not ready
--OFF == Link not present

DAV LED

--LIT == Active Data Xmit
--OFF == No data to Xmit

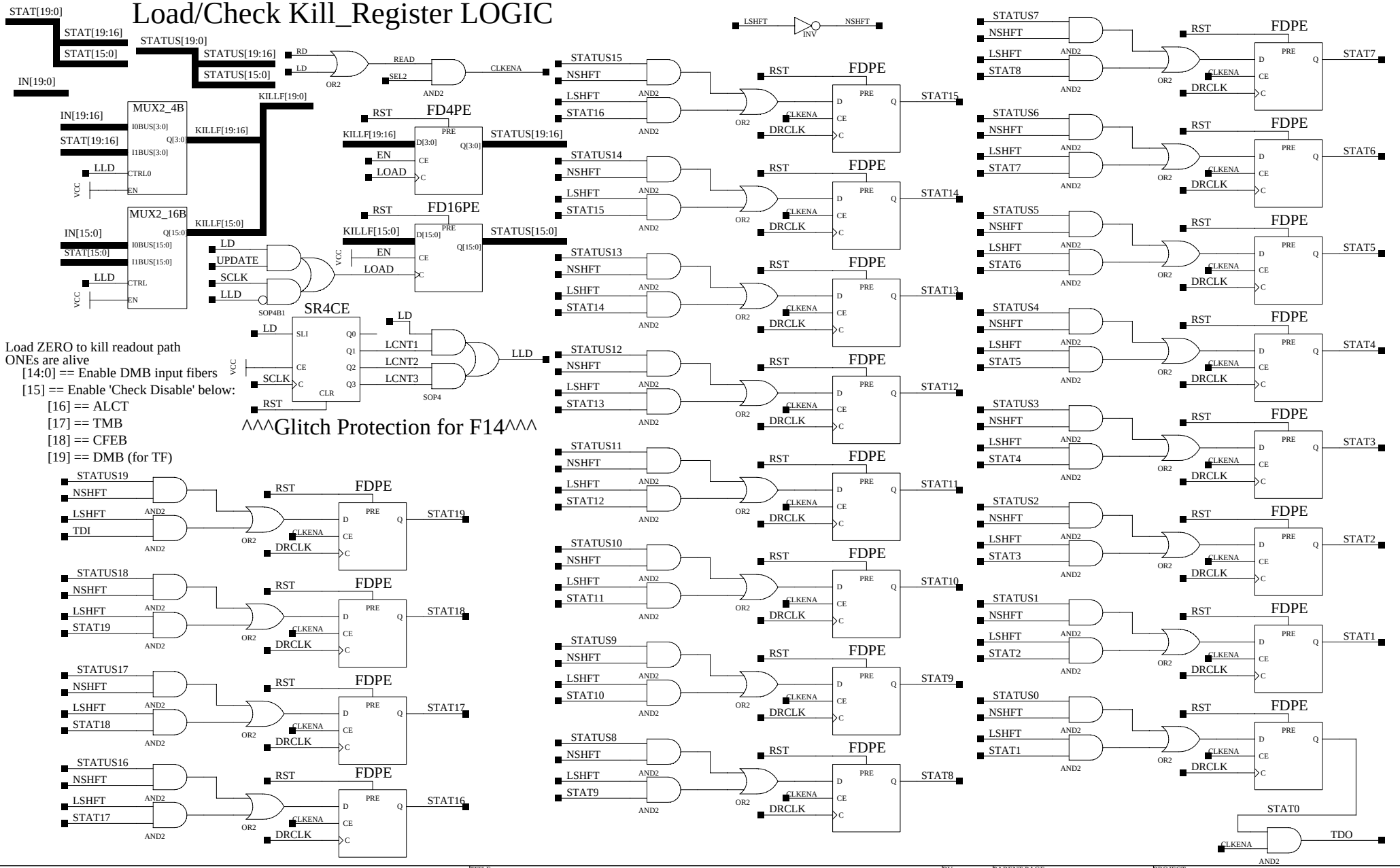


XILINX			JRG
Title:	FIBERLED		
Comments:	Custom LED Slow-Blink Control for Fiber Inputs		
Date:	27th January 2004	Ver:	1
Sheet Size: B		Rev:	A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Instruction Decode DDU Controller CMS CSC ELECTRONICS	BY: JRG PARENT PAGE: 3D DATE: 1-26-2005_12:19	PROJECT: D785C FILE: INSTRGDC . 1 PAGE: 36

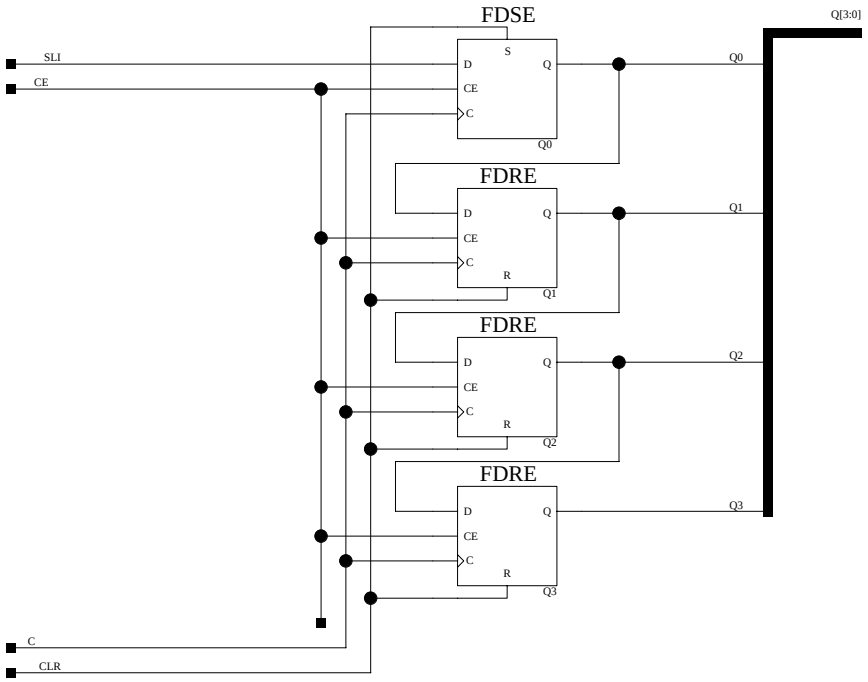
Load/Check Kill_Register LOGIC



Load ZERO to kill readout path
ONEs are alive
- [14:0] == Enable DMB input fibers
- [15] == Enable 'Check Disable' below:
  - [16] == ALCT
  - [17] == TMB
  - [18] == CFEB
  - [19] == DMB (for TF)

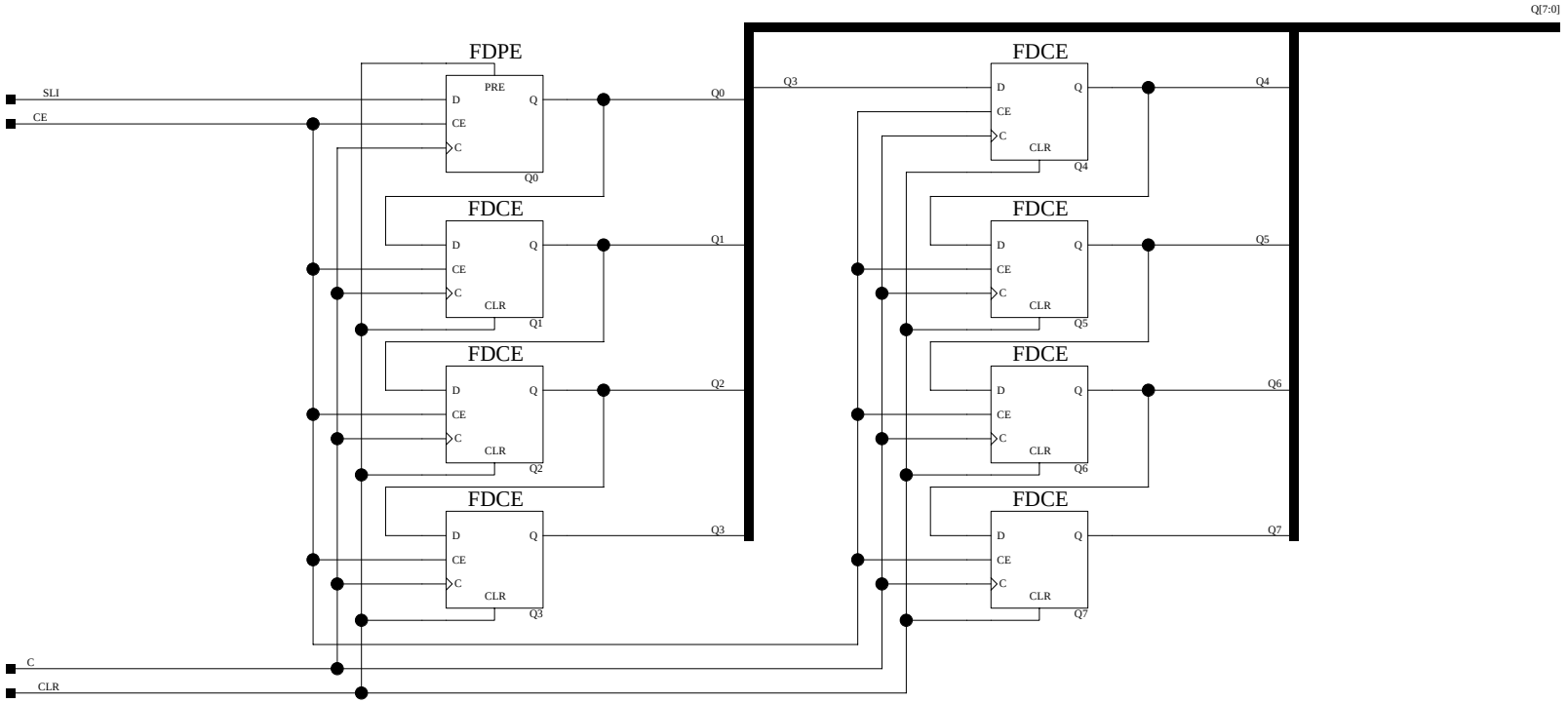
^^^Glitch Protection for F14^^^

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Load/Check Kill_Register Logic DDU Controller CMS CSC Electronics	BY: JRG DATE: 4-12-2007_11:03	PARENT PAGE: 3D FILE: KILL_REG . 1
		PROJECT: D785C	PAGE: 37

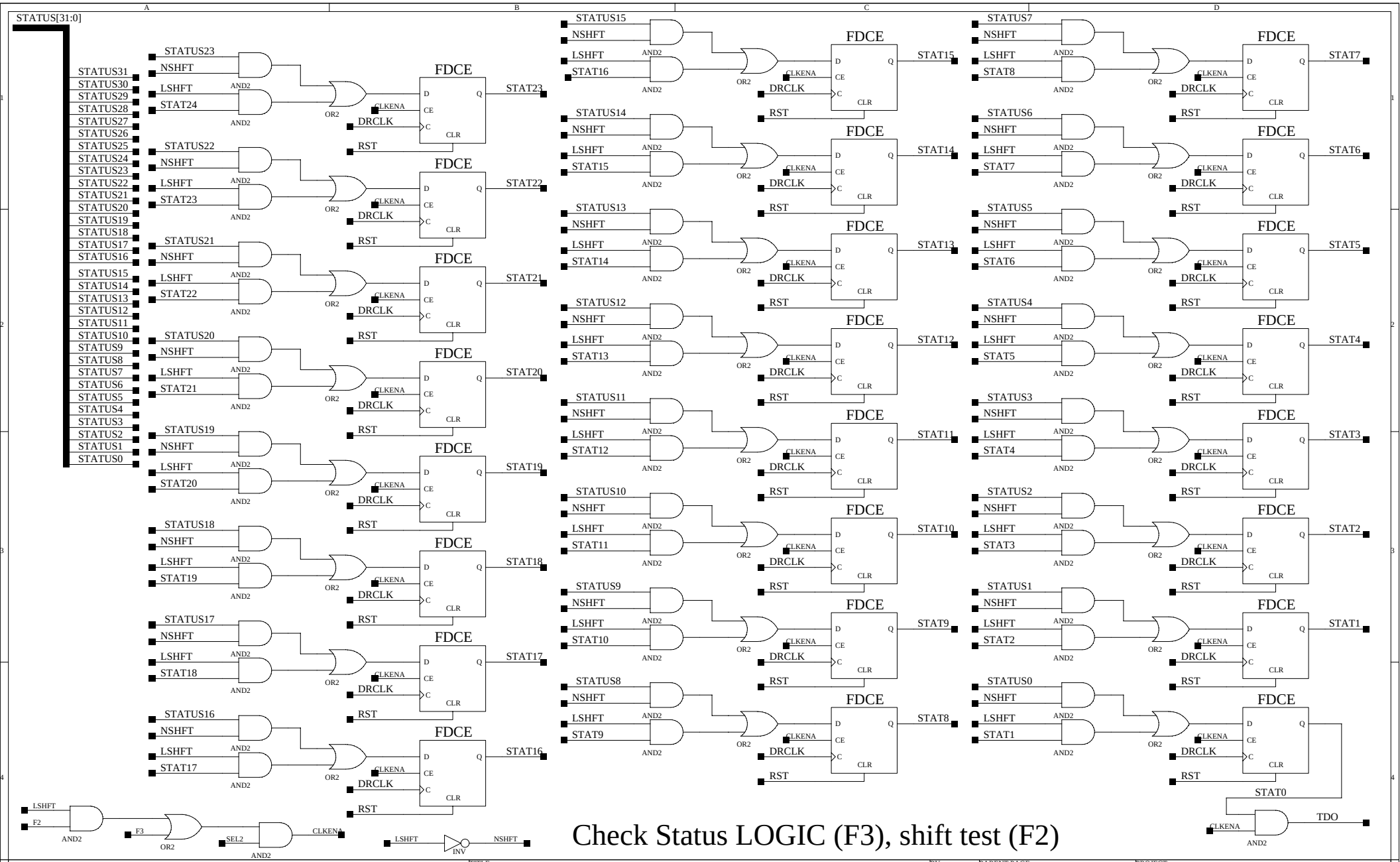


Title:	VIRTEX Family SR4CE Macro		JRG
Comments:	4-bit Serial-In Parallel-Out Shift Register w/ Enable, loads a single "one" on Sync Reset		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A

drawn by KS



Title:	VIRTEX Family SR8CE Macro		JRG
Comments:	8-bit Serial-In Parallel-Out Shift Register w/ Enable, loads a single one on Async Clr		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A

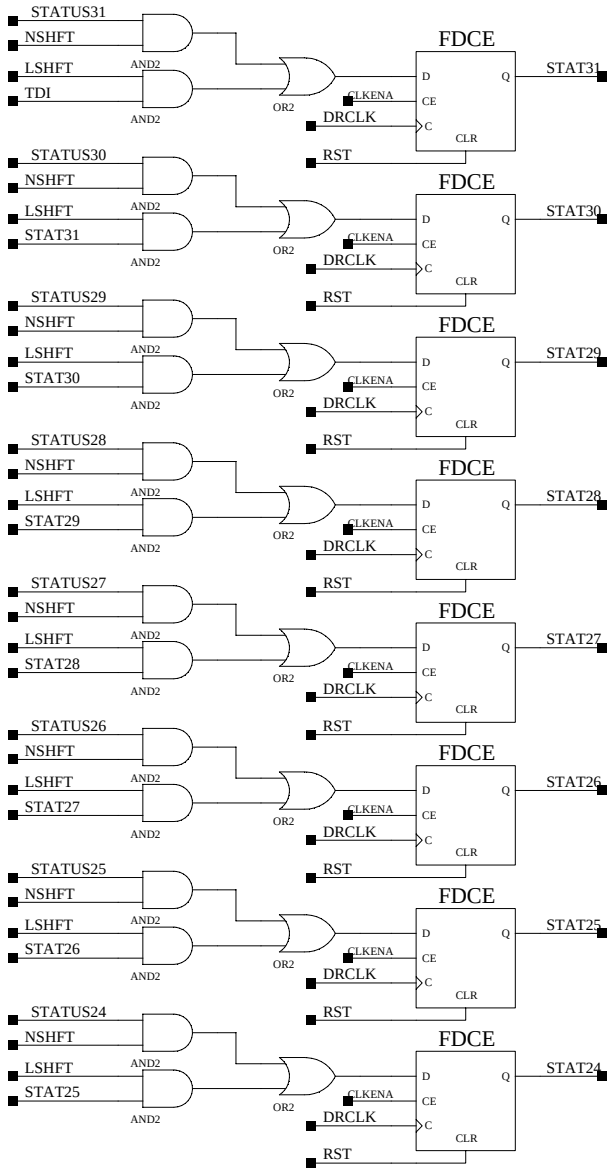


Check Status LOGIC (F3), shift test (F2)

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU JTAG Status Monitor
DDU Controller
CMS CSC Electronics

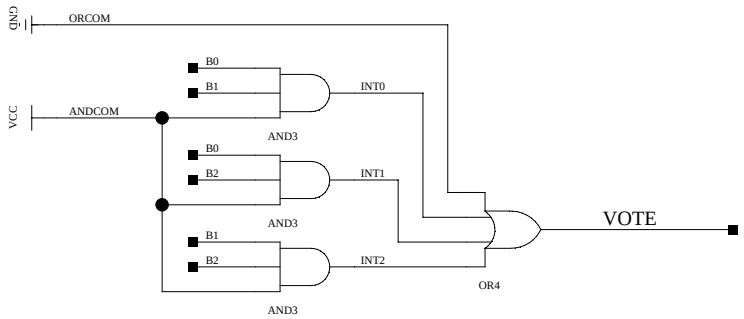
BY	PARENT PAGE	PROJECT
JRG	3D	D785C
DATE	FILE	PAGE
1-26-2005_12:27	STAT_MON_1	40



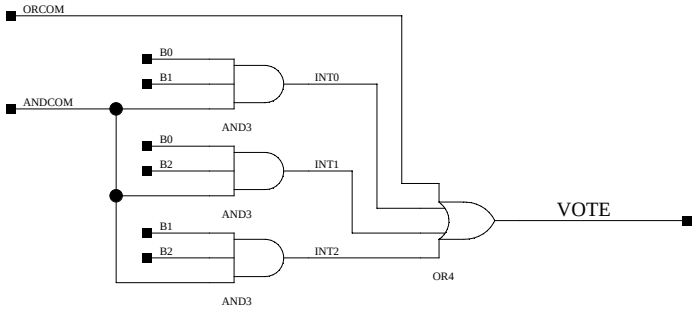
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU JTAG Status Monitor
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	3D	D785C
DATE	FILE	PAGE
1-26-2005_12:27	STAT_MON_2	40A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Vote 2 out of 3 DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 12C	PROJECT: D785C
		DATE: 1-26-2005_12:28	FILE: VOTE3 . 1	PAGE: 41



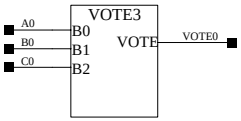
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Vote 2 out of 3, PLUS common AND and OR bits DDU Controller CMS CSC Electronics	BY: JRG DATE: 7-18-2005_16:56	PARENT PAGE: ? FILE: VOTE3P . 1	PROJECT: D785C PAGE: 42

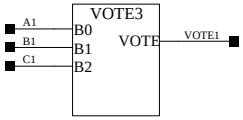
A[15:0]

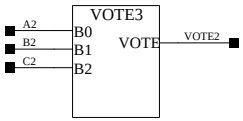
B[15:0]

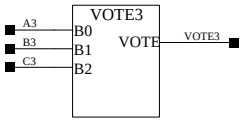
C[15:0]

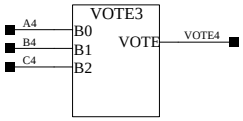
VOTE[15:0]

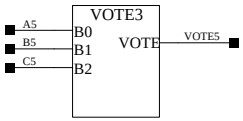


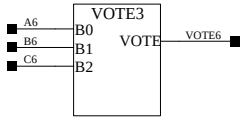


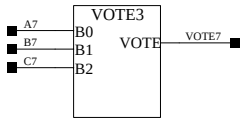


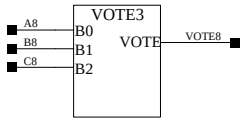


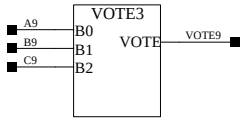


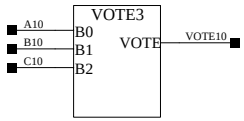


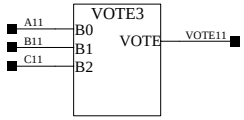


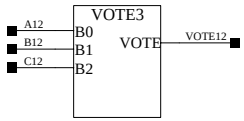


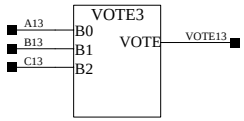


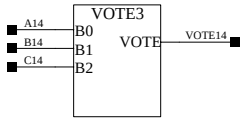


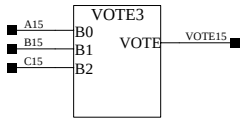












THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Vote 2 out of 3 on a 16-bit bus
DDU Controller
CMS CSC Electronics

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