DDU5CTRL (file 0dductrl)

3-25-2012_17:59

CMS CSC DDU5, Central Control FPGA

CF054A02 Version 54

v45: tune TrigTrailProb, CfebCntErr logic, add CSC RepeatErr logic to LsumErr reg & take it to JTAG F35
r2: remove DMBwarn from FMMwarn logic. r3: add vote3 for DDUCRC r4: remove CRC voting, delay S-Link clock by 3.2ns
v46: tests ck156, SLink clk from DCM --> SLink. r2: shift OWCLK by +3.2ns v47: move ROD pipe reg. into stage2 before DDUCRC v48: GbE skips Empty Events for Global runs
v49: add SYSTEM_RDY diagnostics on LA0 mode 11; r2: add ChBond code for DCC
r7: ChBond fix; v50: hold back Resync until Empty for TFDDU
v51: new ChBond method; r2: ChBnd runs free sync RST
r3: add special Idle sequence for DCC; r4: change special Idle
v52: prevent backpressure response during DoFW phase, may allow 7 words to DCC
r2: replace all EvtCntRst functions with RST; r3: edit RstStop logic, remove ~DoDat; fix DDU_IS_EMPTY startup logic
r4: tune DDU_IS_EMPTY wait for EOE logic
v53: change LinkRdy->DCCwait logic, store both for EOE status register
v54: add DCC Preamble (default) plus ForceIdle logic states
r2: fix WantRen logic, tune DoIdle & OSTAT fields

Set All I/O to 3.3V

PART=XC2VP7-6-FF672

PROM=2*XC18V04-VQ44 (PARALLEL)

DDU5ctrl\DDU5ctrl\ddu5ctrl
C051DD99
C151DD99

DDUCNTRL

PromID: 05026093h
FPGAid: 2124A093h

PROGRAM takes < 55 ms (31ms this FPGA)

1: Mode Bit 0
2: Mode Bit 1
3: Mode Bit 2
4: Mode Bit 3
5: Mode Bit 4; High for GBE debug, Low otherwise
6: GbE test, send counter on GBE link
7: Set L1A Fake mode, Kill TTC L1A/BXR/ECR if SW8 is off
8: FPGA version on LEDs

LED0 on top, pins on away-side from LEDs
RST_1=Asynchronus Reset for FPGA1 and ALL FIFOs

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DDU Format Since DDUctrl v15:

BOEJ typs L1A Number BXN ID FOV K-Status
H1: 0x/5T/NN.NNNN/XXX/I.II/VK

49-bit ~unique constant DMBfull(15)
H2: 0x/8000/0001/8000/HHHH

LiveDMB(15) Ostat DMB-DAV(15) BOEstat DMBcnt
H3: 0x/LLLL/oooo/ZZZZ/GGMY

64-bit unique constant
T-2: 0x/8000/FFFF/8000/8000

DDU EOE Status DMBerr DMBwarn(15)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP

EOE WordCount CRCword EOEstat K-Status
TR: 0x/A/?/WW.WWWW/RRRR/UUMK

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount 8 TS assumed

mojo

DDU5CTRL -- Project History

v1-2: from ddu4ctrl_v28, FIFO Full JTAG Reg is 16-bits
Last w/DDU_FOV=4 --->> v10-12: Add RCLK1, Tune OutUnit GT resets, tune DCC_WAIT modes & add Klll opti
v13-14: Fix LVT/LVA, kill DMB-CFEB-Sync, bring DMB Results to CRCerr; tune DMB checks, GbE Prescale & SLinkWtEn from VME
v15-16: fix DMBwarn, add VME_FakeL1enable; put DMBLIVE[14:0] in HDR3; put DMBwarn/err in TR-1, Tune TRG_Trail_Err resets, FOV
v17-18: tune DMB_Full, RST_InStat, EndTimeRST, PRST, add InRD-C-Code JTAG path (F20), GbE Packets now 7952 byt
v19: Require SLinkWaitEn for CFEB_L1err check; v20: set RCLK0 to FAST24, CkFB to SLOW6--->rev2: SLOV
v21: add C-code-err Begin/End to JTAG F20, set CLK40-0 to FAST16, DMBliveErr & In_Time_Out go to BOE_St
v22: add DMBLIVE reg's on F25/26, CLK40-1 is FAST16, L1A uses OFD_1; rev2: CLK40's use F16-OFDD
Good! rev3: tune PDMBLIVE_EN & RST_STRT logic v23: add KillCFEBchecks & require FKILL15 to EnableCheckDisal
Good! v24: tune DMBlive timing (yellow FMM), bring signals to LEDm10/LA0/
v25: tune L1err & InFerr "DMBliveOK", fix TTMB_Err, tune RstBOE, check CFEB L1A only on 1st sample (not critic
v26: BXorbit=3563 now, add IDMB_FULL flag on ERB. v27: tune CFEB_L1er, 8/16 sample flag, WarnMon & BX offs
v28: add Big debug reg. on F21, Timeout reg. on F28 use LnextFIFO, replace LLLREN w/LFOE for TimeoutRe
make ERA-St/End-TO perm. . v29: fix Mult.L1Err logic, add InSingWarn/InML1Err, tune DDUsyncErr, L1A-fake kills TTC-L
v30: tune Critical Error, InRdWarn, SpyOvfl & LextStop logi
v31: tune CFEB-DAV check (OR DAVs from DMB Hdr1 & Hdr2), add SP/TF compatibility & diagnostic log
v32: change CfebCalDisable default to True, remove DDU_DLL_Err from FMMerr (InRdErr4), modified ERB13 for perm DDU_DLL_
add DDU CSC-Board occupancy monitor-F34? r2: add zeroing logic at RST for Occ.Mon. -r3: fix LRST log
v33: change SourceID=760=2F8h for TF-DDU v34: Inverted CCB_CMD bus & L1A **for TF-DDU ONLY!
v35: Autodetects TF-DDU, now compatible w/wo TF; add SyncHold & CloseL1A logic; r2, removed redunda
RdyIn2 requirement for SEN bits. r3-4, OSyncRst on ~Clk40, tune OFIFO Mon, req. VMEctrv17+ & InCtrlv22r
v36: non-TF DDUs have SrcID==BrdID, NoLiveFibers now readout on L1A. r2: change TF_SIG to FDRE, Reset CheckCRC with NewTFD
v37: diagnostic changes....Tune DMBL1err(notALCTerr), BadCtrl(notMissTrg), LIE(addMissTrg
DMB/TMB/ALCTerr account for MissTrgTrail, DMB-to on Era15, XtraTrgTrails on Erc5+13,DDUfmm 3-bits held Reset until Systemk
v37r2-3: tune CfebL1aErr/SyncErr &DMBcritErr logic, MultL1err logic, InSingWarn=Era10,ValidDMBfull=Erb0,DMBtimeout=Er
v38: DMBcritErr=Erc7, improve Htmb/alct timing,C-codeErr goes to InMxmitReg, InTimeout goes to EndTimeBusyR
r2: make DAQovfl for FF case only, include C-CodeErr w/MultXmitErr, CFEBcrc flags Reset on BOE, C-code-L1er=FIFOb
LDMB_CRCok held at least 4 cycles
r3: add DMB-TO/FIFOfull to TMB/ALCTerr Regs, adjust their time to L2DMBrd; TrgWC only Comp 8 bits, A-T-Switch Req. NoSpwd
r4: fix LWCb8 Reset logic for long ALCT case (still not inc. in WC check thoug
v39: 64bit_err reset on BOE, TrgWC now uses all 9 bits, CloseL1A range now 1usec, BIG L1Afifo w/better Warn/Busy Lo
r2: add hysteresis for L1A_AF/Busy state, tune DAQovfl logic, tune SysRdy/BUSY logic. r3: tune L1pipe/StuckData lo
-r4: tune CRC_Cnt_Err monitor logic; r5: tune SCAovfl Reset & CountSample timin
v40: DMB & Trig.CRCs use MUX to load Zeroes (not Tbufs), change DDUfb rese
-r2: add time constraint to DDUFB reg to eliminate DDUCRC logic lag. r3: tune BuffOvfl & EthLim log

To Do:

- COMPARE BXN (DMB/TMB too)
- Watch for TRG buff overflows
- Determine correct values to store in Flash Mem
  ---> BX offset, KillCh's, FIFO thresh, Board ID
- Test DCC/SlinkWait feedback function & thresh's
  ---> Make DMB stop too
- Verify that CFEB-CRC is fixed for B-code case
- No logic for BUS1, DCC SBDATA & TDxxx, 4 LSF, 4 LRL
- Make Verilog module to get Fiber/DMB_RD in one CLK?
- Multiple TRG_L1err ought to request a Sync Reset?
  * Same for consecutive events with a TRG_L1err?

Check Phase of CMD to CLK40

- * pg. 2G & 3I
- CFEB-DMB sync check pg. 12C
- CFEB-L1A check disabled, pg. 12D: not! Found a fix...
- options for Monitoring on pg. 3H, 12E?
- Does CFEB-Check-Disable cause TF/SP mimic?

v41: SCA_Ovfl separated from DMB_Err & SomethingBad. r2: tune KillFiber glitc
v42: change to proposed format for ALCT; r2: FOV=6, on TFsig kill ALCT/TMBerr, correct SBXN f
3564-4096 difference in BX<40 case (from CloseL1A logic) r3: change to new ALCT/TMB data forma
r4: fix TRG bugs in stage2 r5: reduce RST logic delays, may have caused TrgTrail detect problen
added bit usage notes in FIFOCTRL, 27nov2007 v43: tune CMD Strobe timing; r2, adjust TMB/ALCT Fful b
r3: fixed bug in TrgL1err reporting. v44: change TF-DDU definition (0xc0 in Flash-Page7

TST	Clock	BUFGMUX	
0P	drck1	5P *4P	-TR
2P	2clk	5S *1S	
3S	clk	7S *7S	
0S	clk625	2S- *2S	
7P	ck125	1P *0S	-BL
5P	clk40	0S *3P	
4S-	clk156	4S- *4S	
1S	drck2	3P *5S	
6S-	sclk	6S- *6S	

* denotes LOCed position

New Ideas:

Store & check DMB source ID's from each fiber?
Feed SLINK status into FMM logic (for UF).
Set DMB CRC OK flag for DDU Empty Events? no...
In case of StuckData send PRST? How to distinguish SEU? Later event still gets LostHdr or Timeout, could self-correct. Add "PRSTed" VME register to track occurrence.
In case of L1Amismatch, let it run and see if it is better a few~10 evts later. Possible to self-correct as above...? Can only work if DMB really lost event data.

Default Startup Order:

Release DLL (no wait)
4) DONE
5) En. Outputs
6) Release WE

CSC_L1Err<--Bring to VME-JTAG Reg?

DDU Format Since DDUctrl v15:

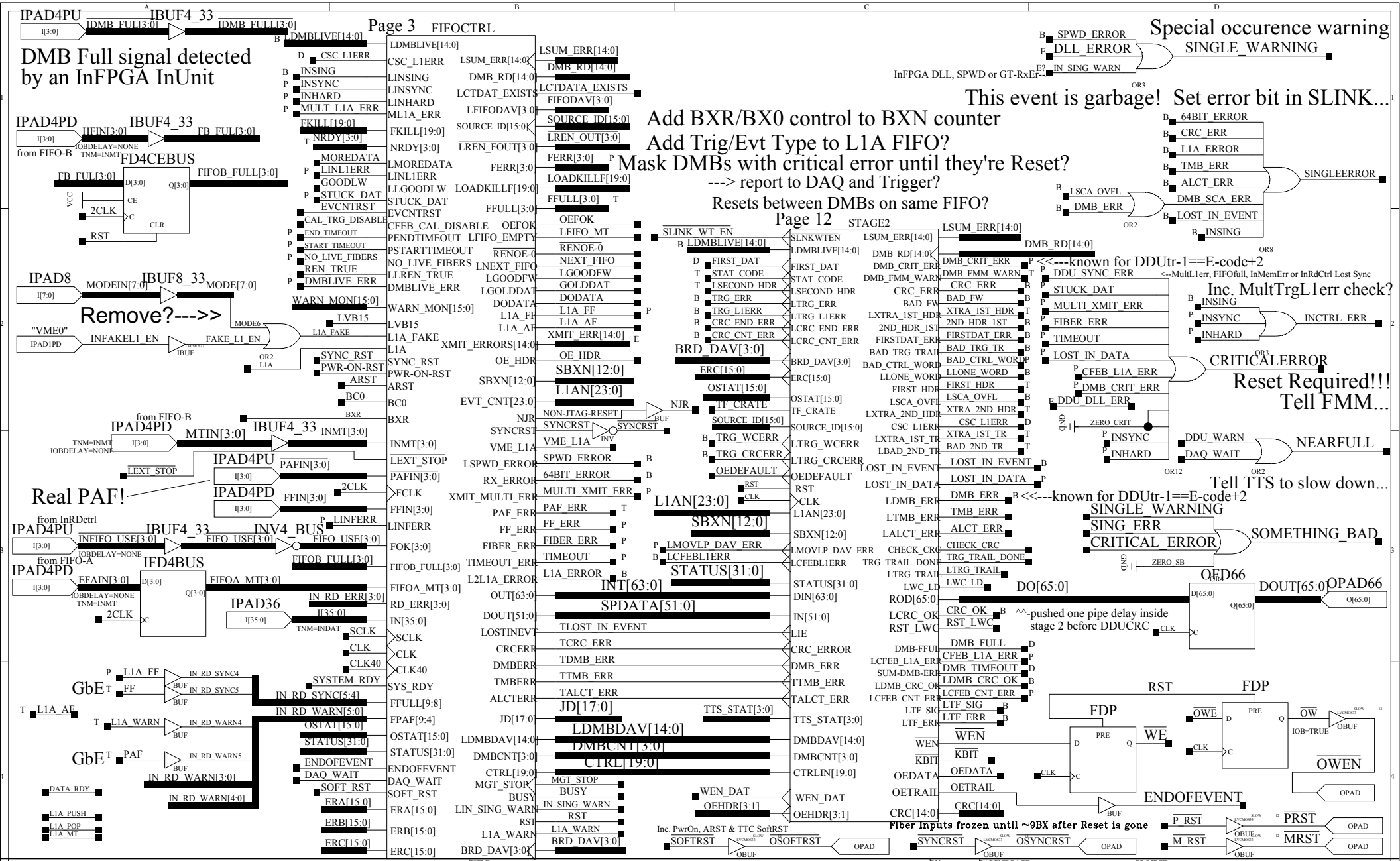
H1: 0x/5T/NN.NNNN/XXX/I.II/VK (BOEJ_type, L1A_Number, BXN, JD, FOV, K-Status)
H2: 0x/8000/0001/8000/HHHH (49-bit_unique_constant, DMBfull(15))
H3: 0x/LLLL/oooo/ZZZZ/GGMY (LiveDMB(15), Ostat, DMB-DAV(15), BOEstat, DMBcnt)

T-2: 0x/8000/FFFF/8000/8000 (64-bit unique constant)
T-1: 0x/SSSS.SSSS/QQQQ/PPPP (DDU EOE Status, DMBerr, DMBwarn(15))
TR: 0x/A/?/WW.WWWW/RRRR/UUMK (EOE, WordCount, CRCword, EOEstat, K-Status)

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070; 240560 Bytes
^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount _8 TS assumed_

DDU WC, 3 DMB with 1 CFEB (nCFEB=3): 26Ah = 618 dec, 4944 Bytes
DDU WC, 4 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes

DDU WC, 11 DMB with 1 CFEB (nCFEB=11): 8CAh = 2250 dec, 18000 Bytes
DDU WC, 12 DMB with 1 CFEB (nCFEB=12): 996h = 2454 dec, 19632 Bytes
DDU WC, 15 DMB with 1 CFEB (nCFEB=15): BFAh = 3066 dec, 24528 Bytes


Page 3
FIFOCTRL
DMB Full signal detected by an InFPGA InUnit
Special occurence warning
SINGLE_WARNING
This event is garbage! Set error bit in SLINK...
Add BXR/BX0 control to BXN counter
Add Trig/Evt Type to L1A FIFO?
Mask DMBs with critical error until they're Reset?
---> report to DAQ and Trigger?
Resets between DMBs on same FIFO?
Page 12
STAGE2
Remove?--->>
Real PAF!
Tell TTS to slow down...
Inc. MultTrgL1err check?
Reset Required!!!
Tell FMM...
Fiber Inputs frozen until ~9BX after Reset is gone
^^-pushed one pipe delay inside stage 2 before DDUCRC
<<---known for DDUtr-1==E-code+2
<--MultL1err, FIFOfull, InMemErr or InRdCtrl Lost Sync
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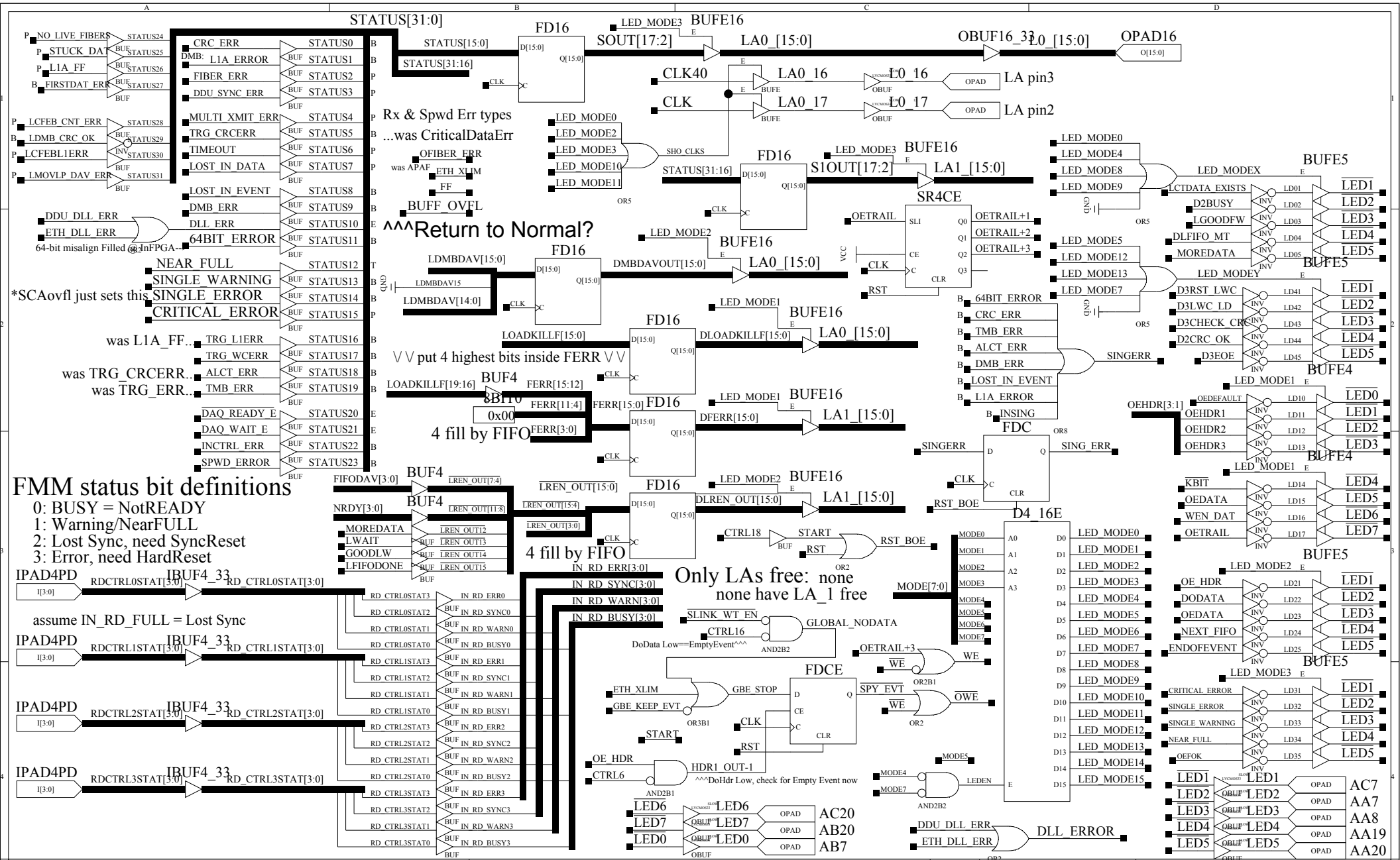
3-22-2012_15:35
DDUCNTRL . 1
2



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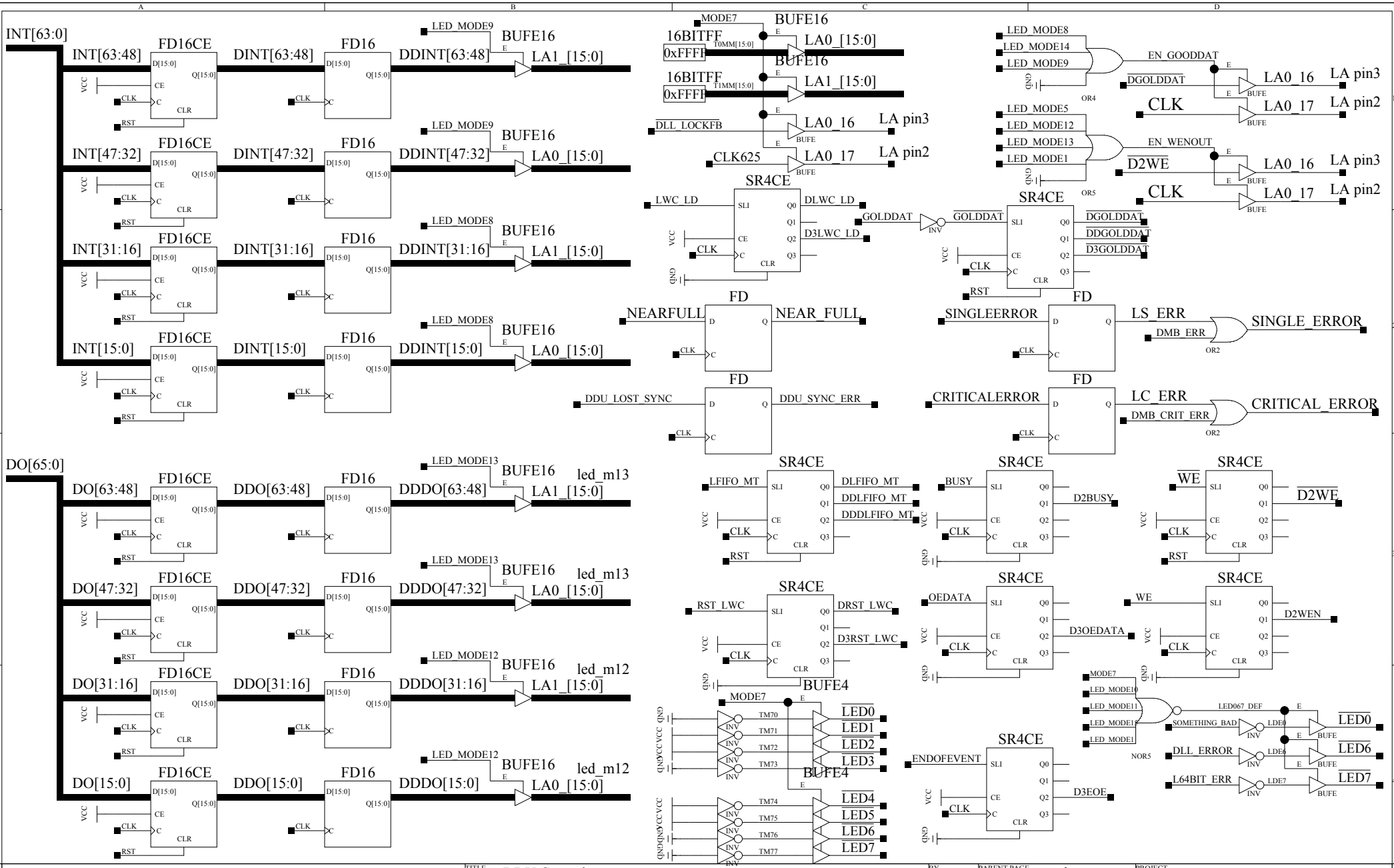
		DATE: 3-21-2012_19:11	FILE: DDUCNTRL . 2	PAGE: 2A



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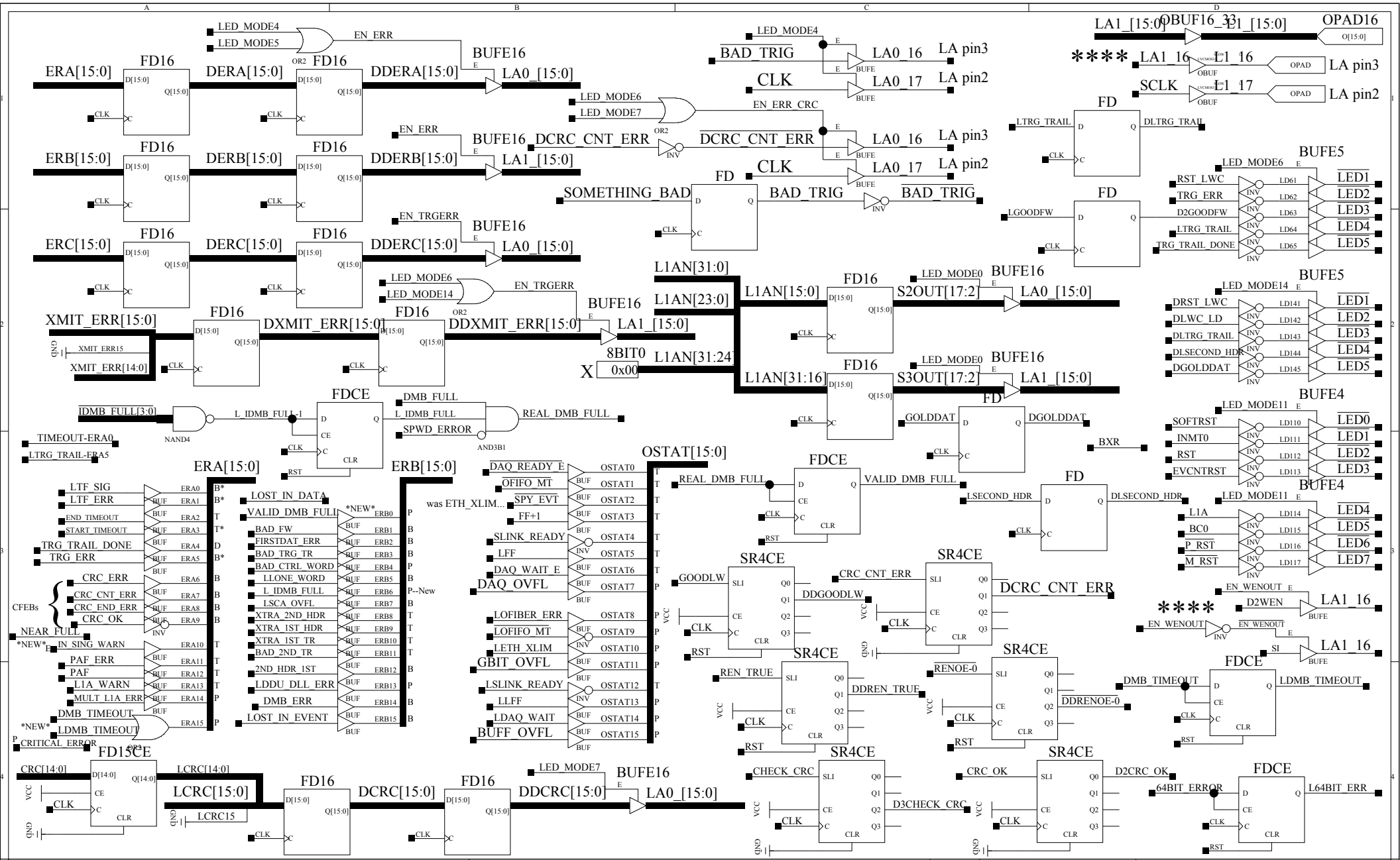
		DATE: 3-21-2012_19:11		FILE: DDUCNTRL . 3	PAGE: 2B



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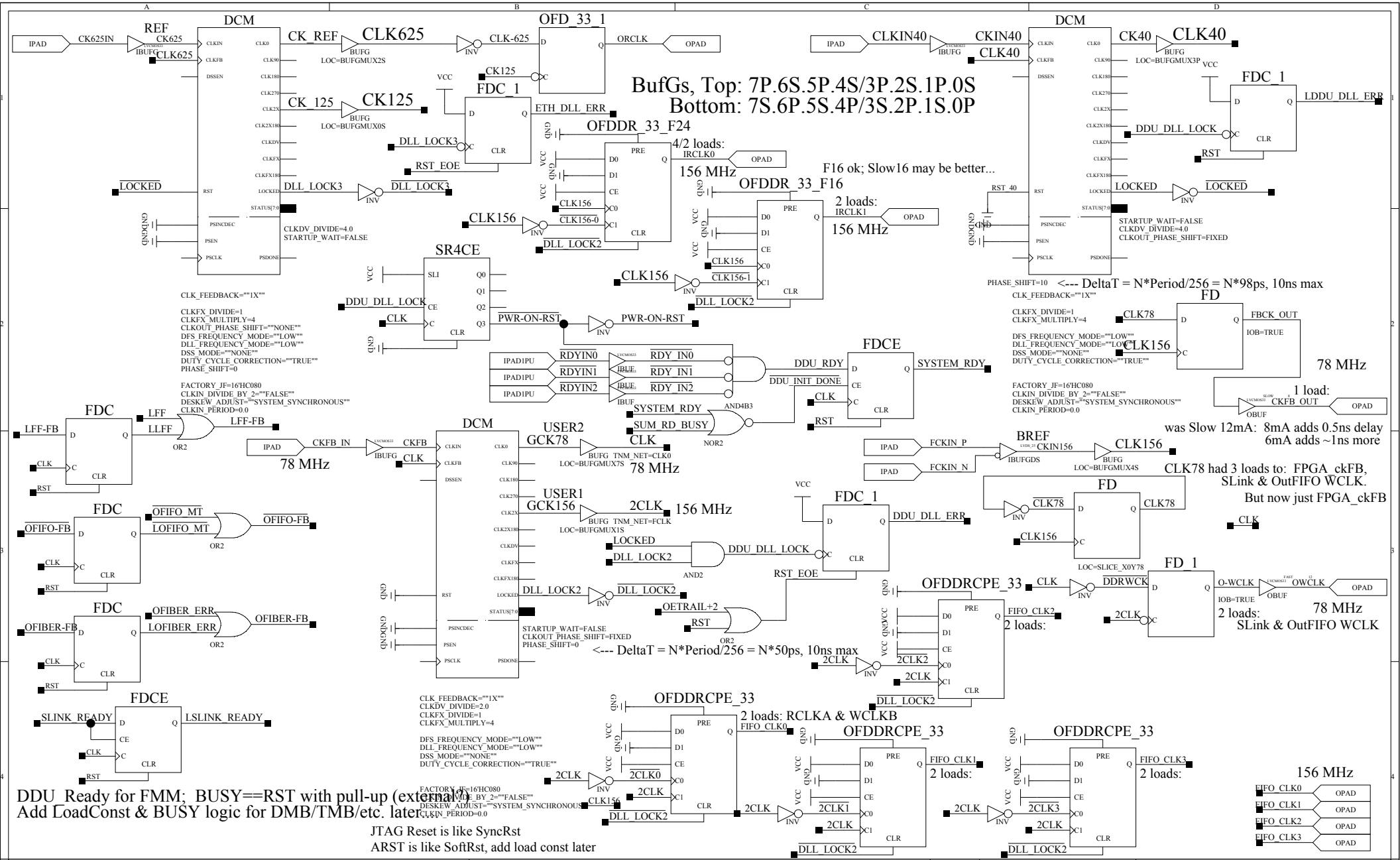
		DATE: 3-25-2012_17:55	FILE: DDUCNTRL . 4	PAGE: 2C



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SLINK_WT_EN enables DCC/SLINK_WAIT and CFEB_DAVLCT checking from DMB
DCC FULL is no use; better for DCC to send "FPGA ProgramDone/Ready" signal, then DDU Stops on DCC ~PAF signal.
Was like SLINK, now is DCC ~FF or ~PAF?
S-Link Ready
S-Link ~Full
True for 1 clock^^^
Page 18
Page 16
FED Kit Reset, hold HIGH
Loadless Rx Data ...monitor Rx Status?
N.L.
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DDU Control
DDU Controller Logic
CMS CSC Electronics
JRG
1
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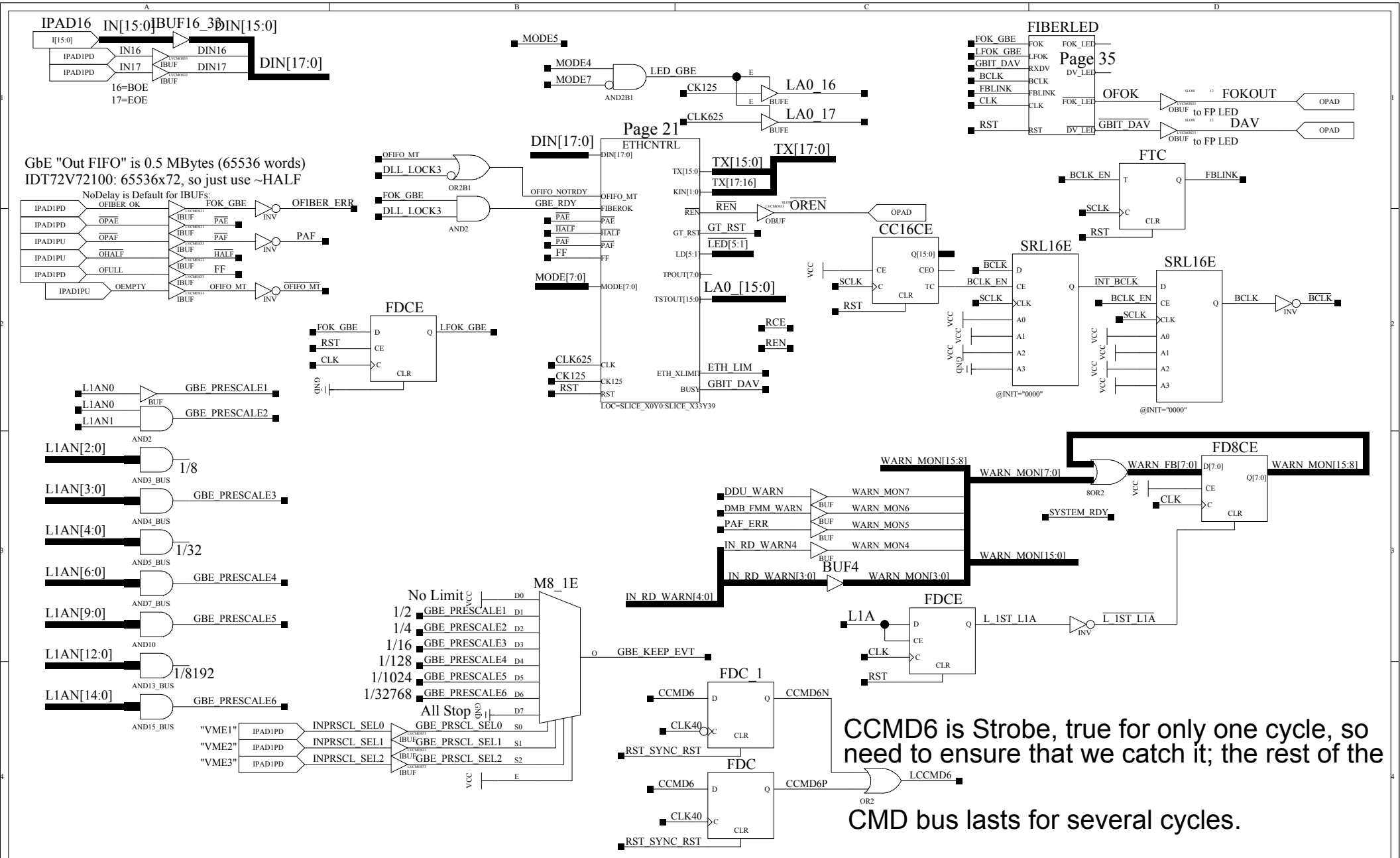
3-25-2012_17:14
DDUCNTRL . 6
2E



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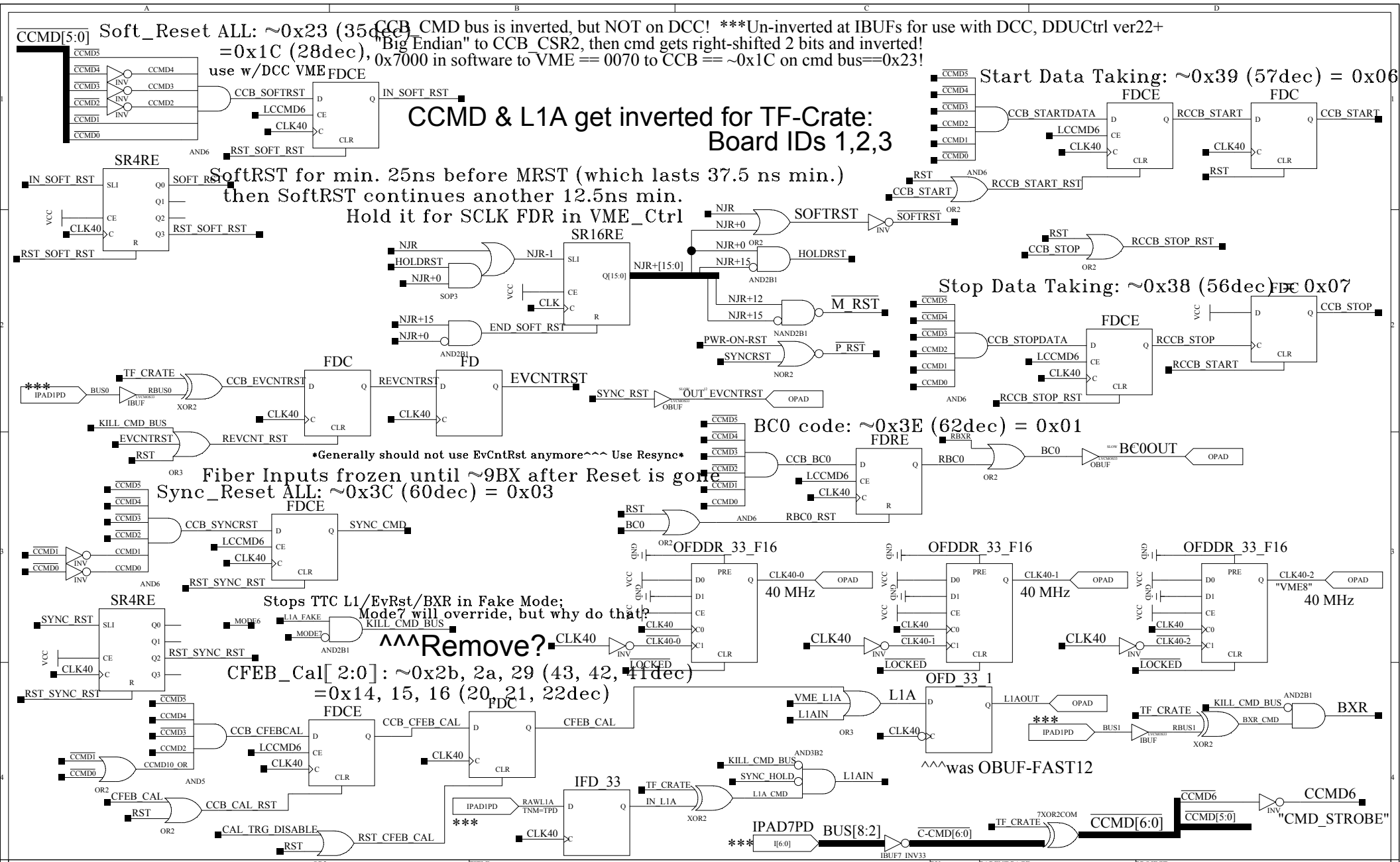
		DATE: 3-21-2012_19:11		FILE: DDUCNTRL . 7	PAGE: 2F


CCMD[5:0]
Soft_Reset ALL: ~0x23 (35dec) =0x1C (28dec), use w/DCC VME
CCB_CMD bus is inverted, but NOT on DCC! ***Un-inverted at IBUFs for use with DCC, DDUCtrl ver22+
"Big Endian" to CCB_CSR2, then cmd gets right-shifted 2 bits and inverted!
0x7000 in software to VME == 0070 to CCB == ~0x1C on cmd bus==0x23!
CCMD & L1A get inverted for TF-Crate:
Board IDs 1,2,3
Start Data Taking: ~0x39 (57dec) = 0x06
SoftRST for min. 25ns before MRST (which lasts 37.5 ns min.)
then SoftRST continues another 12.5ns min.
Hold it for SCLK FDR in VME_Ctrl
Stop Data Taking: ~0x38 (56dec) = 0x07
BC0 code: ~0x3E (62dec) = 0x01
Generally should not use EvCntRst anymore^^^ Use Resync
Fiber Inputs frozen until ~9BX after Reset is gone
Sync_Reset ALL: ~0x3C (60dec) = 0x03
Stops TTC L1/EvRst/BXR in Fake Mode;
Mode7 will override, but why do that?
^^^Remove?
CFEB_Cal[2:0]: ~0x2b, 2a, 29 (43, 42, 41dec)
=0x14, 15, 16 (20, 21, 22dec)
^^^was OBUF-FAST12
FDCE
FDC
FD
SR4RE
SR16RE
OFDDR_33_F16
OFD_33_1
IFD_33
IBUF7_INV33
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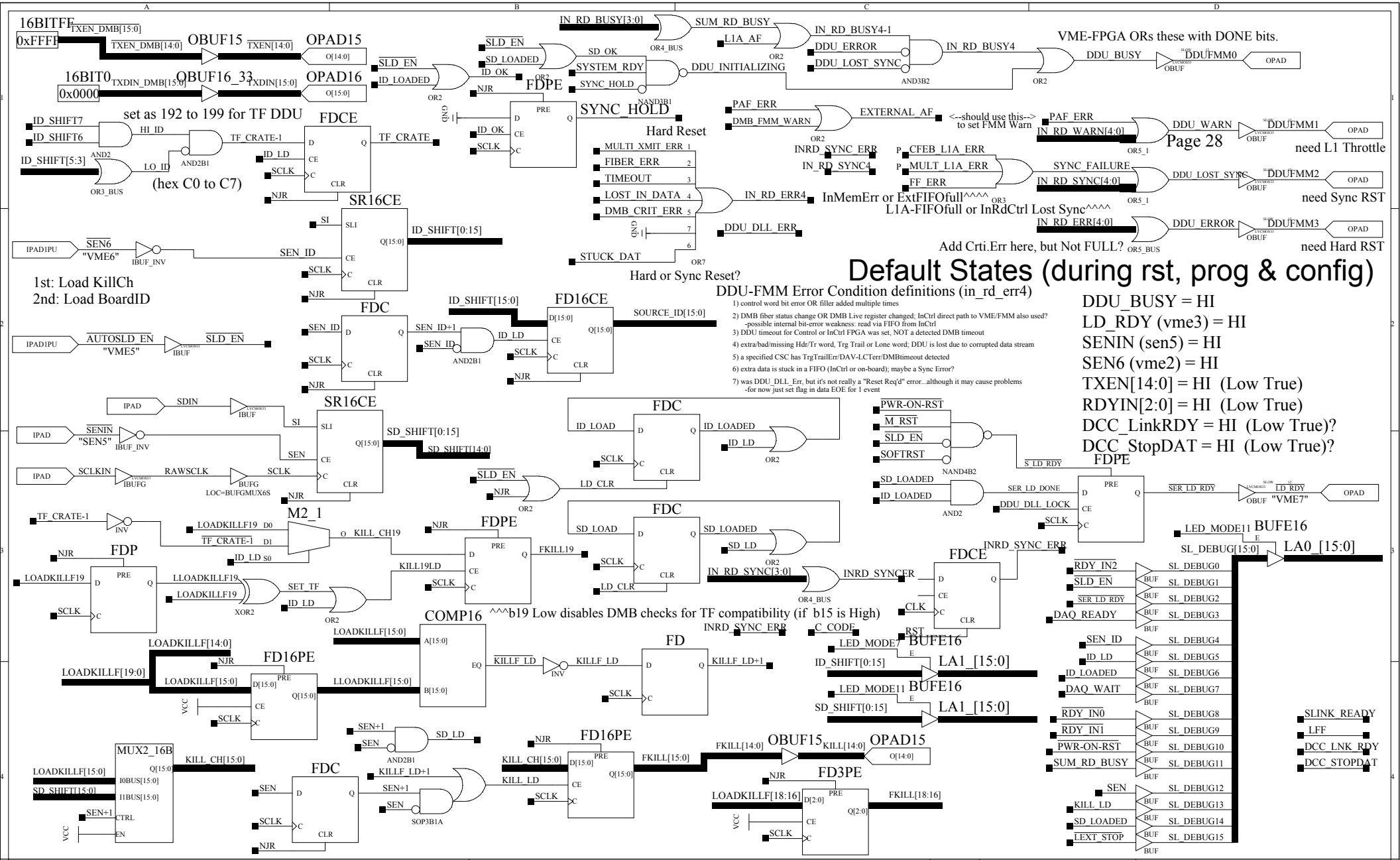
TITLE
DDU CCB Command Decode
DDU Controller Logic
CMS CSC Electronics
BY JRG
PARENT PAGE 1
PROJECT D785C
DATE 3-21-2012_19:11
FILE DDUCNTRL . 8
PAGE 2G



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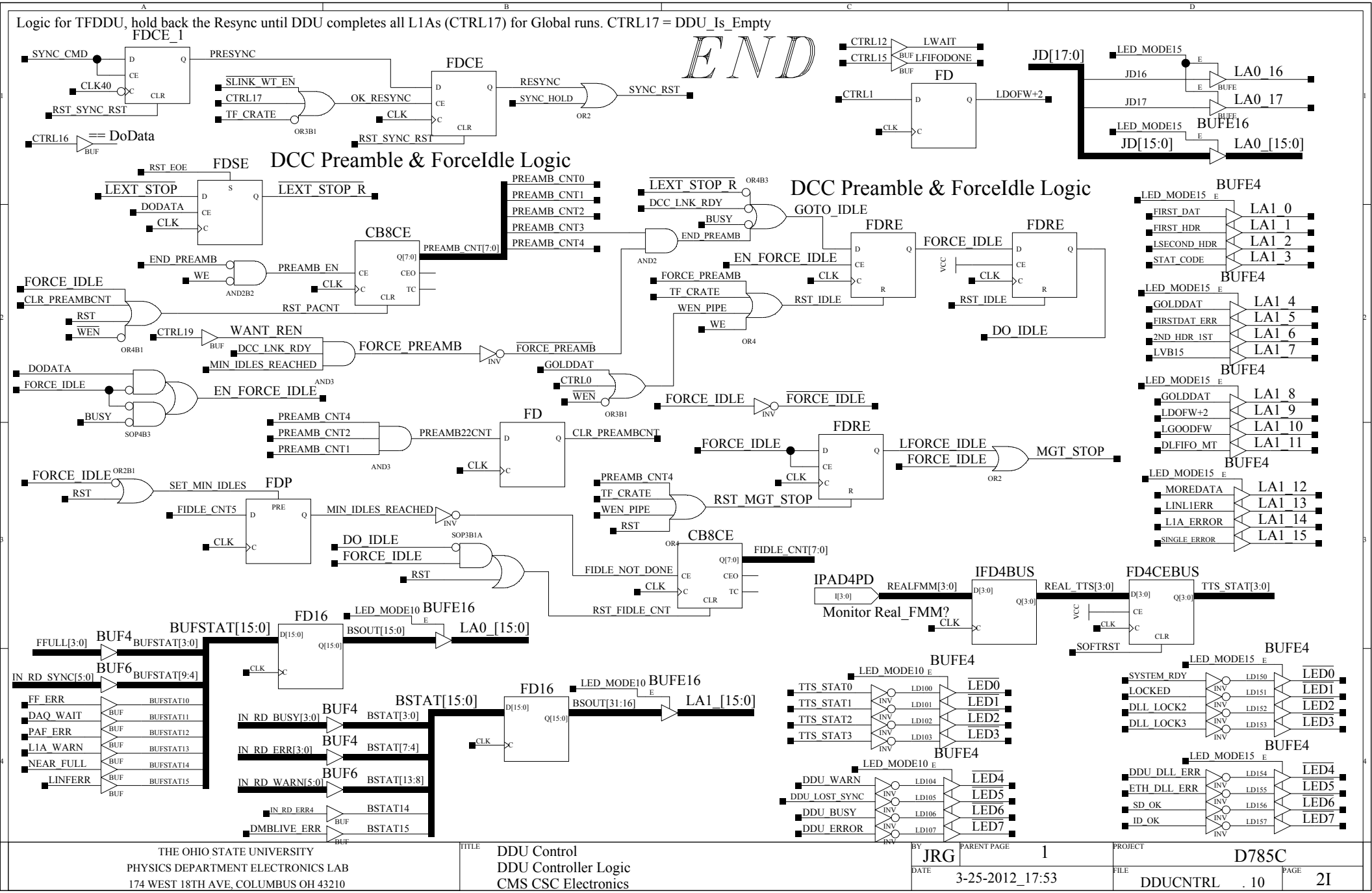
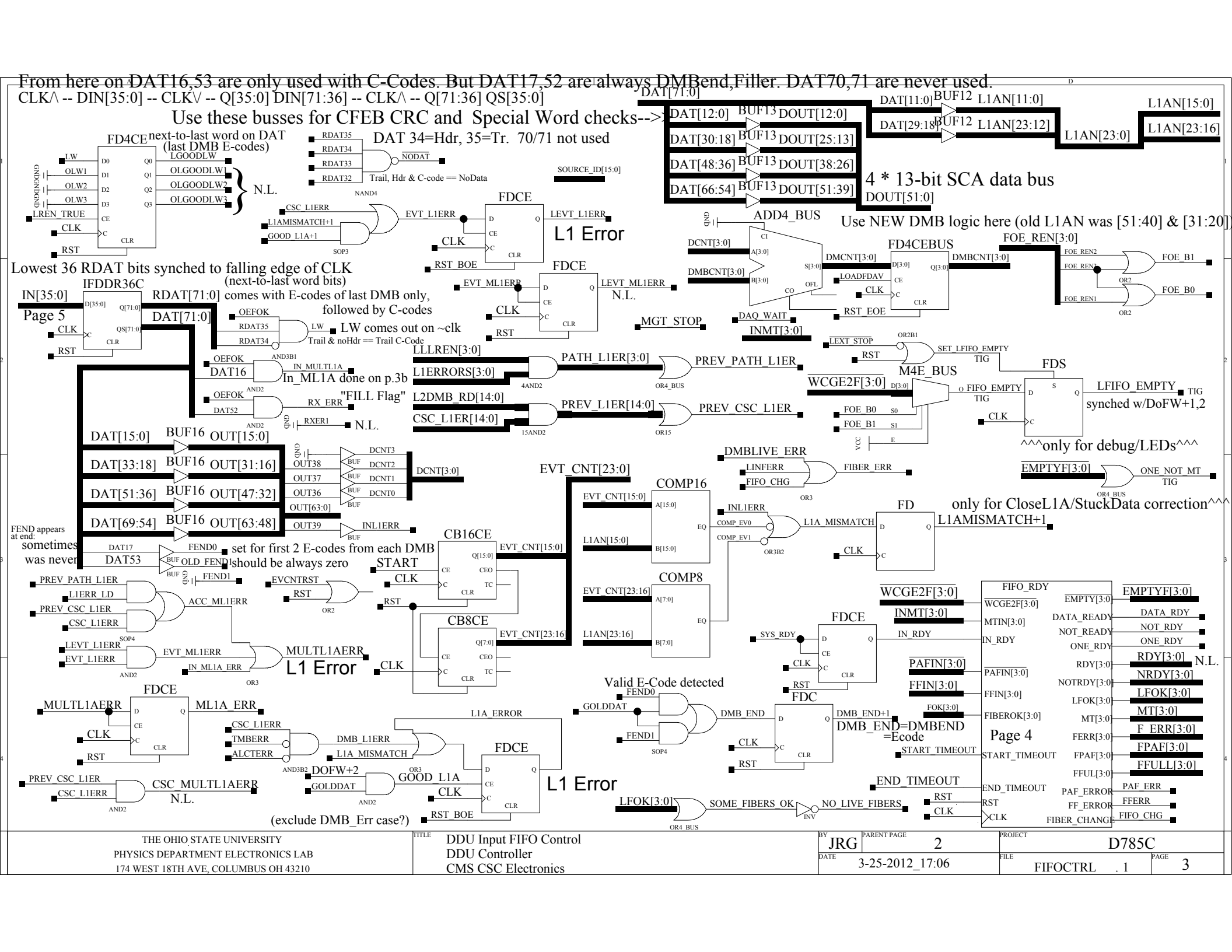
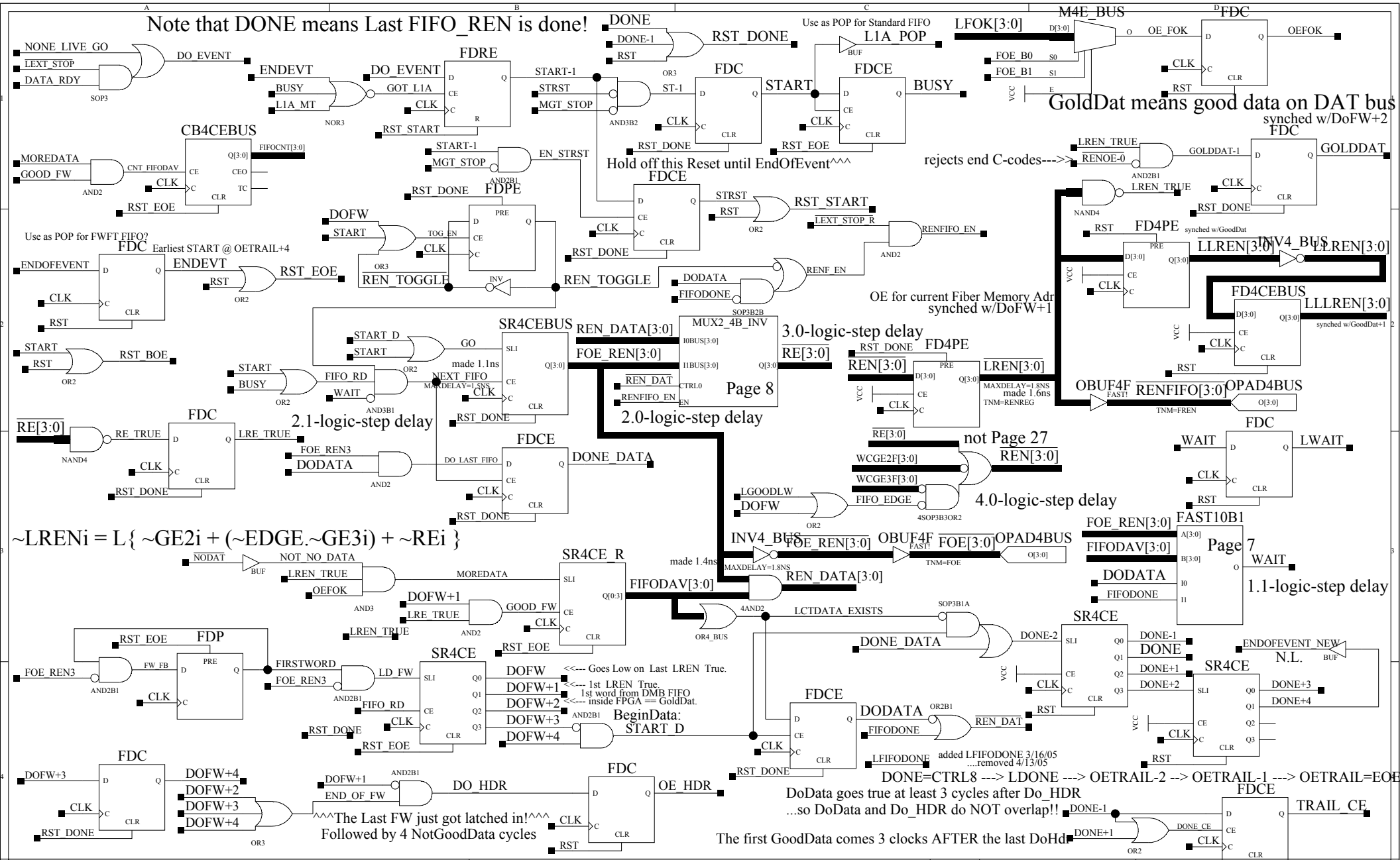
		DATE 3-21-2012_19:11		FILE DDUCNTRL . 9	PAGE 2H

Logic for TFDDU, hold back the Resync until DDU completes all L1As (CTRL17) for Global runs. CTRL17 = DDU_Is_Empty

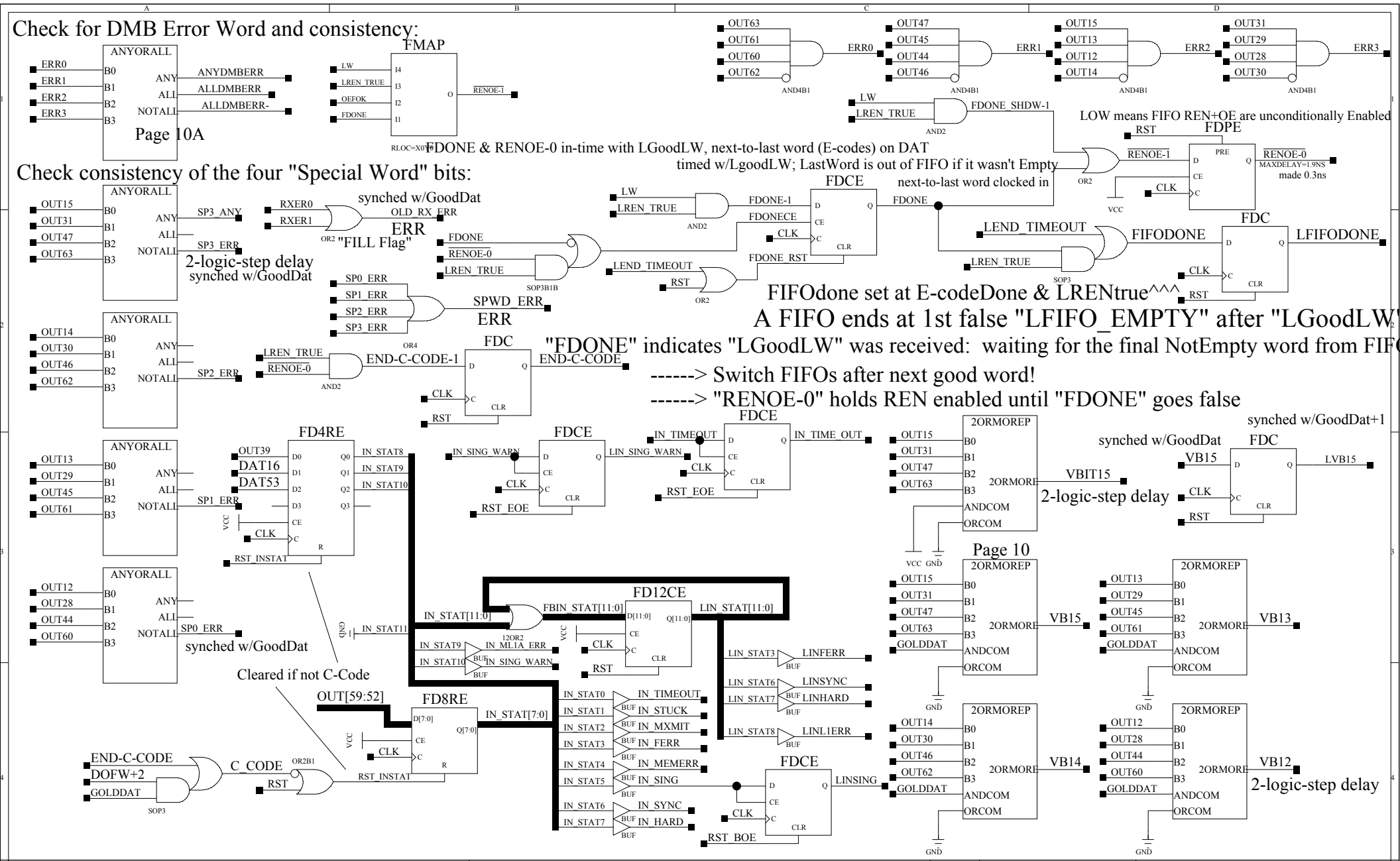


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Control DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 3-25-2012_17:53	PARENT PAGE: 1 FILE: DDUCNTRL . 10
		PROJECT: D785C	PAGE: 2I


From here on DAT16,53 are only used with C-Codes. But DAT17,52 are always DMBend,Filler. DAT70,71 are never used.
CLK/\ -- DIN[35:0] -- CLK\/ -- Q[35:0] DIN[71:36] -- CLK/\ -- Q[71:36] QS[35:0]
Use these busses for CFEB CRC and Special Word checks-->
DAT[71:0]
DAT[12:0] BUF13 DOUT[12:0]
DAT[30:18] BUF13 DOUT[25:13]
DAT[48:36] BUF13 DOUT[38:26]
DAT[66:54] BUF13 DOUT[51:39]
DOUT[51:0]
4 * 13-bit SCA data bus
DAT[11:0] BUF12 L1AN[11:0]
DAT[29:18] BUF12 L1AN[23:12]
L1AN[23:0]
L1AN[15:0]
L1AN[23:16]
FD4CE
next-to-last word on DAT
(last DMB E-codes)
LGOODLW
OLGOODLW1
OLGOODLW2
OLGOODLW3
N.L.
LREN_TRUE
RDAT35
RDAT34
RDAT33
RDAT32
NODAT
Trail, Hdr & C-code == NoData
NAND4
DAT 34=Hdr, 35=Tr. 70/71 not used
SOURCE_ID[15:0]
FDCE
CSC_L1ERR
L1AMISMATCH+1
GOOD_L1A+1
EVT_L1ERR
LEVT_L1ERR
L1 Error
SOP3
RST_BOE
ADD4_BUS
Use NEW DMB logic here (old L1AN was [51:40] & [31:20])
DCNT[3:0]
DMBCNT[3:0]
DMCNT[3:0]
FD4CEBUS
LOADFDAV
RST_EOE
DAQ_WAIT
FOE_REN[3:0]
FOE_REN2
FOE_REN1
FOE_B1
FOE_B0
OR2
Lowest 36 RDAT bits synched to falling edge of CLK
IFDDR36C
IN[35:0]
Page 5
RDAT[71:0]
(next-to-last word bits)
comes with E-codes of last DMB only,
followed by C-codes
DAT[71:0]
OEFOK
LW comes out on ~clk
Trail & noHdr == Trail C-Code
FDCE
EVT_ML1ERR
LEVT_ML1ERR
N.L.
MGT_STOP
INMT[3:0]
LLREN[3:0]
L1ERRORS[3:0]
PATH_L1ER[3:0]
PREV_PATH_L1ER
4AND2
OR4_BUS
LEXT_STOP
OR2B1
SET_LFIFO_EMPTY
TIG
FDS
M4E_BUS
WCGE2F[3:0]
FIFO_EMPTY
LFIFO_EMPTY
synched w/DoFW+1,2
^^^only for debug/LEDs^^^
DAT16
AND3B1
IN_MULTL1A
In_ML1A done on p.3b
DAT52
AND2
RX_ERR
"FILL Flag"
RXER1
L2DMB_RD[14:0]
CSC_L1ER[14:0]
PREV_L1ER[14:0]
PREV_CSC_L1ER
15AND2
OR15
DAT[15:0] BUF16 OUT[15:0]
DAT[33:18] BUF16 OUT[31:16]
DAT[51:36] BUF16 OUT[47:32]
DAT[69:54] BUF16 OUT[63:48]
OUT[63:0]
DCNT3
DCNT2
DCNT1
DCNT0
DCNT[3:0]
OUT38
OUT37
OUT36
OUT39
INL1ERR
DMBLIVE_ERR
LINFERR
FIFO_CHG
FIBER_ERR
OR3
EMPTYF[3:0]
ONE_NOT_MT
OR4_BUS
only for CloseL1A/StuckData correction^^^
FEND appears
at end:
sometimes
was never
DAT17
DAT53
FEND0
FEND1
OLD_FEND!
set for first 2 E-codes from each DMB
should be always zero
EVT_CNT[23:0]
COMP16
EVT_CNT[15:0]
L1AN[15:0]
COMP8
EVT_CNT[23:16]
L1AN[23:16]
INL1ERR
COMP_EV0
COMP_EV1
OR3B2
L1A_MISMATCH
FD
L1AMISMATCH+1
CB16CE
CB8CE
START
EVCNTRST
OR2
PREV_PATH_L1ER
L1ERR_LD
PREV_CSC_L1ER
CSC_L1ER
ACC_ML1ERR
SOP4
LEVT_L1ERR
EVT_L1ERR
EVT_ML1ERR
IN_ML1A_ERR
MULTL1AERR
L1 Error
AND2
OR3
WCGE2F[3:0]
INMT[3:0]
SYS_RDY
IN_RDY
PAFIN[3:0]
FFIN[3:0]
FIFO_RDY
MTIN[3:0]
FIBEROK[3:0]
Page 4
START_TIMEOUT
END_TIMEOUT
EMPTY[3:0]
DATA_READY
NOT_READY
ONE_RDY
RDY[3:0]
NOTRDY[3:0]
LFOK[3:0]
MT[3:0]
FERR[3:0]
FPAF[3:0]
FFUL[3:0]
PAF_ERROR
FF_ERROR
FIBER_CHANGE
EMPTYF[3:0]
DATA_RDY
NOT_RDY
ONE_RDY
RDY[3:0]
N.L.
NRDY[3:0]
LFOK[3:0]
MT[3:0]
F_ERR[3:0]
FPAF[3:0]
FFULL[3:0]
PAF_ERR
FFERR
FIFO_CHG
Valid E-Code detected
GOLDDAT
DMB_END
DMB_END+1
DMB_END=DMBEND
=Ecode
FOK[3:0]
FDC
MULTL1AERR
ML1A_ERR
CSC_L1ERR
TMBERR
ALCTERR
DMB_L1ERR
L1A_MISMATCH
L1A_ERROR
DOFW+2
GOOD_L1A
L1 Error
PREV_CSC_L1ER
CSC_L1ER
CSC_MULTL1AERR
N.L.
(exclude DMB_Err case?)
LFOK[3:0]
SOME_FIBERS_OK
NO_LIVE_FIBERS
INV
END_TIMEOUT
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
DDU Input FIFO Control
DDU Controller
CMS CSC Electronics
BY JRG
PARENT PAGE 2
PROJECT D785C
DATE 3-25-2012_17:06
FILE FIFOCTRL . 1
PAGE 3



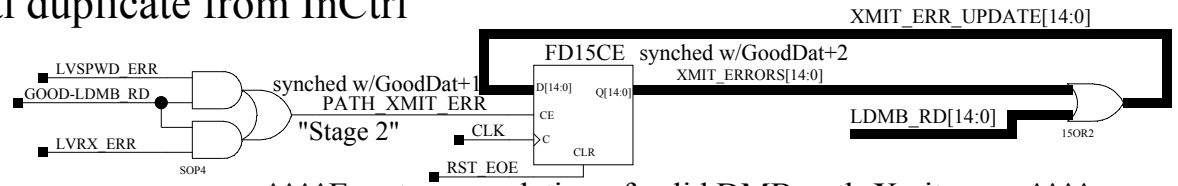
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Read Control DDU Input Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785C	
		DATE 3-4-2012_23:41		FILE FIFOCTRL . 2	PAGE 3A


Check for DMB Error Word and consistency:
ANYORALL
ERR0
ERR1
ERR2
ERR3
ANYDMBERR
ALLDMBERR
ALLDMBERR-
Page 10A
FMAP
LW
LREN_TRUE
OEFOK
FDONE
RENOE-1
RLOC=X0Y0
OUT63
OUT61
OUT60
OUT62
OUT47
OUT45
OUT44
OUT46
OUT15
OUT13
OUT12
OUT14
OUT31
OUT29
OUT28
OUT30
AND4B1
AND2
FDONE_SHDW-1
LOW means FIFO REN+OE are unconditionally Enabled
FDONE & RENOE-0 in-time with LGoodLW, next-to-last word (E-codes) on DAT
timed w/LgoodLW; LastWord is out of FIFO if it wasn't Empty
next-to-last word clocked in
FDPE
PRE
MAXDELAY=1.9NS
made 0.3ns
Check consistency of the four "Special Word" bits:
SP3_ANY
SP3_ERR
2-logic-step delay
synched w/GoodDat
RXER0
RXER1
OLD_RX_ERR
ERR
"FILL Flag"
FDCE
FDONE-1
FDONECE
FDONE_RST
LEND_TIMEOUT
FIFODONE
LFIFODONE
FDC
SP0_ERR
SP1_ERR
SP2_ERR
SP3_ERR
SPWD_ERR
FIFOdone set at E-codeDone & LRENtrue^^^
A FIFO ends at 1st false "LFIFO_EMPTY" after "LGoodLW"
SP2_ERR
END-C-CODE-1
END-C-CODE
"FDONE" indicates "LGoodLW" was received: waiting for the final NotEmpty word from FIF
------> Switch FIFOs after next good word!
------> "RENOE-0" holds REN enabled until "FDONE" goes false
FD4RE
DAT16
DAT53
SP1_ERR
RST_INSTAT
IN_STAT8
IN_STAT9
IN_STAT10
IN_SING_WARN
LIN_SING_WARN
IN_TIMEOUT
IN_TIME_OUT
RST_EOE
2ORMOREP
VBIT15
VB15
LVB15
synched w/GoodDat+1
Page 10
SP0_ERR
synched w/GoodDat
Cleared if not C-Code
FD12CE
IN_STAT[11:0]
FBIN_STAT[11:0]
LIN_STAT[11:0]
12OR2
IN_ML1A_ERR
IN_STAT11
OUT[59:52]
FD8RE
IN_STAT[7:0]
LINFERR
LINSYNC
LINHARD
LINL1ERR
IN_STUCK
IN_MXMIT
IN_FERR
IN_MEMERR
IN_SING
IN_SYNC
IN_HARD
LINSING
RST_BOE
VB13
VB14
VB12
END-C-CODE
DOFW+2
GOLDDAT
C_CODE
OR2B1
RST_INSTAT
SOP3
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
TITLE
Read Control
DDU Input Controller Logic
CMS CSC Electronics
BY
JRG
PARENT PAGE
2
PROJECT
D785C
DATE
11-27-2007_9:58
FILE
FIFOCTRL . 3
PAGE
3B

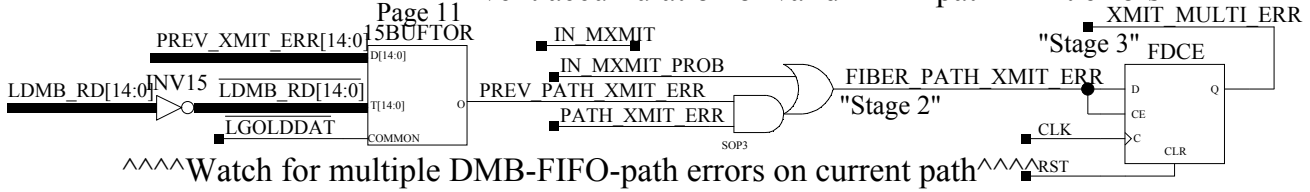
Control Bit List:

0: Gold Data (Active DMB has REN, OE, notMT, LFOK)
1: DMB First Word Mode
2: Latched Voted Special Bit 12 {2 or more out of 4}
3: Latched Voted Special Bit 13 {2 or more out of 4}
4: Latched Voted Special Bit 14 {2 or more out of 4}
5: Latched Voted Special Bit 15 {2 or more out of 4}
6: Do Header Mode (Header to Output)
7: Word Count Enable (DDU Header, DMB Data)
8: End of Event (DONE--->OETrail)

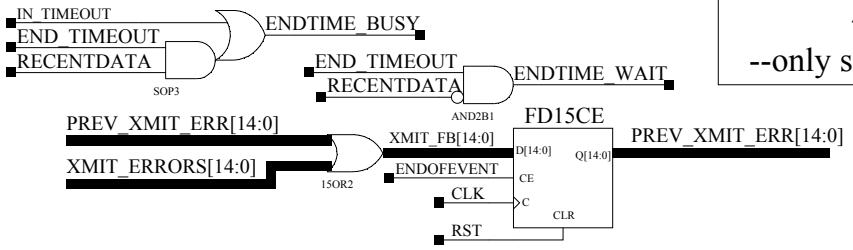
Virtual duplicate from InCtrl



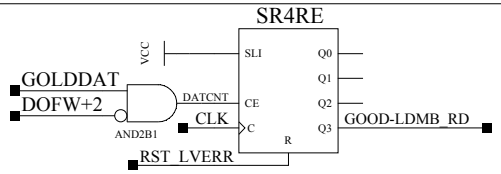
^^^^Event accumulation of valid DMB-path-Xmit errors^^^^

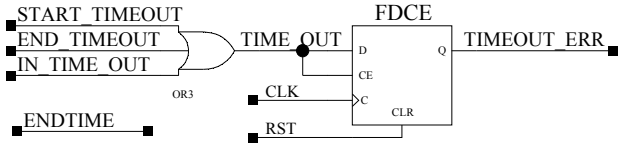


^^^^Watch for multiple DMB-FIFO-path errors on current path^^^^
--only sets errors for separate-event case or InMultXmit case

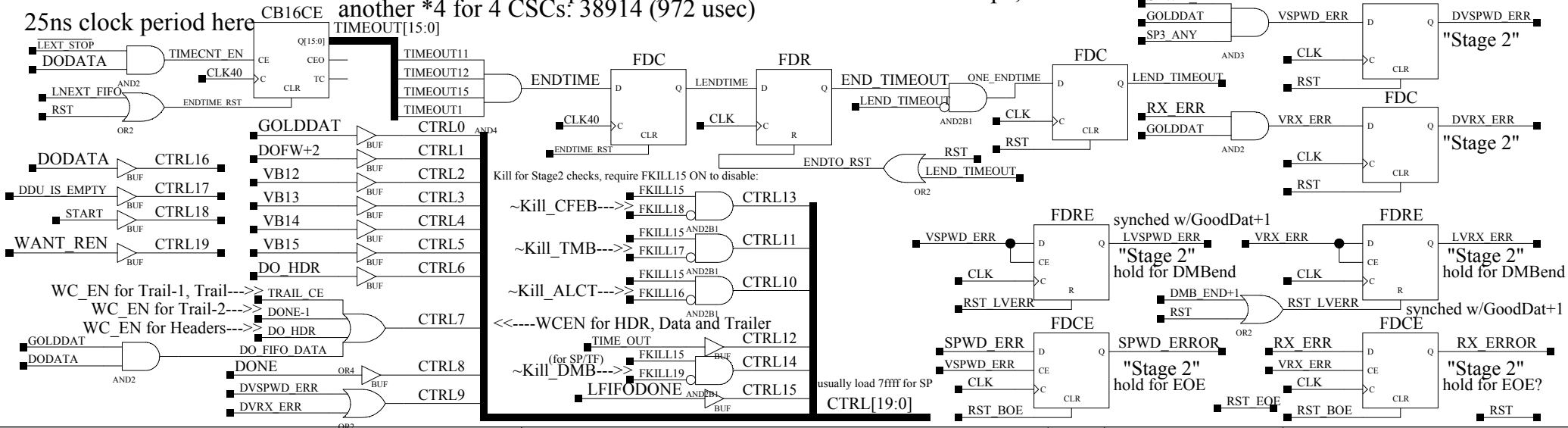


^^^^Permanent accumulation of DMB-path-Xmit errors^^^^





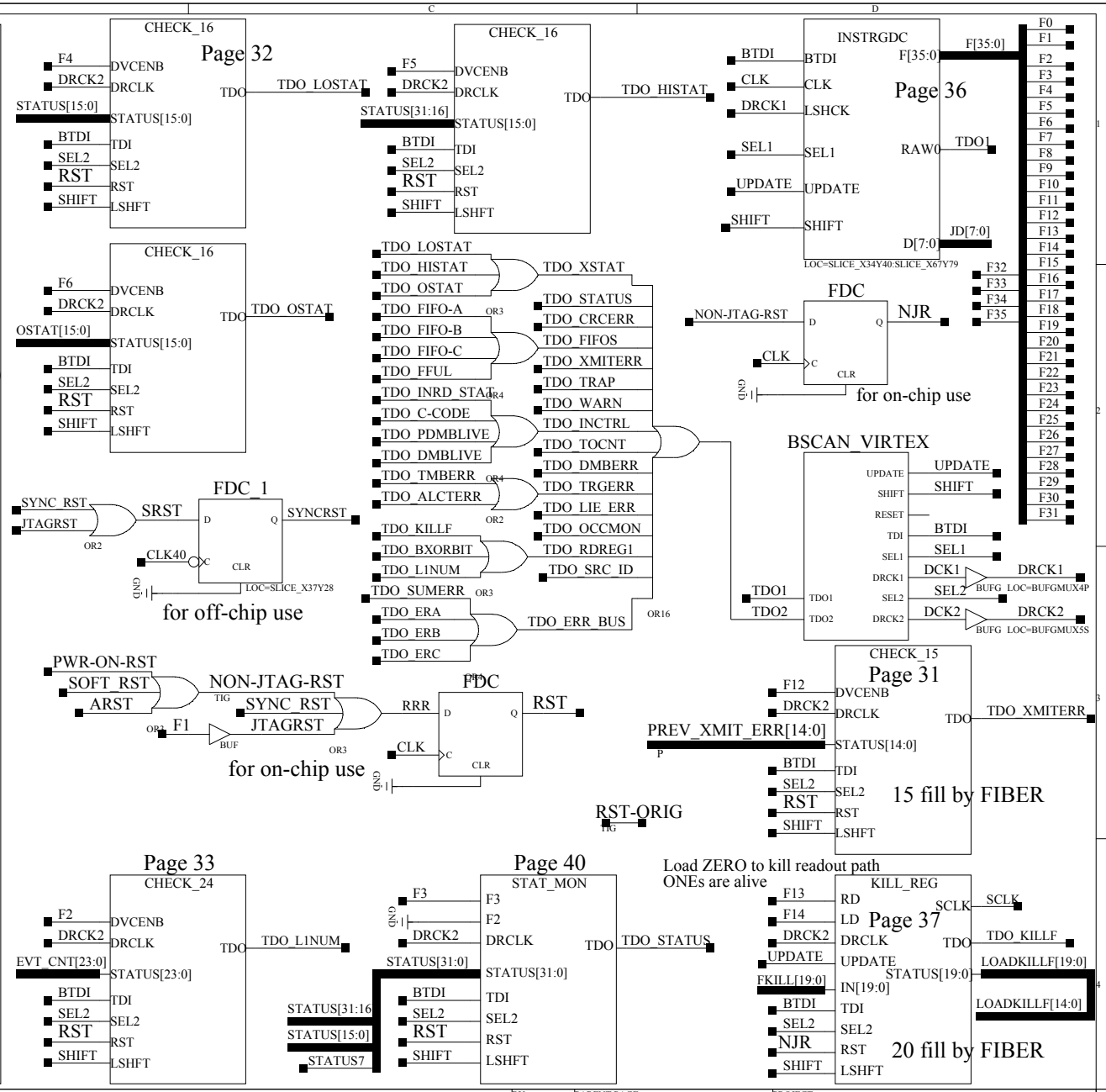
FIFO Done Timeout: 132 usec=5281 is the worst case per CSC, add about 100 usec w/TMB scope, then another *4 for 4 CSCs: 38914 (972 usec)
25ns clock period here



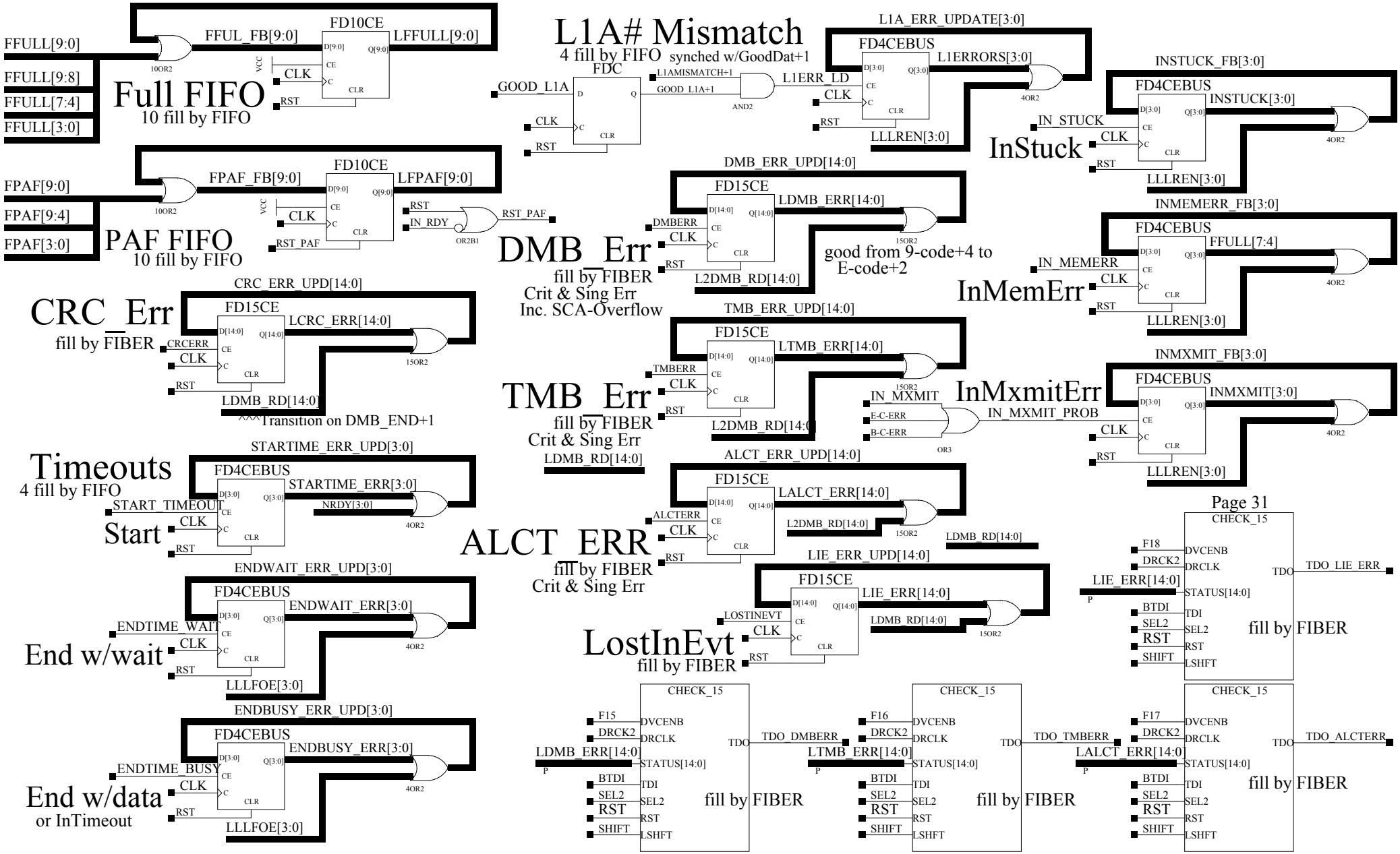
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 3-4-2012_23:55	FILE: FIFOCTRL . 4	PAGE: 3C

JTAG Instruction Decode

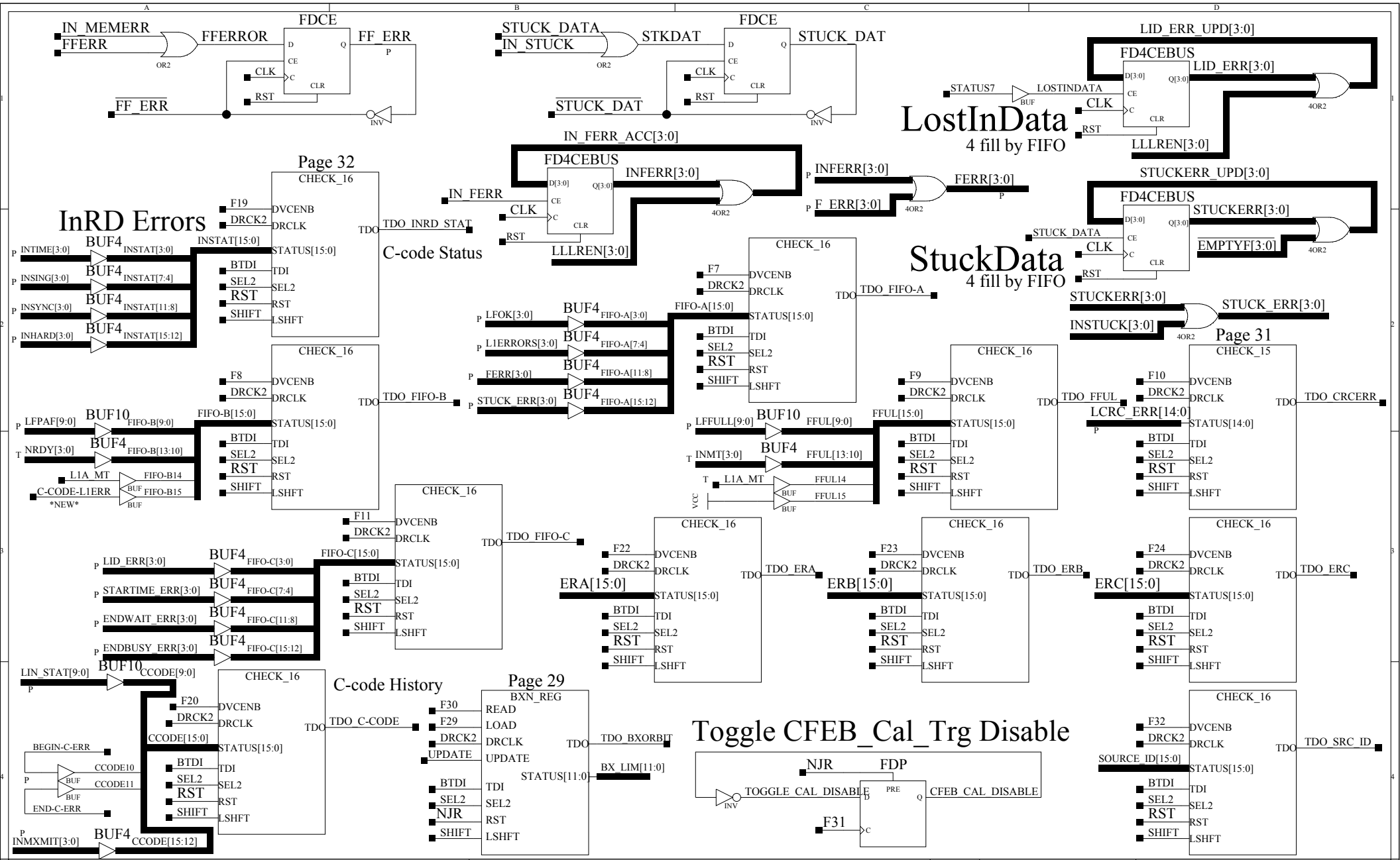
OpCode	Function [OpName]	
0	No Operation [NOOP]	
1	FPGA Reset [toggle]	
2	Read Current DDU L1A Number (24-bit scaler)	
3	Check status (capture and shift) [32 bits]	
4	Check status, low-word [16 bits]	
5	Check status, high-word [16 bits]	
6	Output Path Status [16-bits]	
7a	Check FOK (active input FIFOs) [lowest 4 bits]	
7b	L1A Mismatch (FIFO headers) [4-bits]	check FIFO-A
7c	Check FIFO Err (active FIFO change) [4 bits]	
7d	Stuck Data Errors (input FIFOs) [highest 4-bits]	
8a	Almost Full FIFOs [lowest 10-bits]	check FIFO-B
8b	FIFO Empty/GE2 Status [highest 6-bits]	
9a	Full FIFOs [lowest 10-bits]	FIFO Full/MT (raw)
* 9b	Raw FIFO Empty [highest 6-bits]	
10	CRC Errors [15-bits]	
11a	Lost In Data [lowest 4-bits]	check FIFO-C
11b	Timeout: start [4-bits]	
11c	Timeout: end-wait [4-bits]	
11d	Timeout: end-active [highest 4-bits]	
12	Data Xmit Errors [15-bits]	
13	Check KILL_Register [20 bits]	
14	Load KILL_Register [20 bits]	
15	DMB Errors [15-bits]	
16	TMB Errors [15-bits]	
17	ALCT Errors [15-bits]	
18	Lost In Event [15-bits]	
* 19	InRD Status [16-bits]	
* 20	InRD C-code & MxmitErr History [16-bits]	
* 21	Critical Error Trap Reg. [192 bits]	
22	Error Register A [16-bits]	
23	Error Register B [16-bits]	
24	Error Register C [16-bits]	
25	Read DMB_LIVE [15-bits]	
26	Read P_DMB_LIVE [15-bits]	
27	Read WARN_MON [16-bits]	
* 28	Max Timeout Count [16-bits]	
29	Set BX per Orbit [12-bits]	
30	Read BX per Orbit [12-bits]	
31	Toggle CFEB_Cal Auto_L1 [default enable]	
32	Read DDU Source ID [16-bits]	
33	DDU-only VME_L1A	
* 34	Read CSC Board Occupancy scalers (loops for 60 words, 32-bit)	
35	Sum of Errors for each CSC [15-bits]	



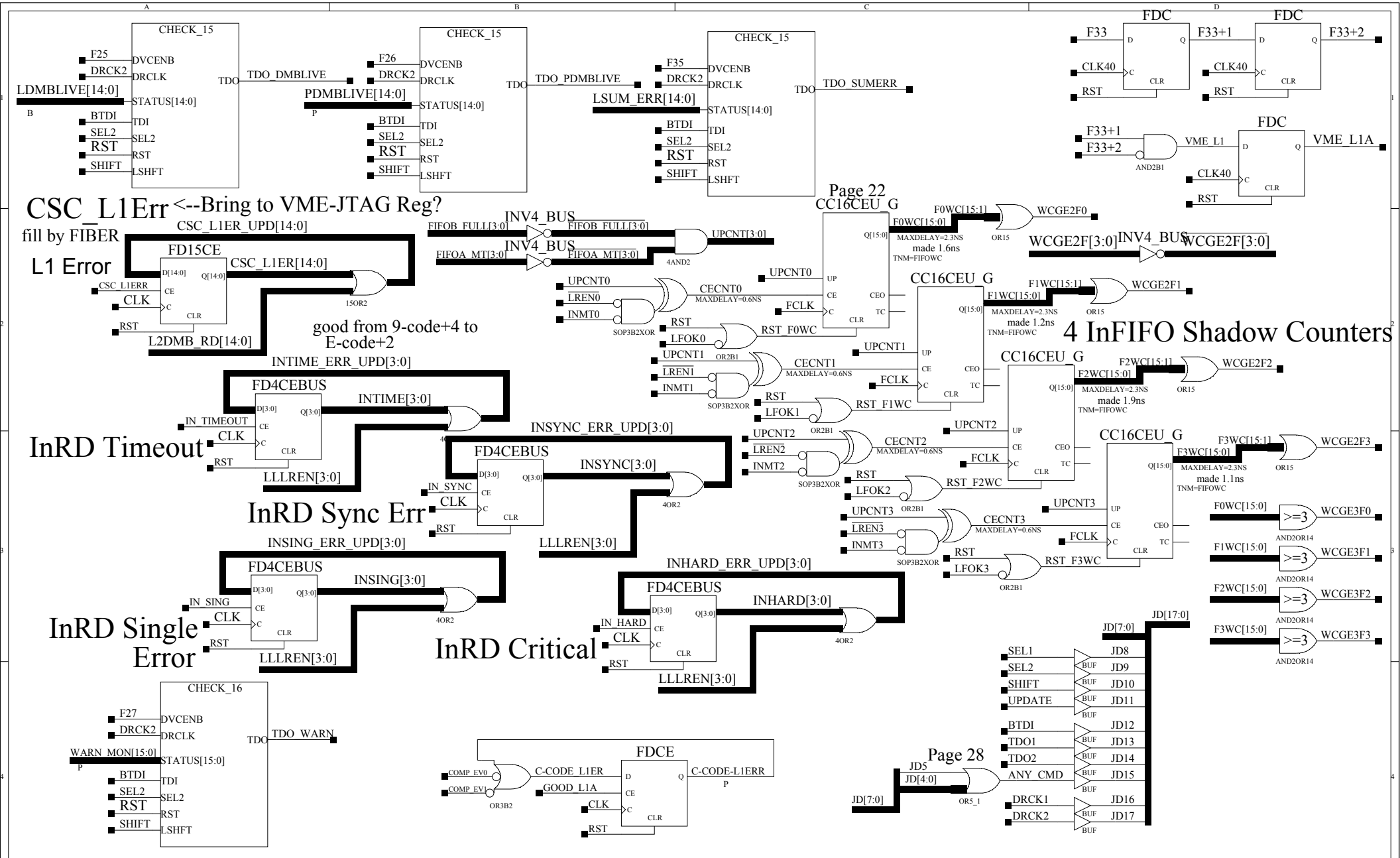
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Signals DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 3-2-2012_18:28	FILE: FIFOCTRL . 5	PAGE: 3D



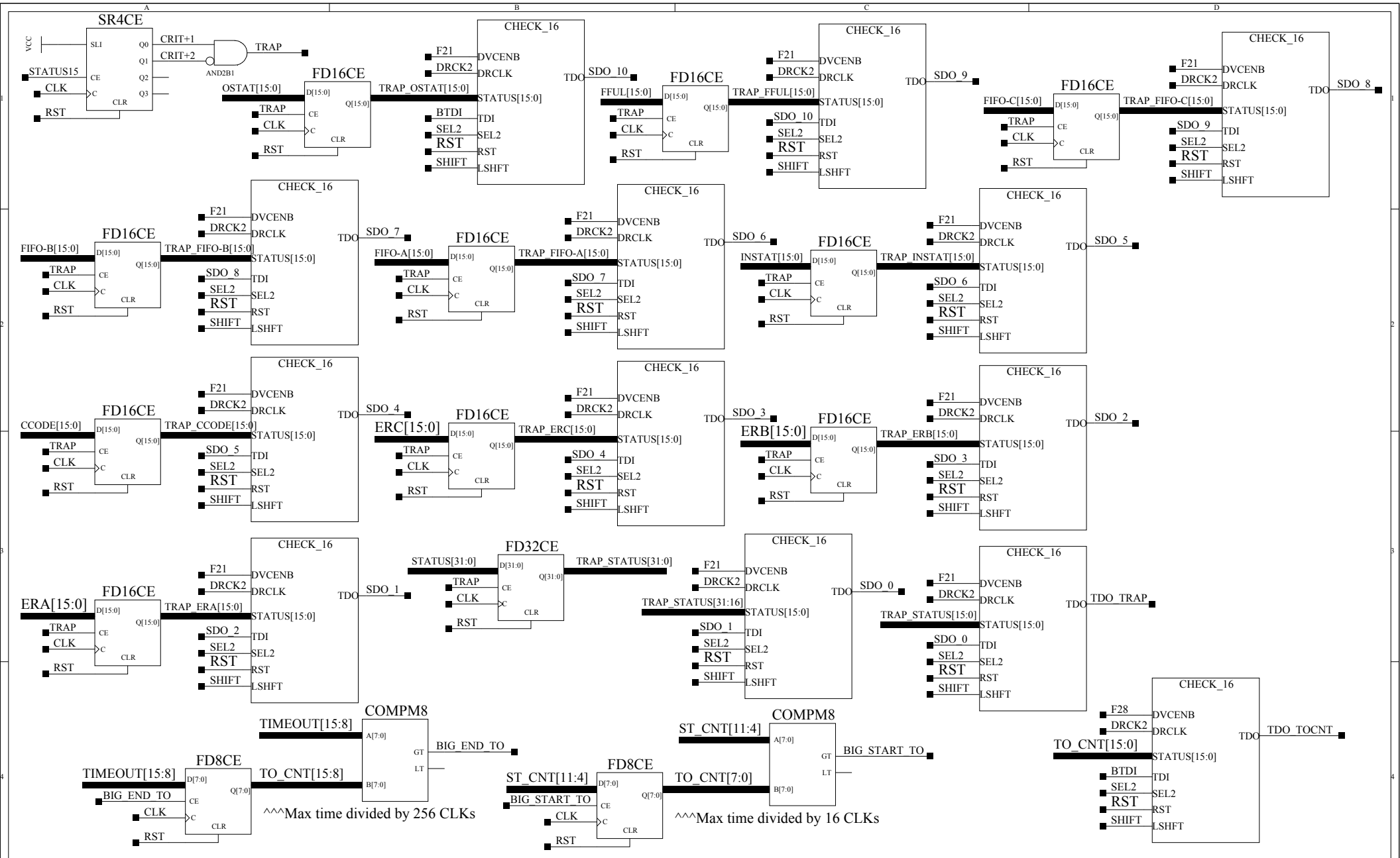
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-9-2006_15:30	FILE: FIFOCTRL . 6	PAGE: 3E



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG DATE: 8-14-2008_16:21	PARENT PAGE: 2 FILE: FIFOCTRL . 7
		PROJECT: D785C	PAGE: 3F

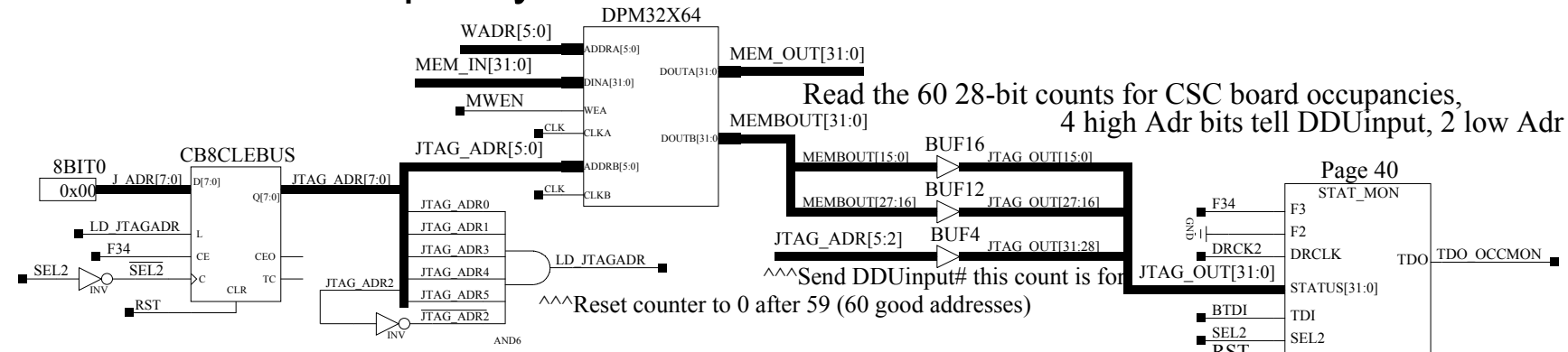


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785C
			DATE 8-14-2008_16:14	FILE FIFOCTRL . 8	PAGE 3G



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Critical Error Trap DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 5-23-2006_14:23	FILE: FIFOCTRL . 9	PAGE: 3H

CSC Board Occupancy Tracker: 15 fibers x 4-boards each

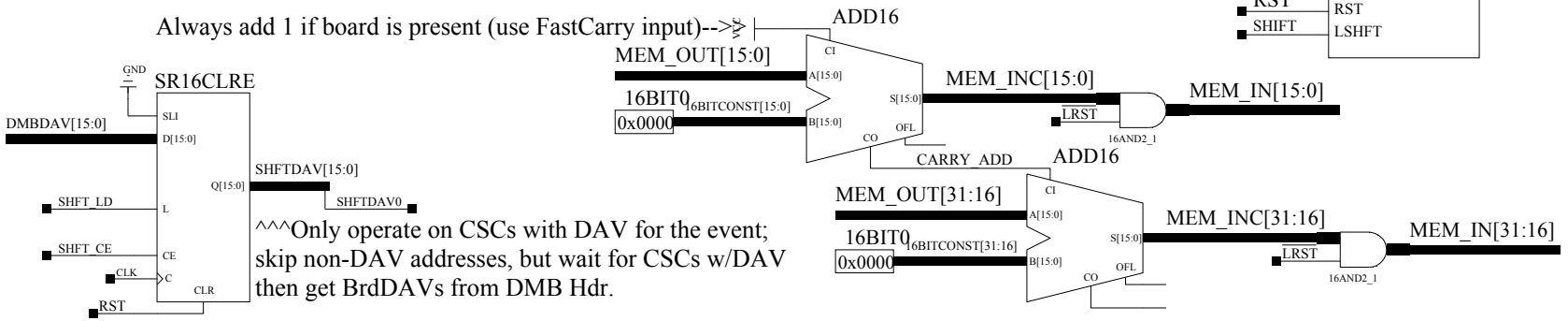


Read the 60 28-bit counts for CSC board occupancies,
4 high Adr bits tell DDUinput, 2 low Adr bits specifiy Board Type:
0 = DMB
1 = ALCT
2 = TMB
3 = CFEB

^^^Send DDUinput# this count is for

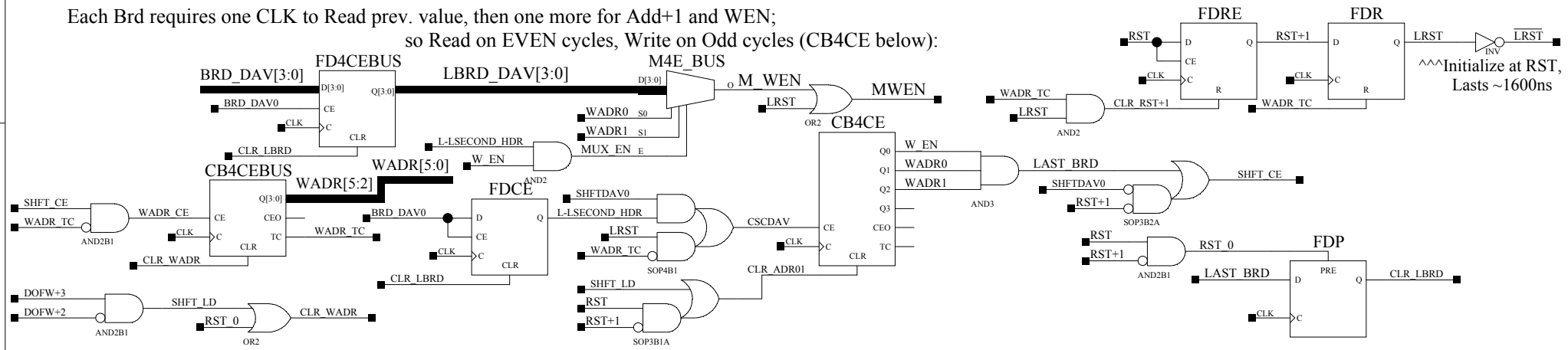
^^^Reset counter to 0 after 59 (60 good addresses)

Always add 1 if board is present (use FastCarry input)-->

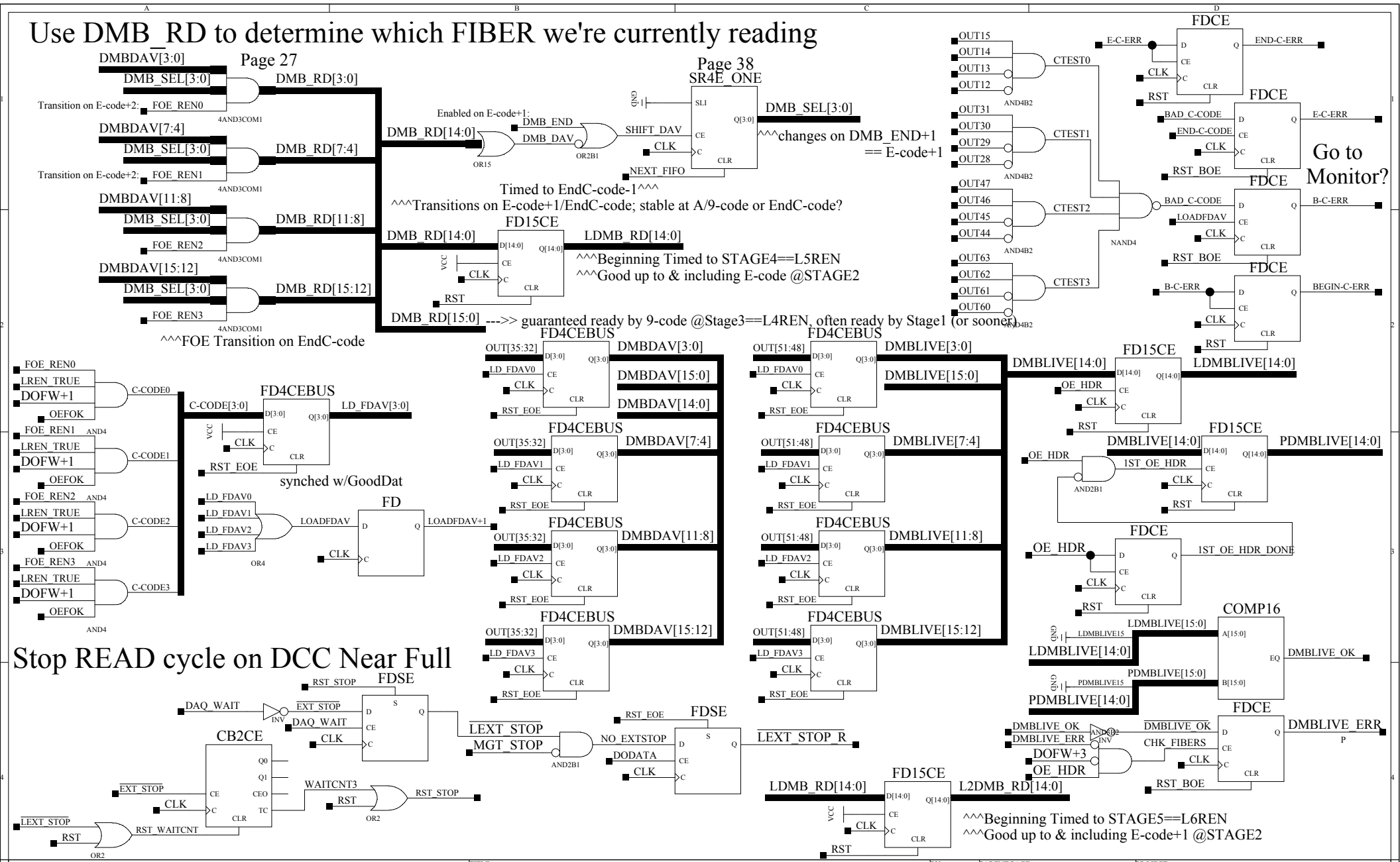


^^^Only operate on CSCs with DAV for the event;
skip non-DAV addresses, but wait for CSCs w/DAV
then get BrdDAVs from DMB Hdr.

Each Brd requires one CLK to Read prev. value, then one more for Add+1 and WEN;
so Read on EVEN cycles, Write on Odd cycles (CB4CE below):

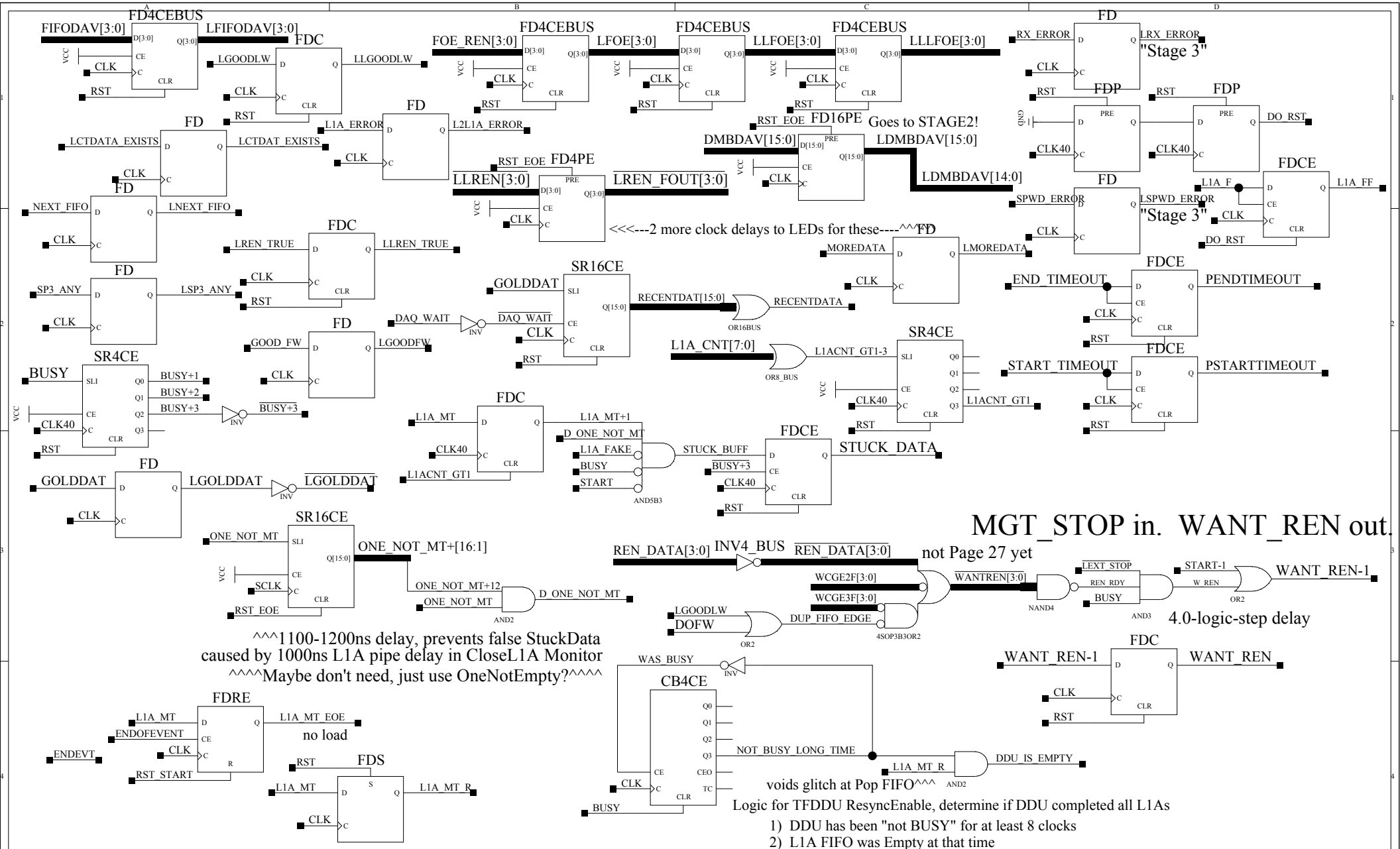


Use DMB_RD to determine which FIBER we're currently reading



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE	DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY	JRG	PARENT PAGE	2
		DATE	3-5-2012_0:59	PROJECT	D785C
		FILE	FIFOCTRL . 11	PAGE	3J

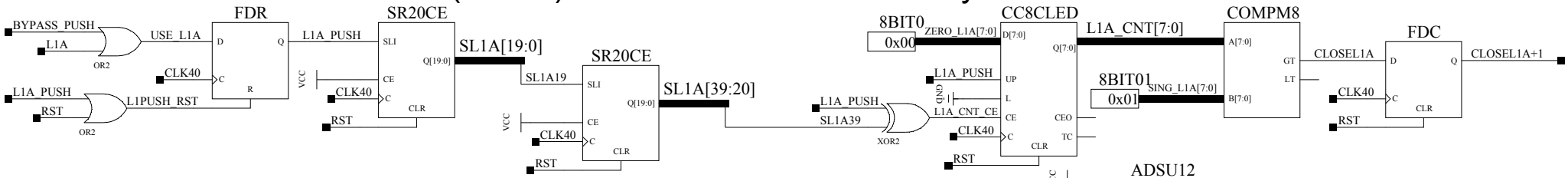


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C	
		DATE: 3-25-2012_15:19		FILE: FIFOCTRL . 12	PAGE: 3K

L1A Proximity Tracker: 1000ns Close L1A Monitor

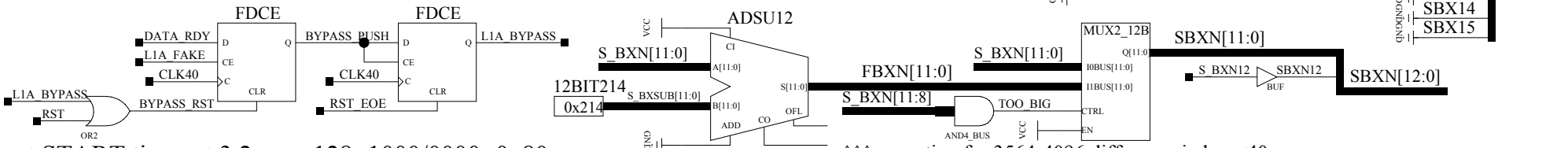
(40 BX) closer than 950ns is Tricky for DMBs

END



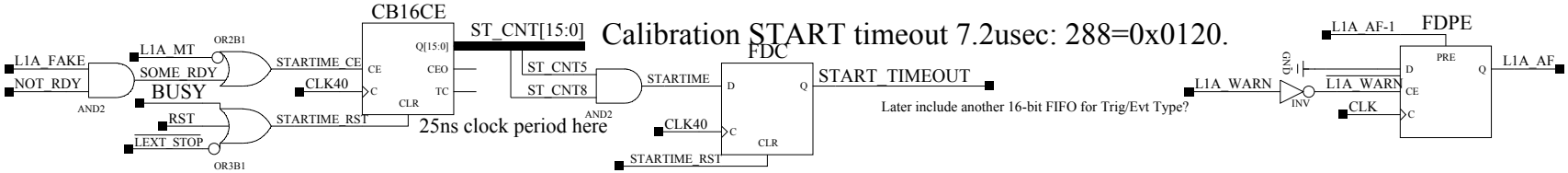
Pipe all L1As for 1000ns, if more than 1 then set CloseL1A bit^^^

Finally, perform BX-40 to correct BXN and store CloseL1A as BXN bit-12 (& correct for BX<40 case).
Then use SBXN12 output (Close_L1A) for Stage2 DMB checks: 1000+ ns L1As means
that first 2 CFEB samples should always have good L1A#



Event START timeout 3.2usec: 128=1000/0000=0x80....

^^^correction for 3564-4096 difference in bxn<40 case

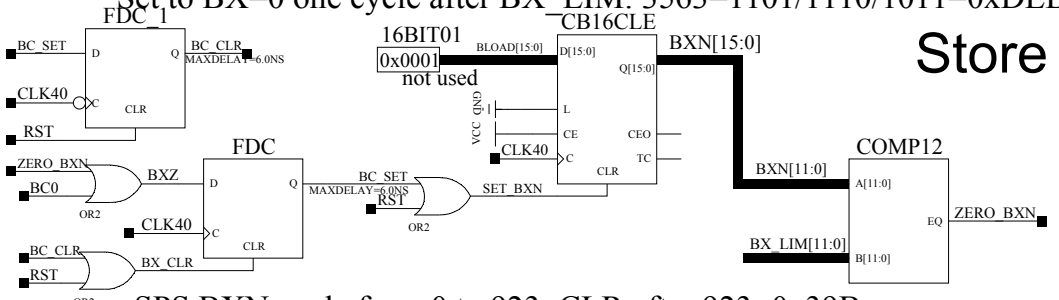


Calibration START timeout 7.2usec: 288=0x0120.

25ns clock period here

LHC BXN cycles from 0 to 3563

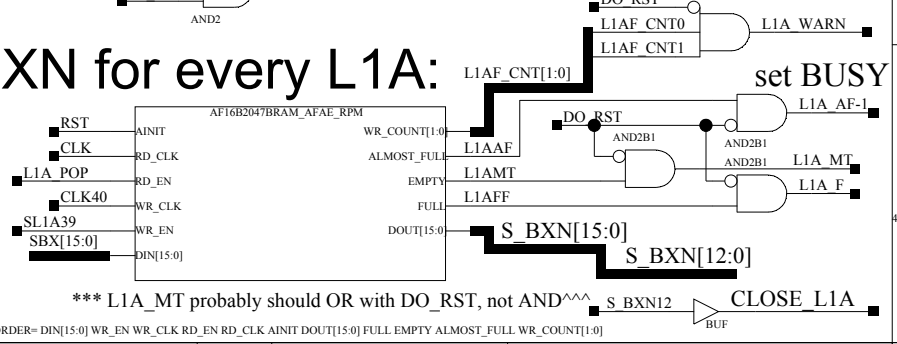
Set to BX=0 one cycle after BX_LIM: 3563=1101/1110/1011=0xDEB



SPS BXN cycle from 0 to 923: CLR after 923=0x39B.

NO_LIVE_FIBERS
ST_CNT5
AND2
NONE_LIVE_GO

Store the BXN for every L1A:

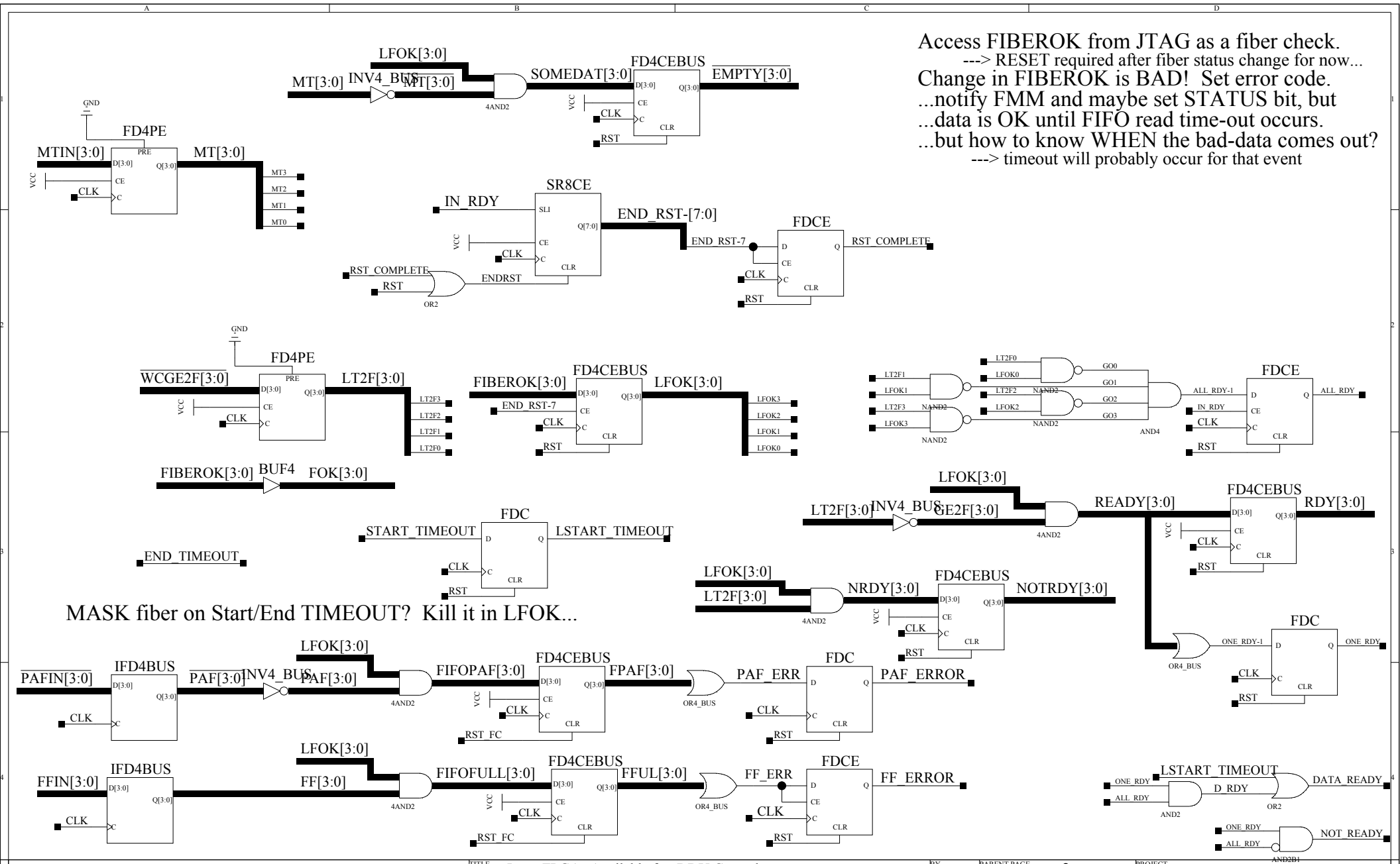


*** L1A_MT probably should OR with DO_RST, not AND^^^

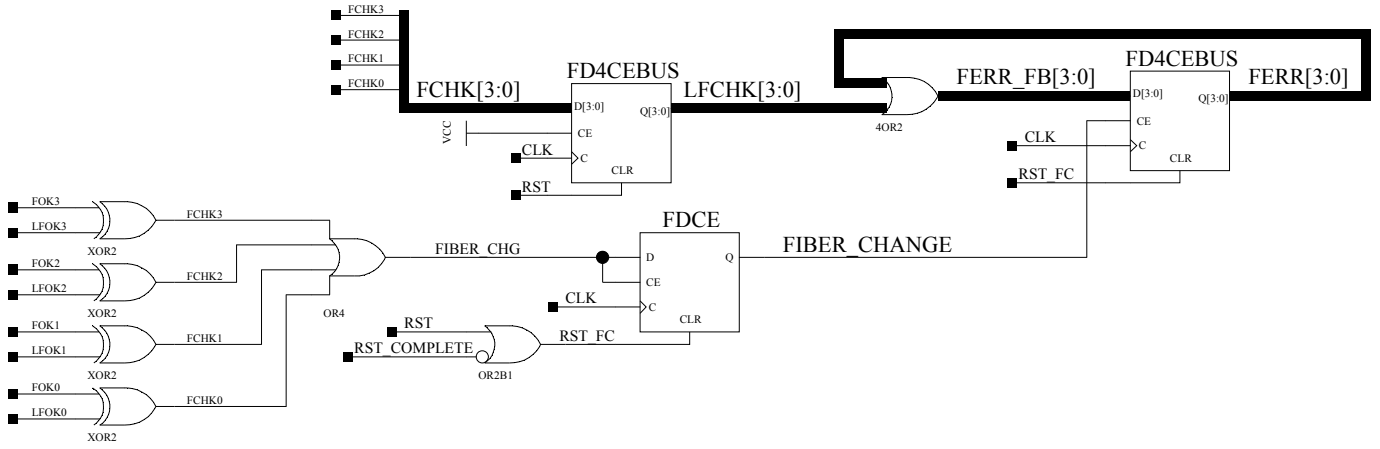
PINORDER= DIN[15:0] WR_EN WR_CLK RD_EN RD_CLK AINIT DOUT[15:0] FULL EMPTY ALMOST_FULL WR_COUNT[1:0]

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

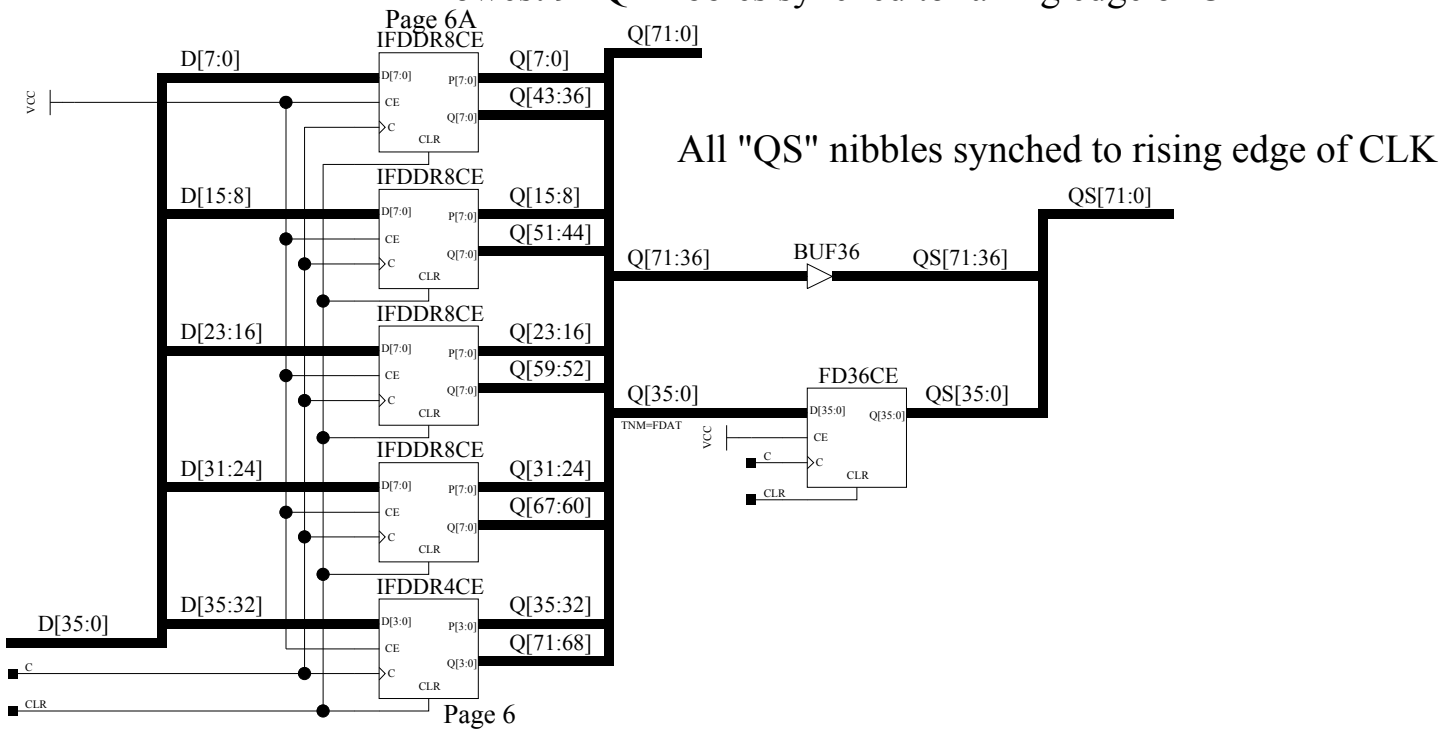
TITLE	DDU Input FIFO Control DDU Controller CMS CSC Electronics	BY	JRG	PARENT PAGE	2
		DATE	3-2-2012_18:30	PROJECT	D785C
		FILE	FIFOCTRL . 13	PAGE	3L



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Input FPGAs Available for DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 9-12-2006_10:43	FILE: FIFO_RDY . 1	PAGE: 4



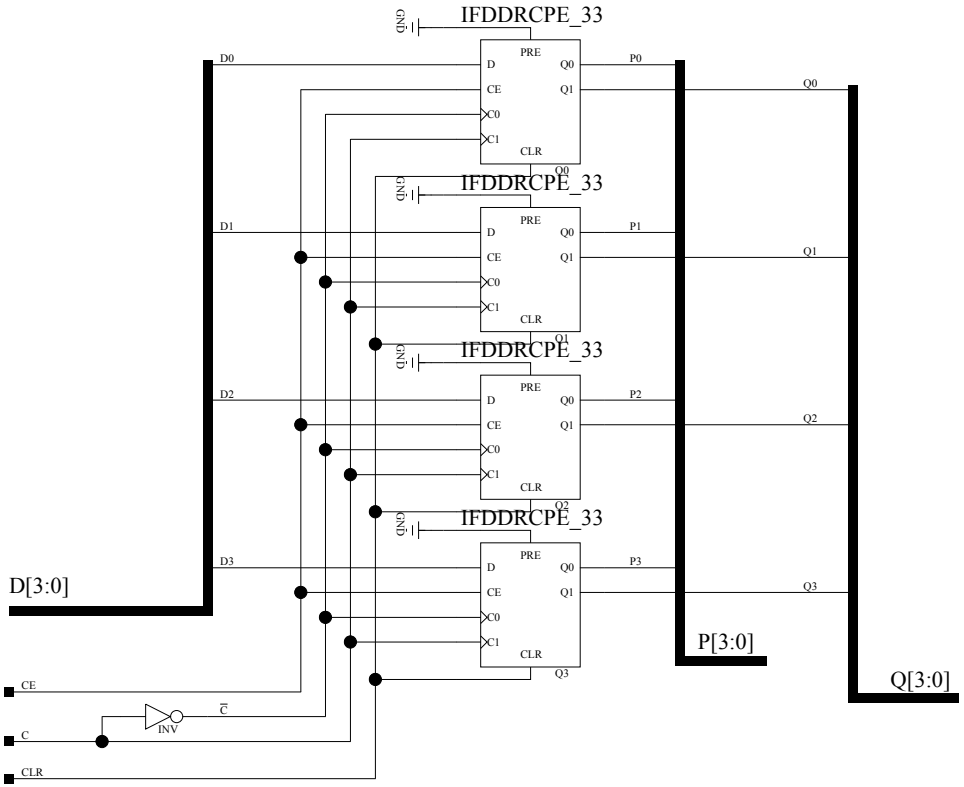
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Inputs from DMB FIFOs to DDU Control DDU Input Controller Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 3	PROJECT: D785C
		DATE: 9-12-2006_10:43	FILE: FIFO_RDY . 2	PAGE: 4A



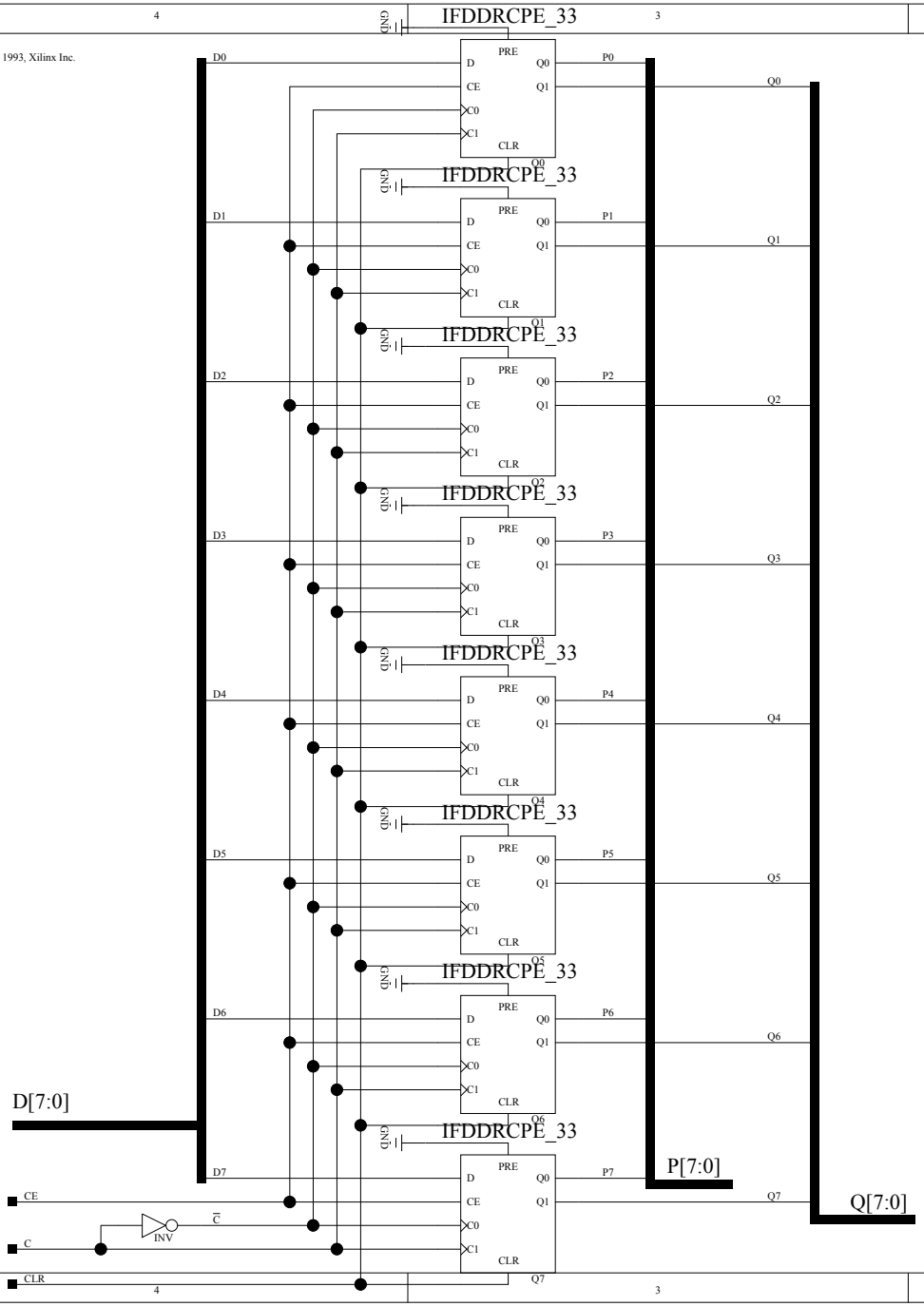
CLK/\ -- DIN[35:0] -- CLK\/ -- Q[35:0] DIN[71:36] -- CLK/\ -- Q[71:36] QS[35:0]

XILINX			
Title:	VIRTEX Family IFDDR36C Macro, LVCMOS33		
Comments:	36-Bit DDR Input Flip-Flop with asynchronus clear	JRG	
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A

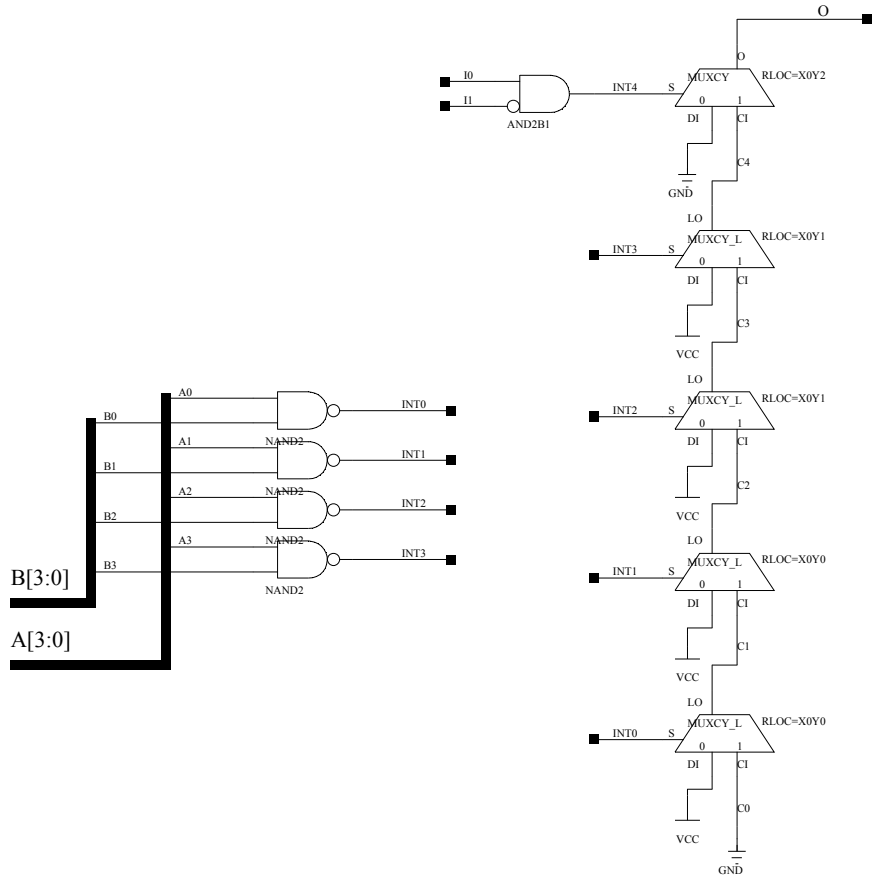
drawn by KS



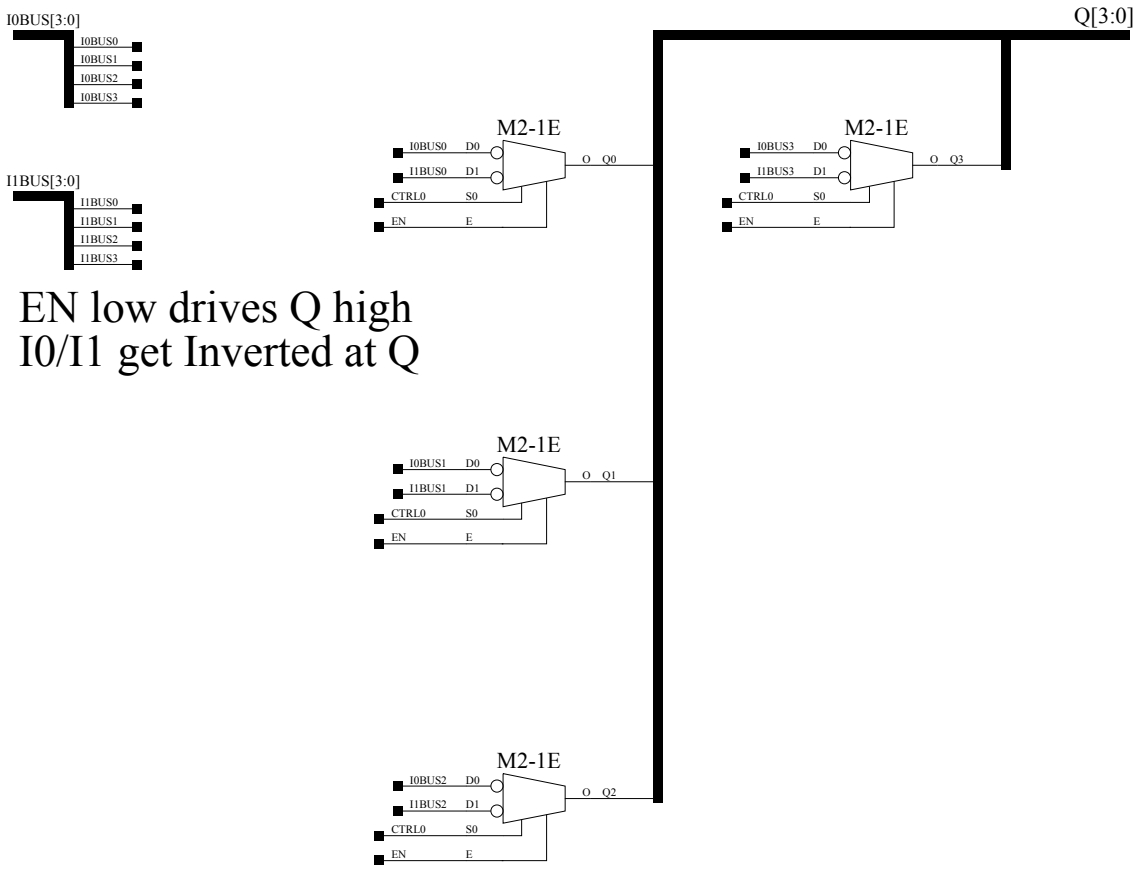
XILINX			
Title:	VIRTEX Family IFDDR4CE Macro, LVCMOS33		JRG
Comments:	4-Bit Double-Data-Rate Input Register w/ Clock Enable & Asynchronous Clr		
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A



Title:	VIRTEX Family IFDDR8CE Macro, LVCMOS33		JRG
Comments:	8-Bit Double-Data-Rate Input Register w/ Clock Enable & Asynchronous Clr		
Date:	10th December 2003	Ver:	1
Sheet Size: B		Rev:	A



XILINX			JRG
Title:	FAST10B1		
Comments:	Custom Fast, Complex Logic for DDU, use 4 MUXCY as OR, 1 as AND similar to: OR of 4 AND2 .AND. AND2B1		
Date:	15th October 2003	Ver:	1
Sheet Size: B		Rev:	A



EN low drives Q high
I0/I1 get Inverted at Q

THE OHIO STATE UNIVERSITY
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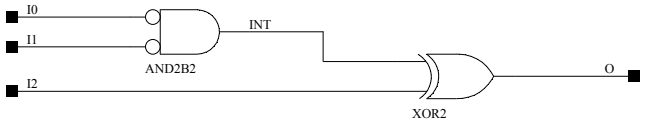
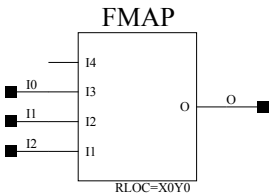
174 WEST 18TH AVE, COLUMBUS OH 43210

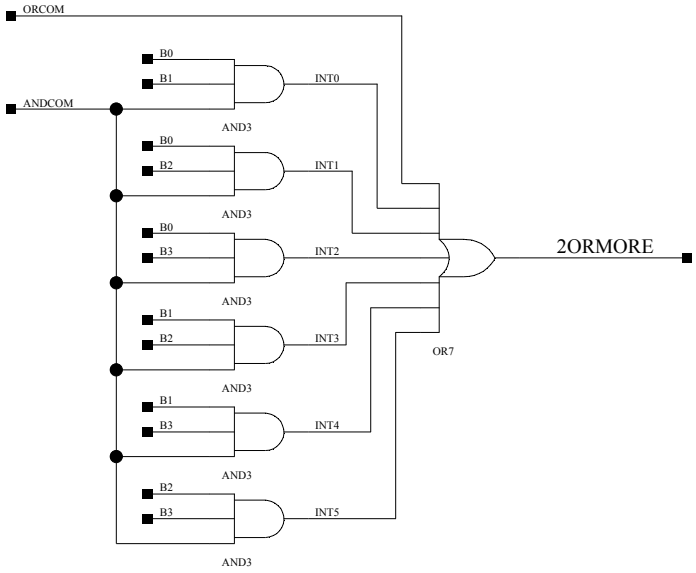
TITLE: 4-bit MUX for 2 4-bit Inputs, w/Enable, invert selected DIN
DDU Input Controller Logic
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	3	D785C
DATE	FILE	PAGE
5-24-2005_14:02	MUX2_4B_INV . 1	8

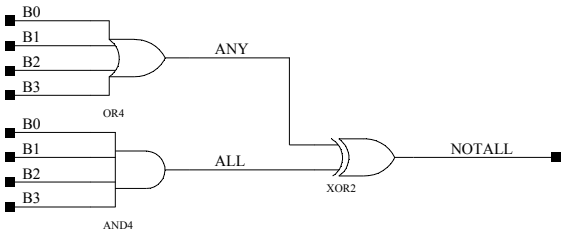




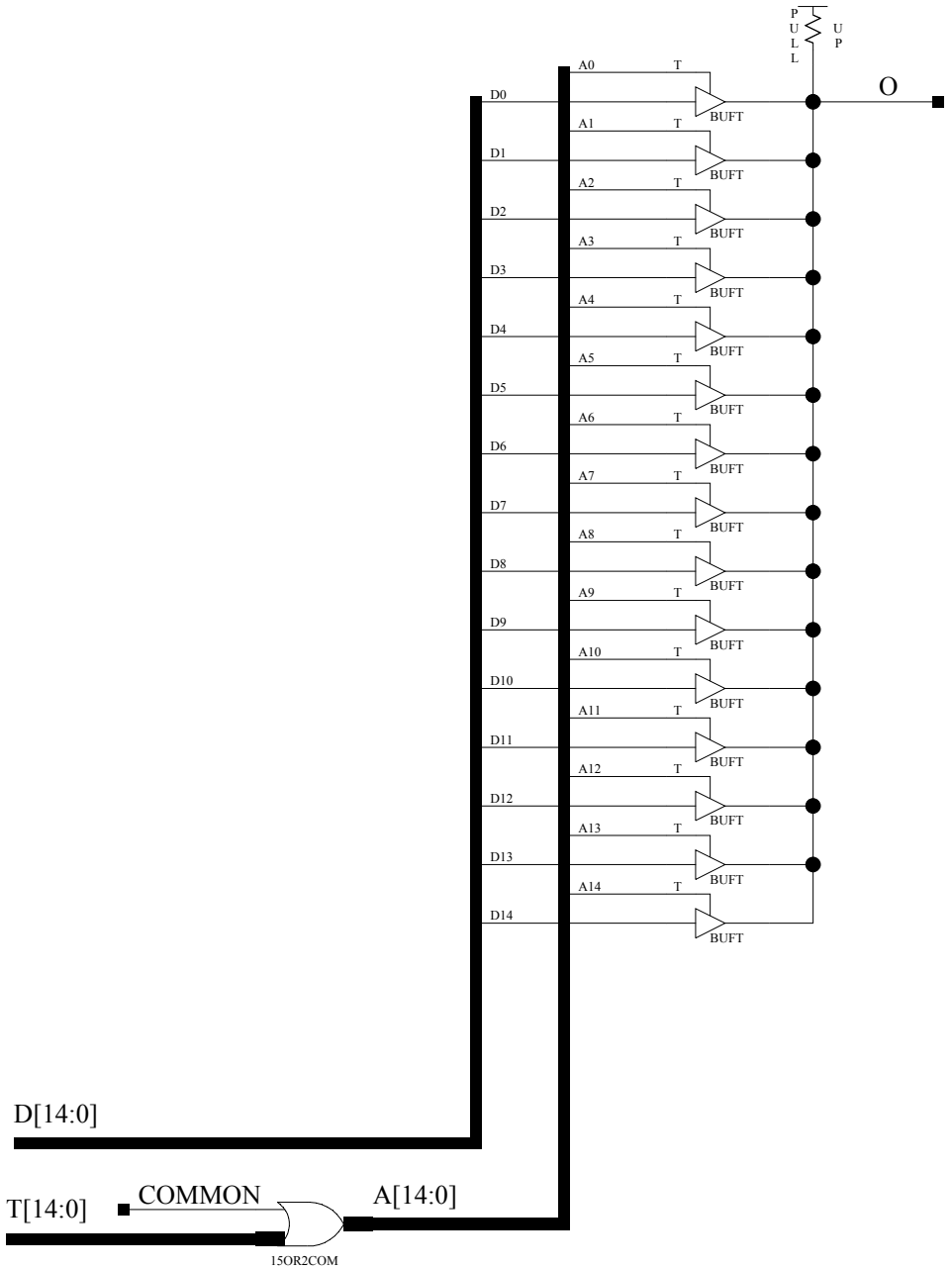
Title:	VIRTEX Family SOP3B2XOR Macro
Comments:	SOP3B2XOR Gate
	JRG
Date:	11th December 2003
Ver:	1
Sheet Size: A	
Rev:	A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Check for 2 Or More Bits Set Out of 4, PLUS common AND and OR bits DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 3	PROJECT D785C
			DATE 7-18-2005_17:01	FILE 2ORMOREP . 1	PAGE 10



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Check for ALL bits set, ANY bits set and NOTALL bits set DDU Controller CMS CSC Electronics	BY: JRG DATE: 7-18-2005_17:01	PARENT PAGE: 3	PROJECT: D785C FILE: ANYORALL . 1 PAGE: 10A



XILINX

Title: VIRTEX Family 15-BufTOR Macro

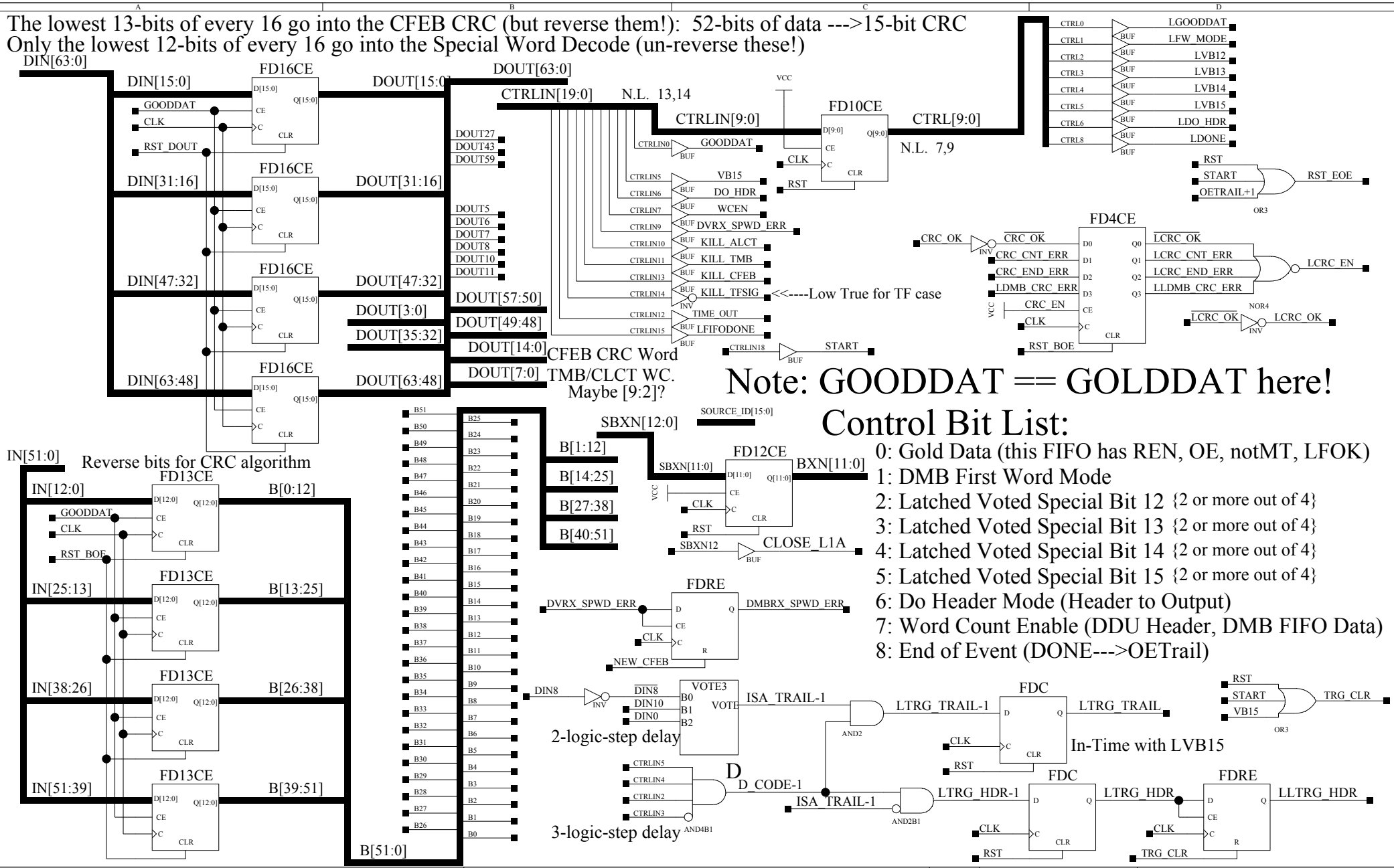
Comments: 15-BufT Bus Gate with Bus-OR-Common control

JRG

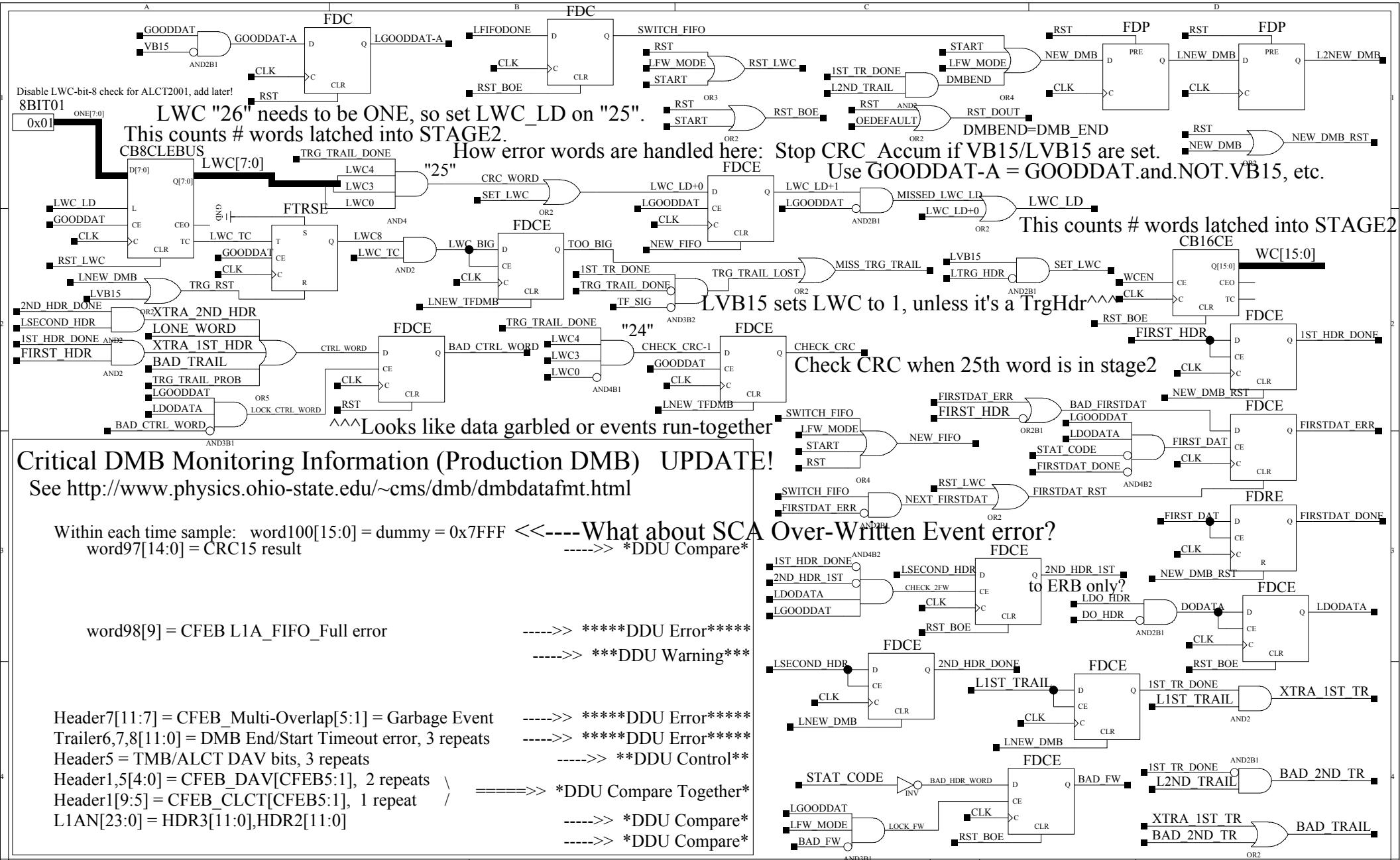
Date: 27th December 2001 Ver: 1

Sheet Size: A Rev: A

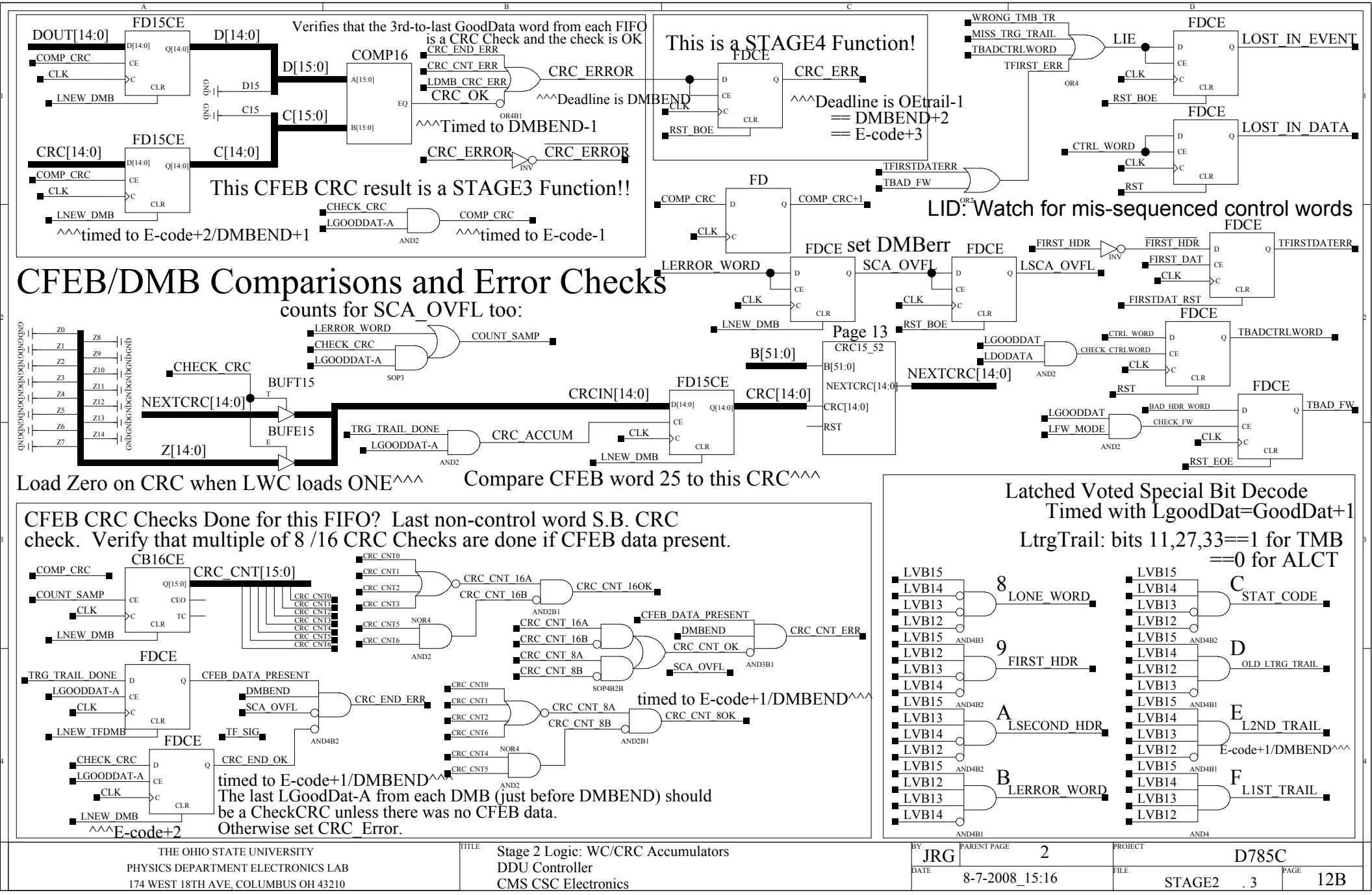
drawn by KS



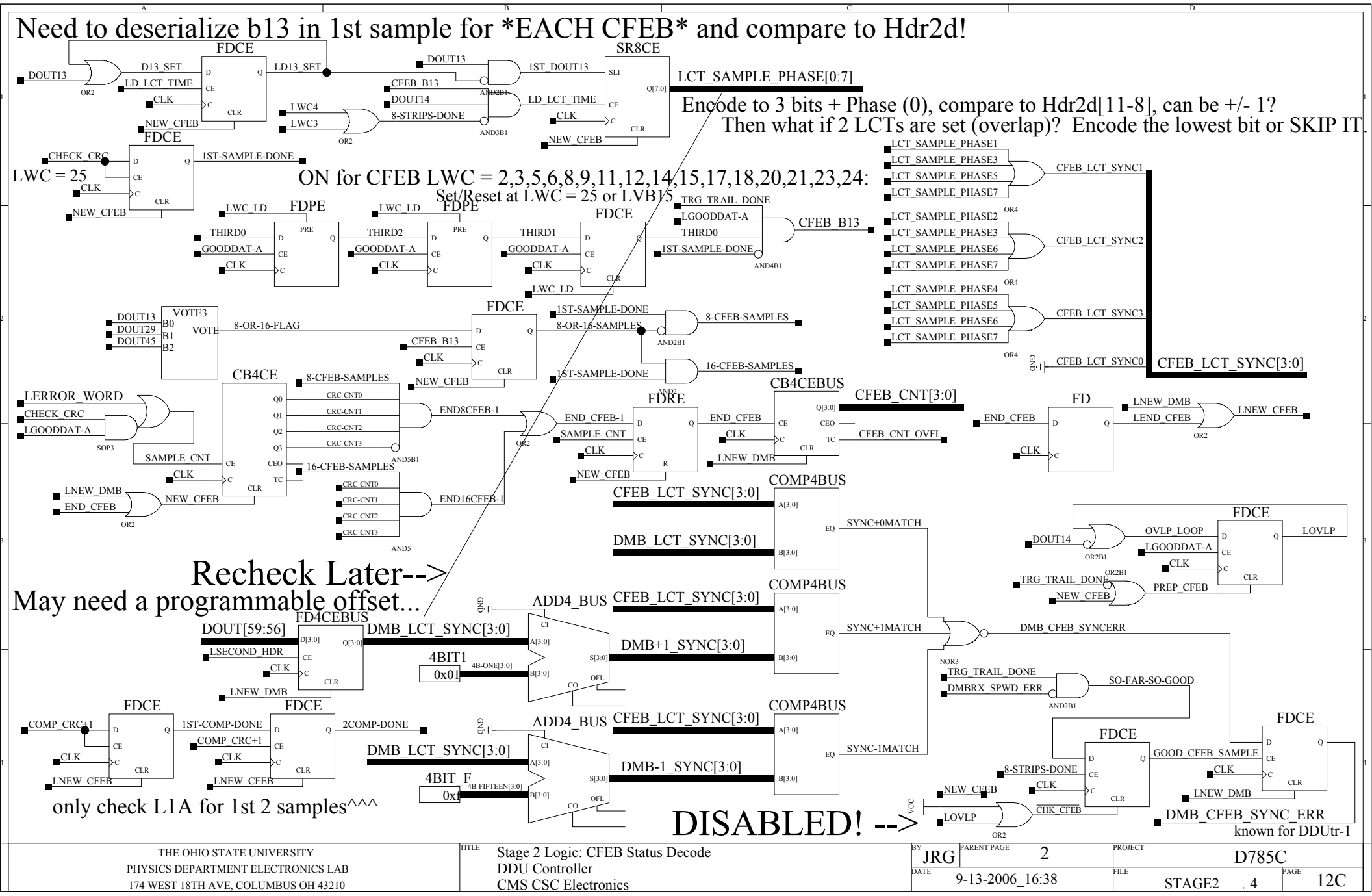
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG PARENT PAGE: 2 DATE: 3-5-2012_0:39	PROJECT: D785C FILE: STAGE2 . 1 PAGE: 12

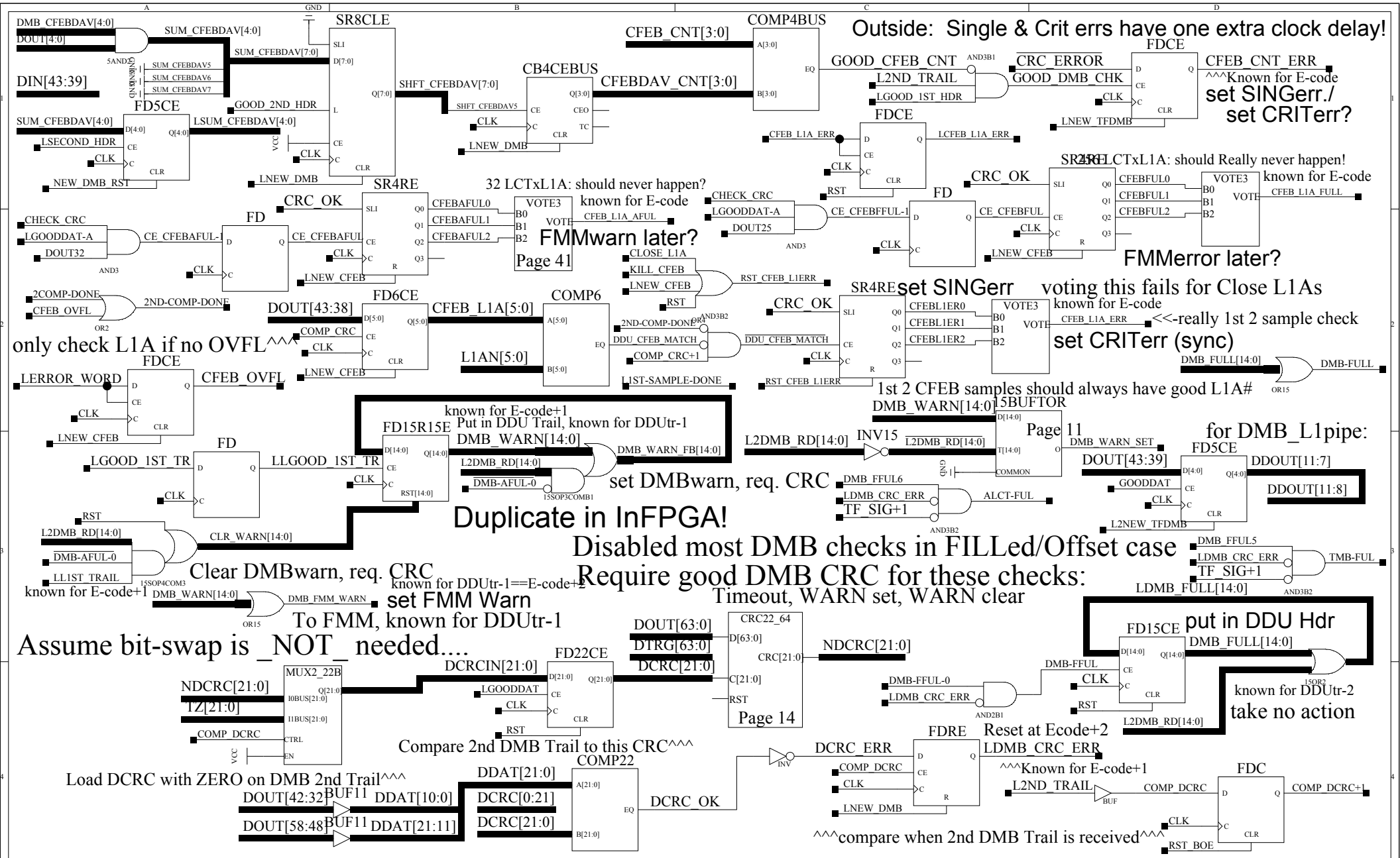


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-17-2007_16:35	FILE: STAGE2 . 2	PAGE: 12A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: WC/CRC Accumulators DDU Controller CMS CSC Electronics	BY: JRG DATE: 8-7-2008_15:16	PARENT PAGE: 2 FILE: STAGE2 . 3
		PROJECT: D785C	PAGE: 12B

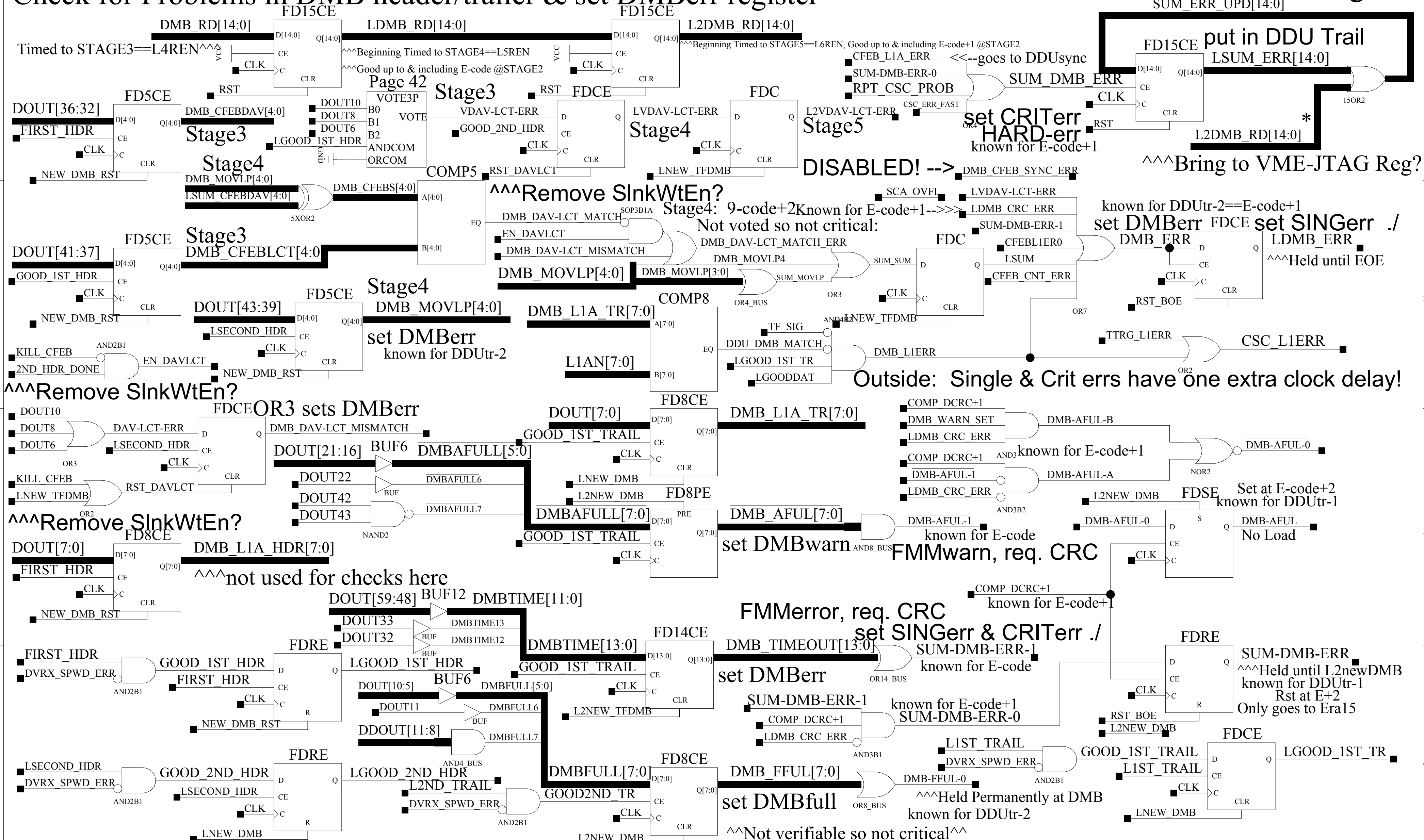

Need to deserialize b13 in 1st sample for *EACH CFEB* and compare to Hdr2d!
Encode to 3 bits + Phase (0), compare to Hdr2d[11-8], can be +/- 1?
Then what if 2 LCTs are set (overlap)? Encode the lowest bit or SKIP IT.
LWC = 25
ON for CFEB LWC = 2,3,5,6,8,9,11,12,14,15,17,18,20,21,23,24:
Set/Reset at LWC = 25 or LVB15
Recheck Later-->
May need a programmable offset...
only check L1A for 1st 2 samples^^^
DISABLED! -->
known for DDUtr-1
FDCE
SR8CE
FDPE
CB4CE
CB4CEBUS
FDRE
FD
FD4CEBUS
COMP4BUS
ADD4_BUS
LCT_SAMPLE_PHASE[0:7]
CFEB_LCT_SYNC[3:0]
CFEB_CNT[3:0]
DMB_LCT_SYNC[3:0]
DMB+1_SYNC[3:0]
DMB-1_SYNC[3:0]
DMB_CFEB_SYNCERR
DMB_CFEB_SYNC_ERR
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210
Stage 2 Logic: CFEB Status Decode
DDU Controller
CMS CSC Electronics
JRG
2
D785C
9-13-2006_16:38
STAGE2 . 4
12C



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: CFEB Count & DMB CRC Check DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 8-7-2008_15:16	FILE: STAGE2 . 5	PAGE: 12D

Check for Problems in DMB header/trailer & set DMBerr register

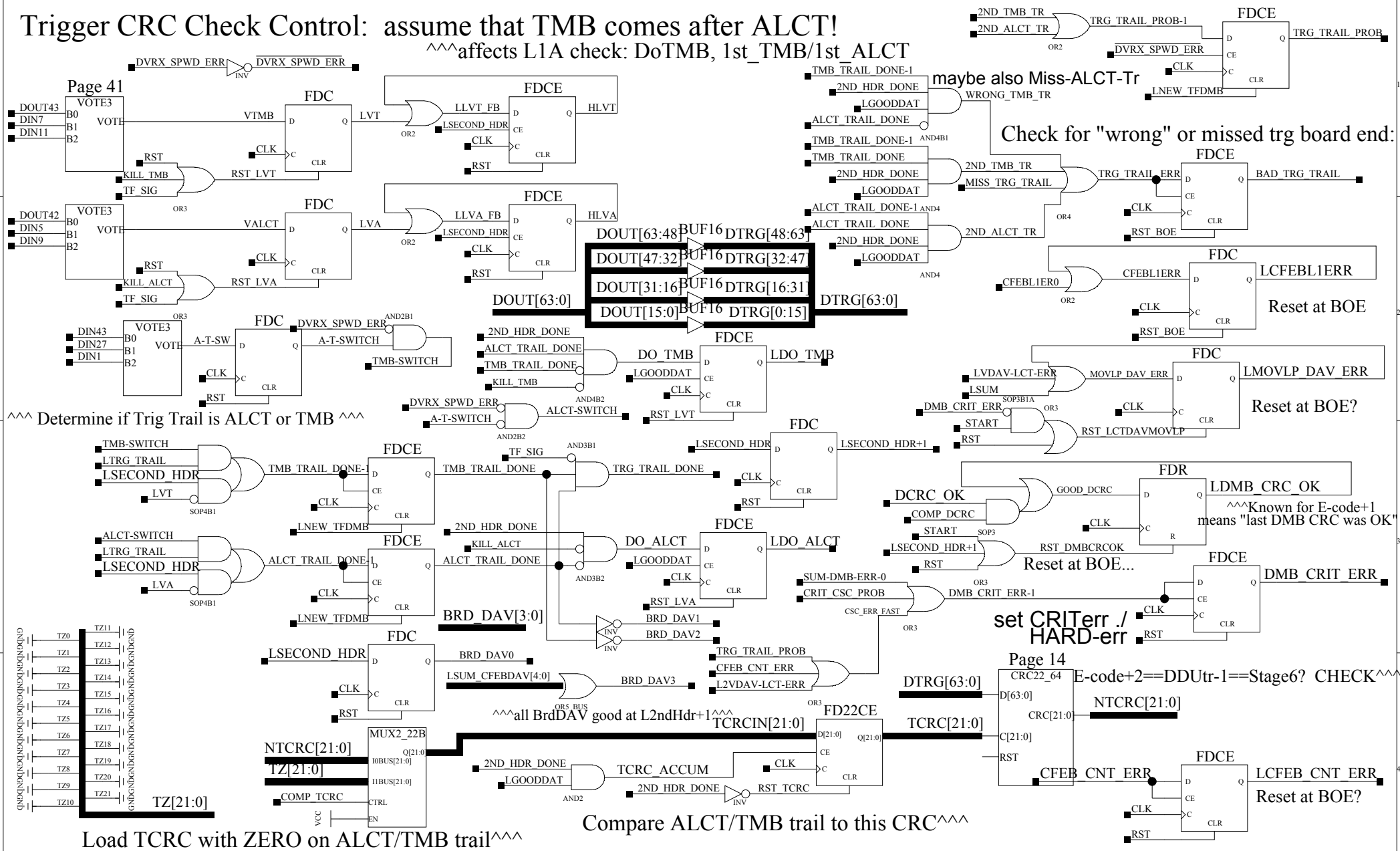
CSC "Reset Needed" register


SUM_ERR_UPD[14:0]
put in DDU Trail
LSUM_ERR[14:0]
FD15CE
DMB_RD[14:0]
LDMB_RD[14:0]
L2DMB_RD[14:0]
Timed to STAGE3==L4REN^^^
^^^Beginning Timed to STAGE4==L5REN
^^^Good up to & including E-code @STAGE2
^^^Beginning Timed to STAGE5==L6REN, Good up to & including E-code+1 @STAGE2
CFEB_L1A_ERR
<<--goes to DDUsync
SUM-DMB-ERR-0
SUM_DMB_ERR
RPT_CSC_PROB
CSC_ERR_FAST
set CRITerr
HARD-err
known for E-code+1
^^^Bring to VME-JTAG Reg?
Page 42
VOTE3P
Stage3
Stage4
Stage5
DOUT[36:32]
FIRST_HDR
FD5CE
DMB_CFEBDAV[4:0]
NEW_DMB_RST
VDAV-LCT-ERR
LVDAV-LCT-ERR
L2VDAV-LCT-ERR
GOOD_2ND_HDR
LGOOD_1ST_HDR
LNEW_TFDMB
DISABLED! --> DMB_CFEB_SYNC_ERR
DMB_MOVLP[4:0]
LSUM_CFEBDAV[4:0]
DMB_CFEBS[4:0]
COMP5
RST_DAVLCT
^^^Remove SlnkWtEn?
SCA_OVFL
LVDAV-LCT-ERR
LDMB_CRC_ERR
SUM-DMB-ERR-1
CFEBL1ER0
LSUM
CFEB_CNT_ERR
Stage4: 9-code+2 Known for E-code+1-->>>
Not voted so not critical:
known for DDUtr-2==E-code+1
set DMBerr
set SINGerr ./
DMB_ERR
LDMB_ERR
^^^Held until EOE
RST_BOE
DOUT[41:37]
GOOD_1ST_HDR
DMB_CFEBLCT[4:0]
DMB_DAV-LCT_MATCH
EN_DAVLCT
DMB_DAV-LCT_MISMATCH
DMB_DAV-LCT_MATCH_ERR
DMB_MOVLP4
DMB_MOVLP[3:0]
SUM_SUM
SUM_MOVLP
DOUT[43:39]
LSECOND_HDR
set DMBerr
known for DDUtr-2
DMB_L1A_TR[7:0]
COMP8
L1AN[7:0]
TF_SIG
DDU_DMB_MATCH
LGOOD_1ST_TR
LGOODDAT
DMB_L1ERR
TTRG_L1ERR
CSC_L1ERR
KILL_CFEB
2ND_HDR_DONE
Outside: Single & Crit errs have one extra clock delay!
^^^Remove SlnkWtEn?
OR3 sets DMBerr
DAV-LCT-ERR
DOUT[7:0]
FD8CE
DMB_L1A_TR[7:0]
GOOD_1ST_TRAIL
COMP_DCRC+1
DMB_WARN_SET
LDMB_CRC_ERR
DMB-AFUL-B
known for E-code+1
DMB-AFUL-0
DMB-AFUL-1
DMB-AFUL-A
DOUT[21:16]
BUF6
DMBAFULL[5:0]
DOUT22
DMBAFULL6
DOUT42
DOUT43
DMBAFULL7
LNEW_DMB
L2NEW_DMB
FD8PE
DMBAFULL[7:0]
DMB_AFUL[7:0]
set DMBwarn
known for E-code
FMMwarn, req. CRC
LNEW_TFDMB
^^^Remove SlnkWtEn?
Set at E-code+2
known for DDUtr-1
FDSE
DMB-AFUL
No Load
DMB_L1A_HDR[7:0]
^^^not used for checks here
DOUT[59:48]
BUF12
DMBTIME[11:0]
DOUT33
DOUT32
DMBTIME13
DMBTIME12
DMBTIME[13:0]
FD14CE
DMB_TIMEOUT[13:0]
FMMerror, req. CRC
set SINGerr & CRITerr ./
SUM-DMB-ERR-1
known for E-code
set DMBerr
known for E-code+1
FDRE
SUM-DMB-ERR
^^^Held until L2newDMB
known for DDUtr-1
Rst at E+2
Only goes to Era15
DVRX_SPWD_ERR
DOUT[10:5]
DMBFULL[5:0]
DOUT11
DMBFULL6
DDOUT[11:8]
DMBFULL7
L2NEW_TFDMB
SUM-DMB-ERR-0
L1ST_TRAIL
LGOOD_1ST_TR
GOOD_2ND_HDR
LGOOD_2ND_HDR
L2ND_TRAIL
GOOD2ND_TR
DMBFULL[7:0]
DMB_FFUL[7:0]
DMB-FFUL-0
set DMBfull
^^^Held Permanently at DMB
known for DDUtr-2
^^Not verifiable so not critical^^
L2NEW_DMB

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Stage 2 Logic: DMB Status Checks DDU Controller CMS CSC Electronics	BY JRG	PARENT PAGE 2	PROJECT D785C	
		DATE 8-12-2008_17:20		FILE STAGE2 . 6	PAGE 12E

Trigger CRC Check Control: assume that TMB comes after ALCT!

^^^affects L1A check: DoTMB, 1st_TMB/1st_ALCT

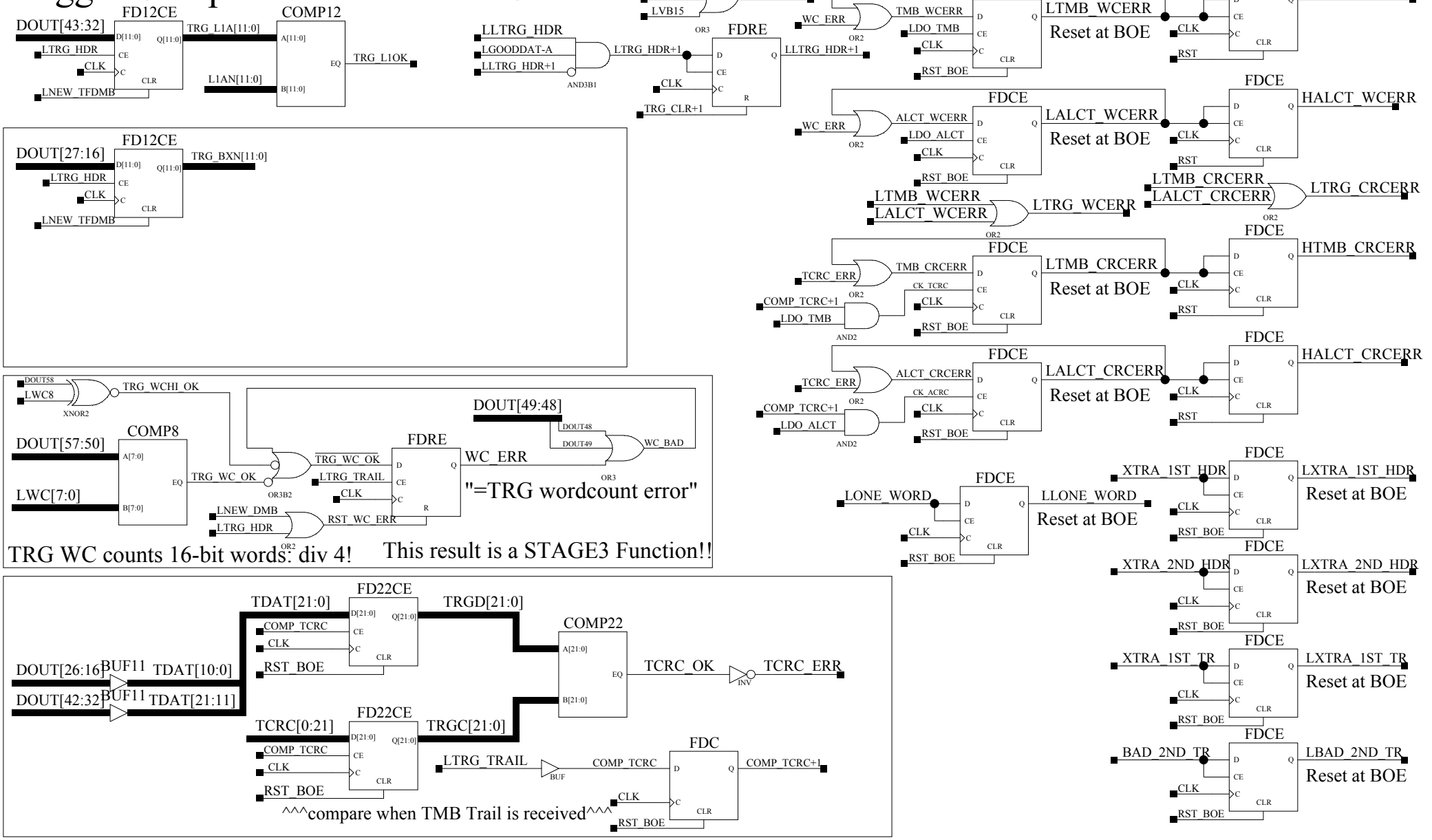


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Stage 2 Logic: Trigger Board Flags
DDU Controller
CMS CSC Electronics

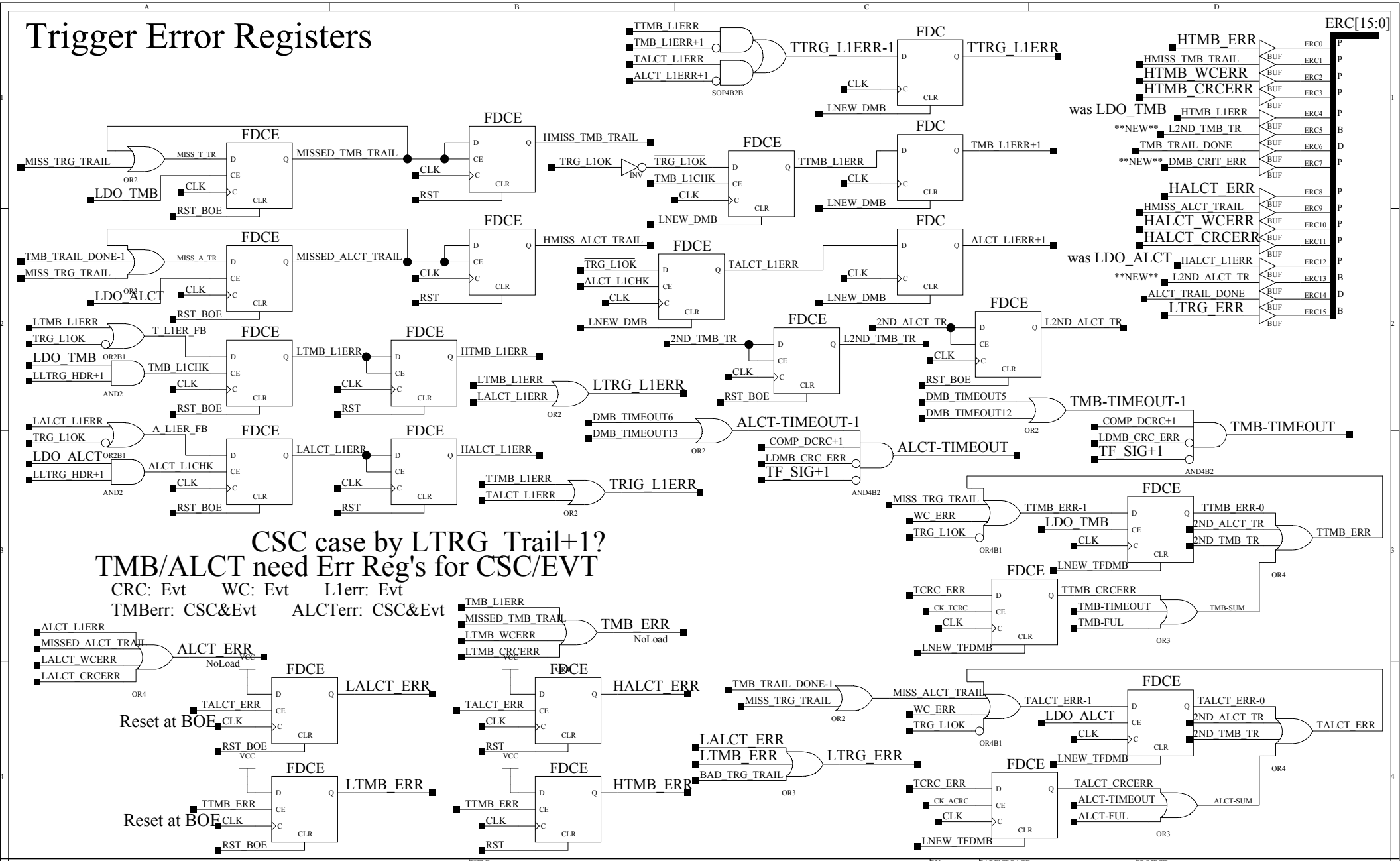
BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
8-12-2008_17:18	STAGE2 . 7	12F

Trigger Comparisons and Error Checks

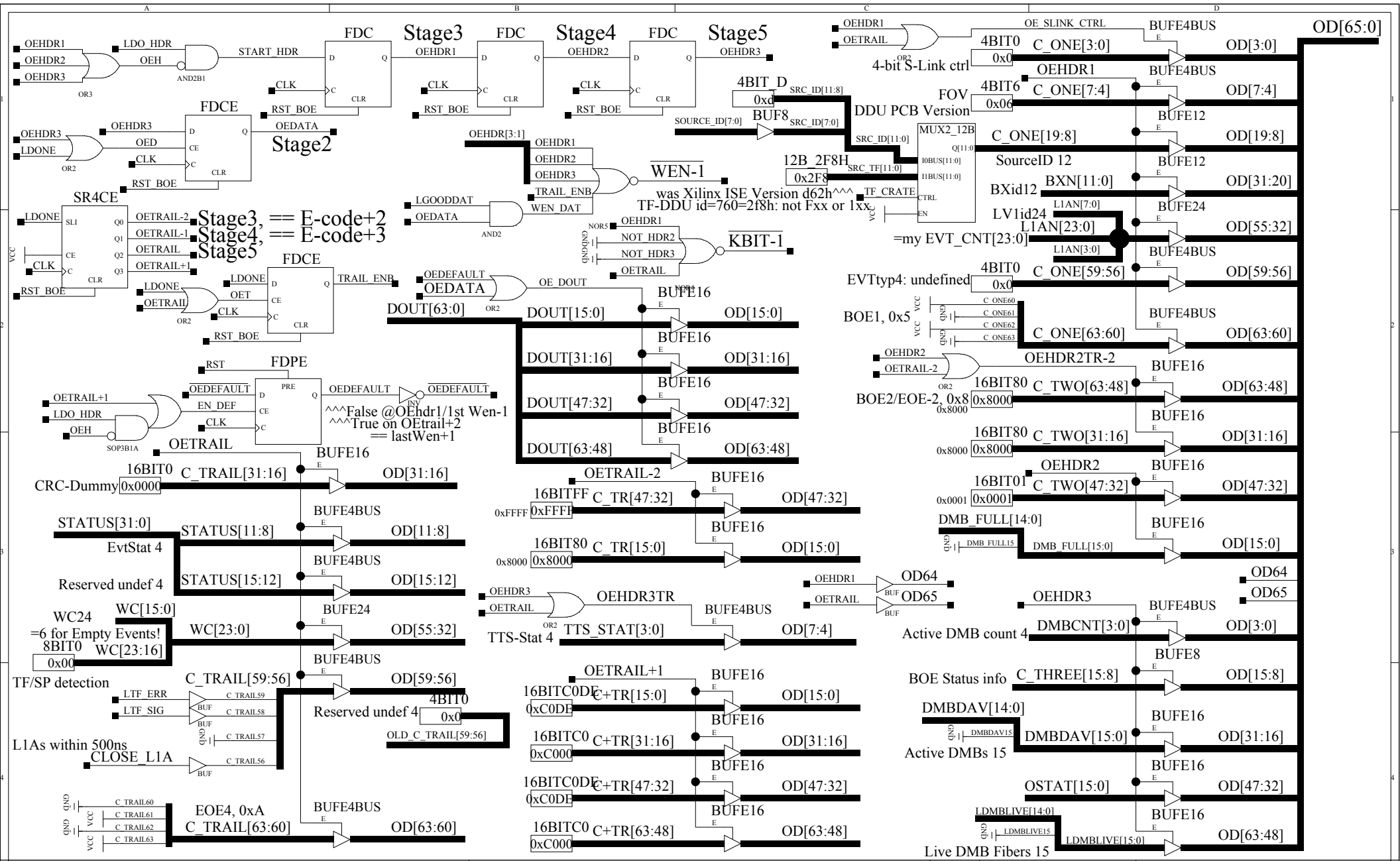


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: Trigger Error Checks DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 10-3-2007_15:07	FILE: STAGE2 . 8	PAGE: 12G

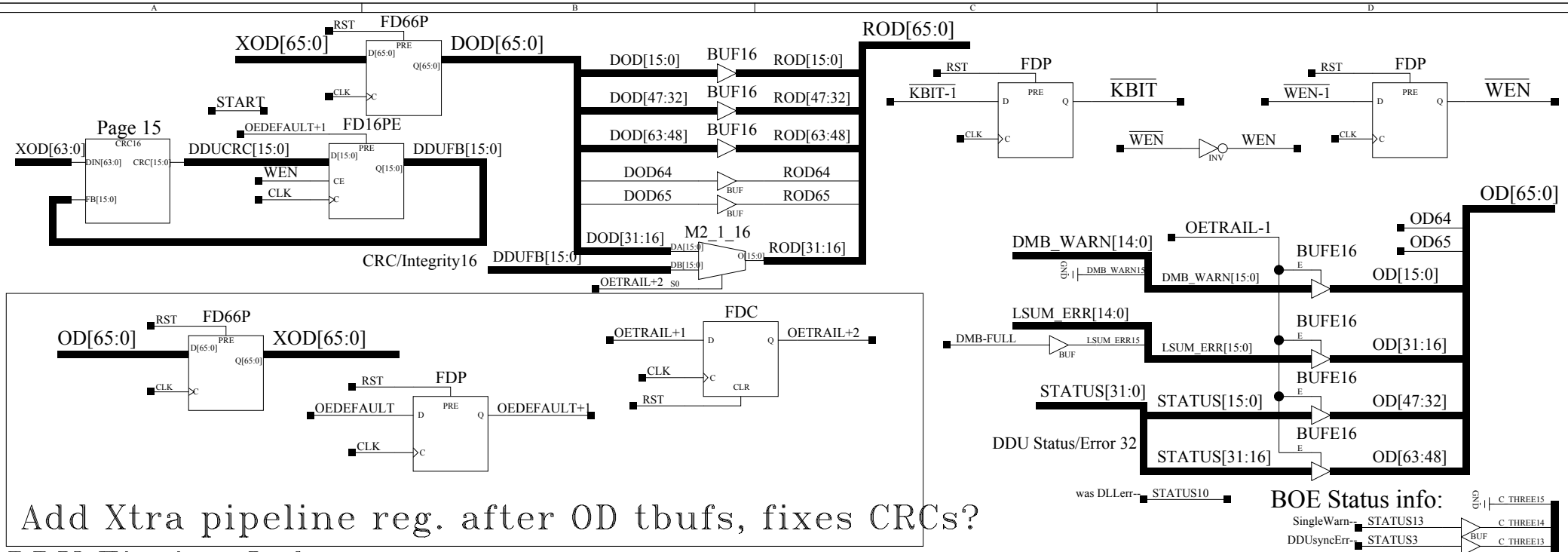
Trigger Error Registers



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: Trigger Error Registers DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 2	PROJECT: D785C
		DATE: 8-12-2008_15:27	FILE: STAGE2 . 9	PAGE: 12H



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Stage 2 Logic: DDU Header/Trailer Control DDU Controller CMS CSC Electronics	BY: JRG DATE: 8-14-2008_16:22	PARENT PAGE: 2 FILE: STAGE2 . 10	PROJECT: D785C PAGE: 12I



Add Xtra pipeline reg. after OD tbufs, fixes CRCs?

DDU Timing Info

DDUctrl to InFIFO signals: 2" – 4", .3ns – .6ns

IRCLK has 4 loads, may slow signal by 0.1–0.5ns?

CKFBout has normal drive, IRCLK has ~1.1ns Faster drive

FPGA I/O Delays (lvcmos33, ns)

IBUF: 0.92

IFD set/hold: 0.92/–0.12 Clk to Q: 0.65

OBUF: 2.33

OFD set/hold: 0.26/0.14 Clk to Q: 2.41

*modifiers for drive/slew settings:

6mA: add 2.60 for Slow, 1.28 for Fast
8mA: add 1.69 for Slow, 0.46 for Fast
12mA: add 1.18 for Slow, 0.26 for Fast
16mA: add 0.52 for Slow, 0.02 for Fast
24mA: +0.44 for Slow, –0.08 for Fast

FPGA CLB Delays (ns)

4–FG: 0.32 5–FG: 0.65

FD set/hold: 0/0.14 Clk to Q: 0.38

Sync. set–rst setup: 0.60

Async. pre–clr to Q: 1.25

SR16 Clk to Q: 3.12

SR32 Clk to Q: 3.49

SI set/hold: 0.34/0.0

TI FIFO I/O Delays (ns)

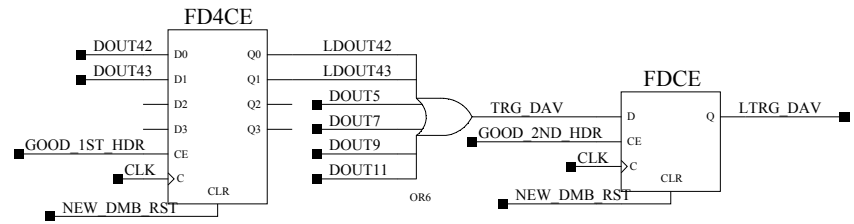
Measured on FIFO test board

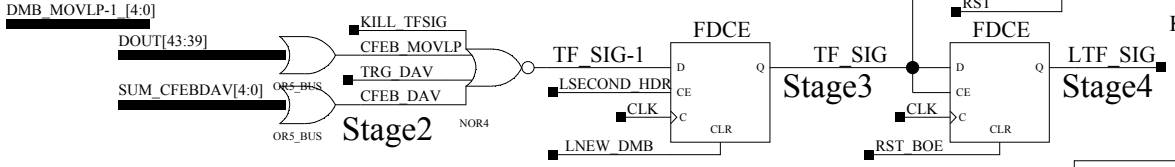
	Vcc: 3.38V	3.04V
RCLK to Empty (low state)		
Max: 3.6, Min: 2.5	3.02–3.18	3.20–3.29
to Not Empty (high state)	3.22–3.34	3.23–3.31
RCLK to Q11 False (low state)		
Max: 4.3, Min: 2.5	3.32–3.62	3.40–3.64
to Q11 True (high state)	3.31–3.87	3.51–4.06

to Q11 (low state) 3.22–3.34 3.28

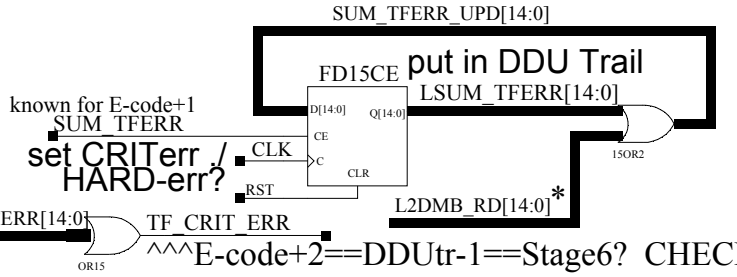
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU CRC Logic for SLINK/C.D.F. Compatibility DDU Controller CMS CSC Electronics	BY: JRG PARENT PAGE: 2 DATE: 5-15-2009_13:47	PROJECT: D785C FILE: STAGE2 . 11 PAGE: 12J

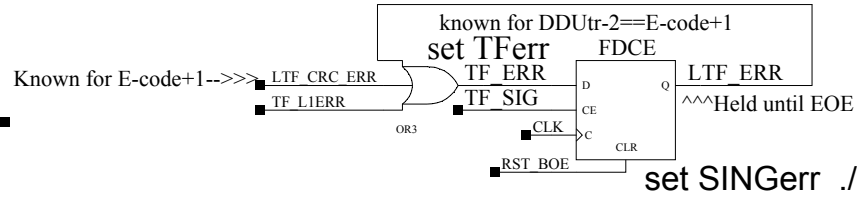
Check for Track Finder signal, record TF errors

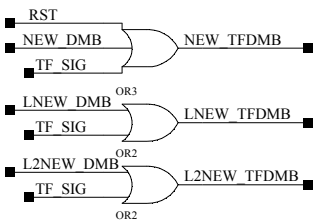


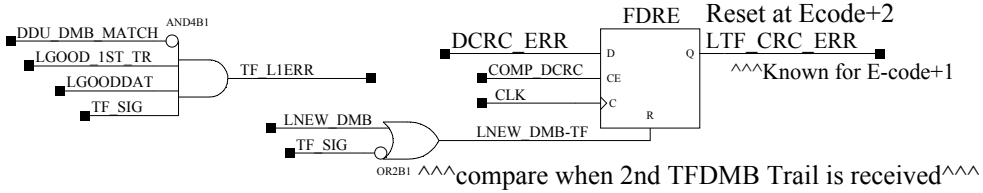


END

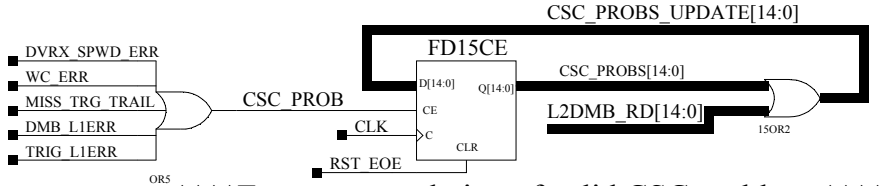


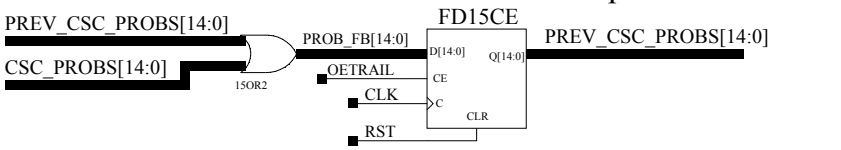


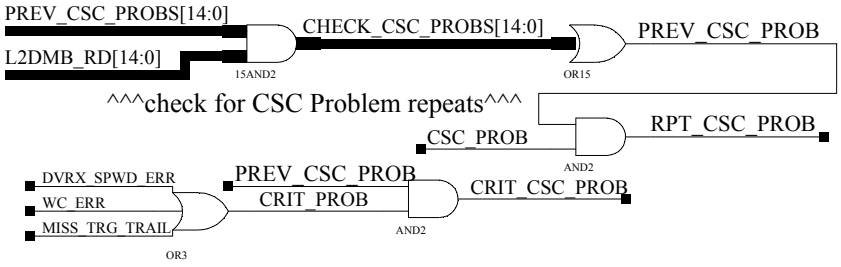




CSC Problem Repeat checking



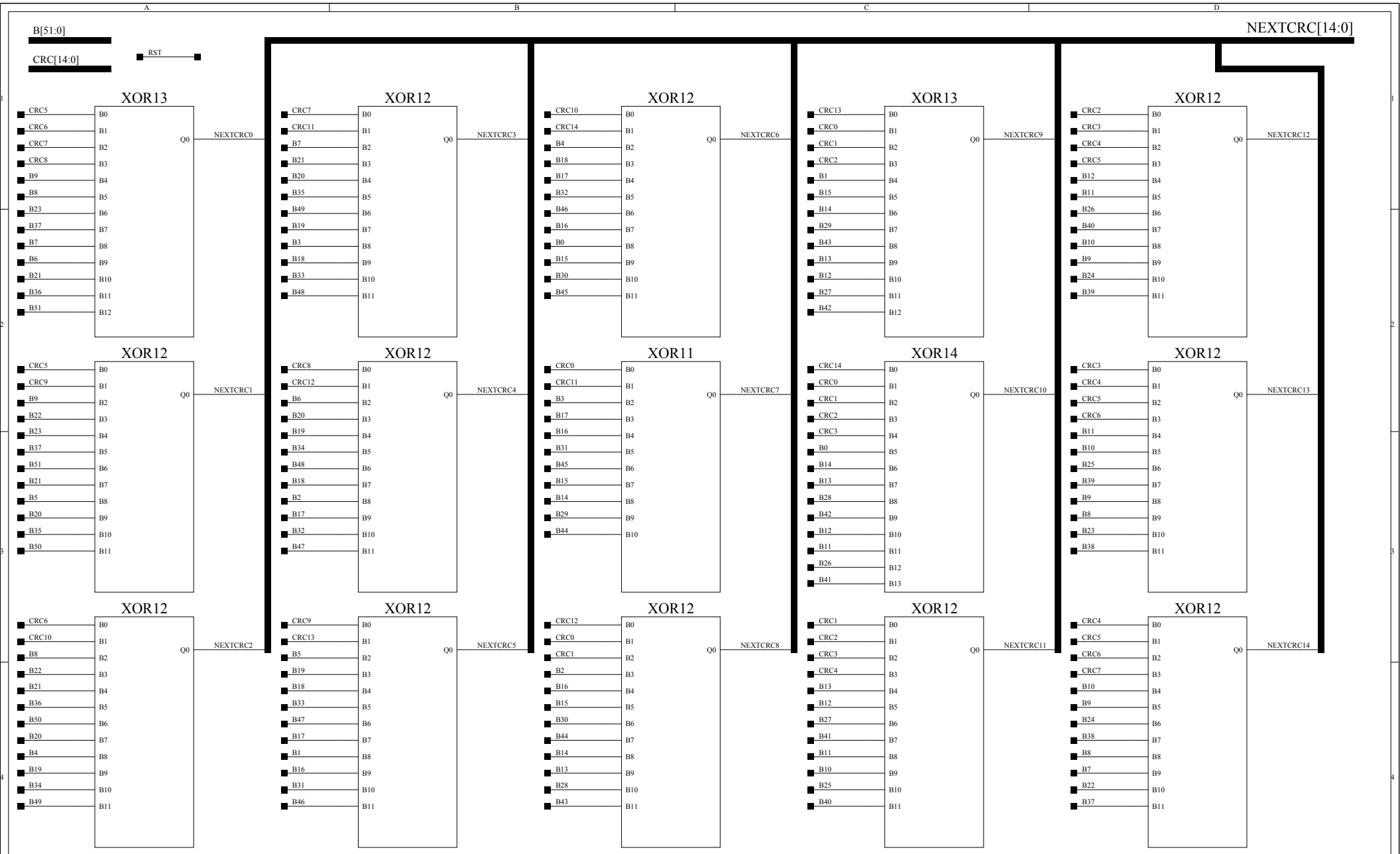




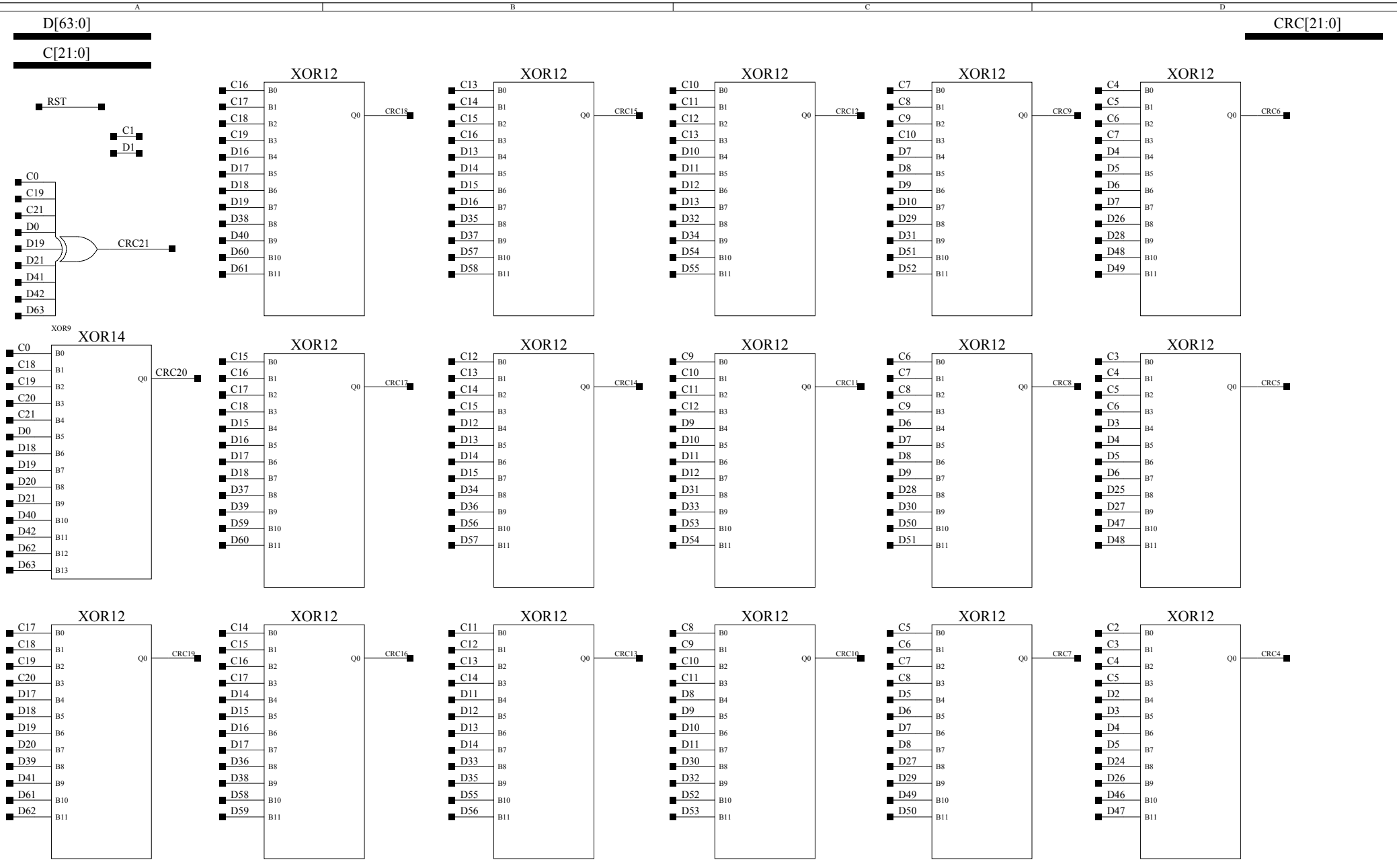
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Stage 2 Logic: DMB Status Checks
DDU Controller
CMS CSC Electronics

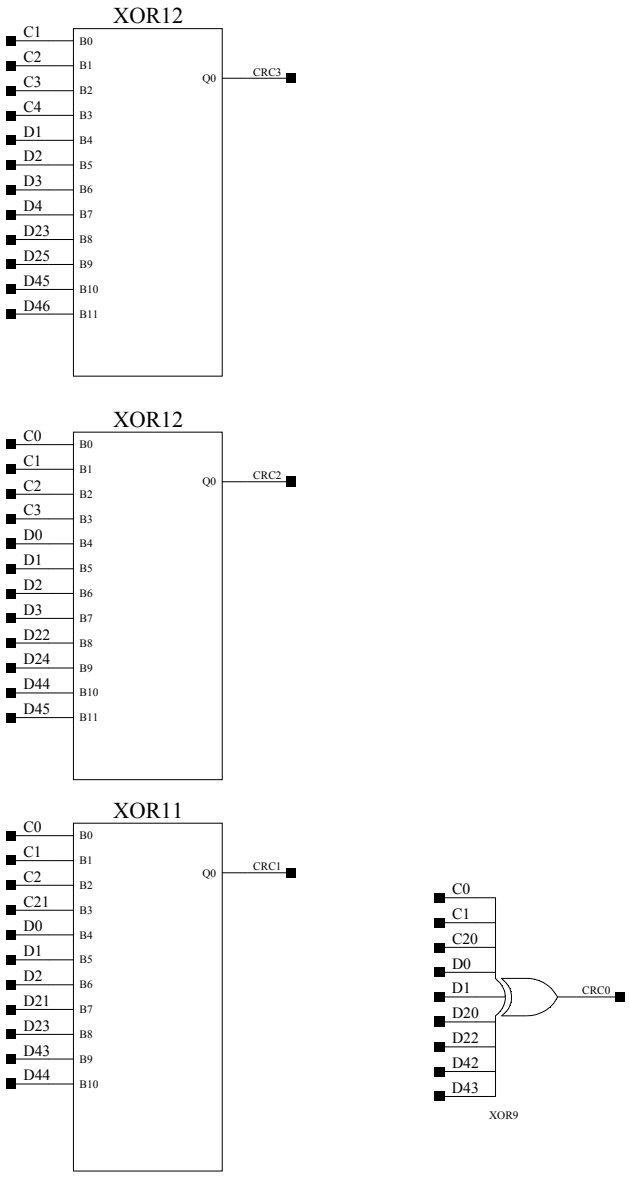
BY	PARENT PAGE	PROJECT
JRG	2	D785C
DATE	FILE	PAGE
8-12-2008_17:18	STAGE2 . 12	12K



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC15, 52-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_11:33	PARENT PAGE: 12B	PROJECT: D785C FILE: CRC15_52 . 1 PAGE: 13

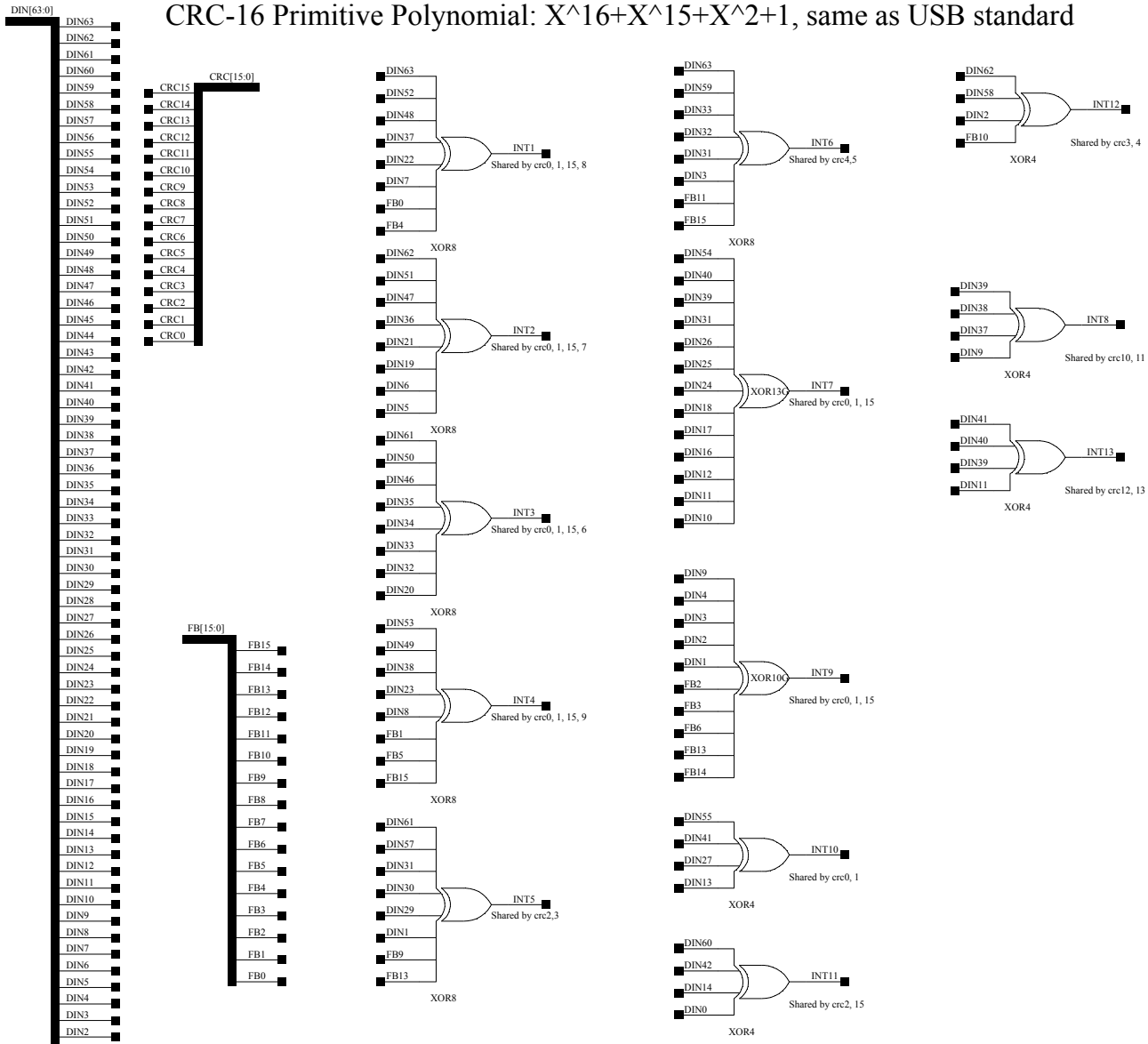


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC22, 64-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 12C	PROJECT: D785C	
		DATE: 1-26-2005_11:33		FILE: CRC22_64 . 1	PAGE: 14

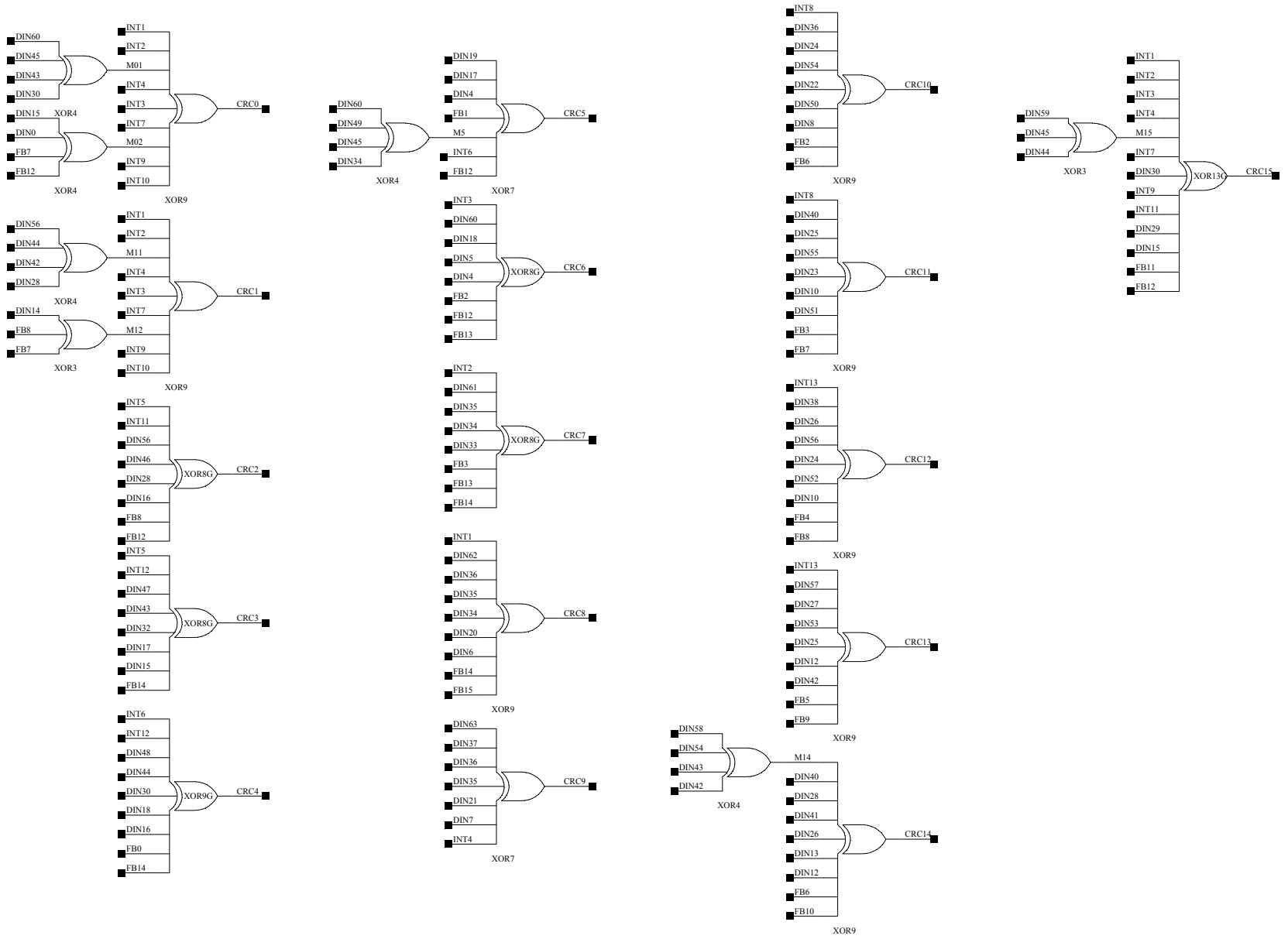


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CRC22, 64-bit wide data equations DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 12C	PROJECT: D785C
		DATE: 1-26-2005_11:34	FILE: CRC22_64 . 2	PAGE: 14A

CRC-16 Primitive Polynomial: X^16+X^15+X^2+1, same as USB standard



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	SLINK CRC16 Calculation, common components DDU Slink Interface FPGA CMS CSC Electronics	BY GU	PARENT PAGE 12F	PROJECT D785C
			DATE 2-7-2005_17:50	FILE CRC16 . 1	PAGE 15

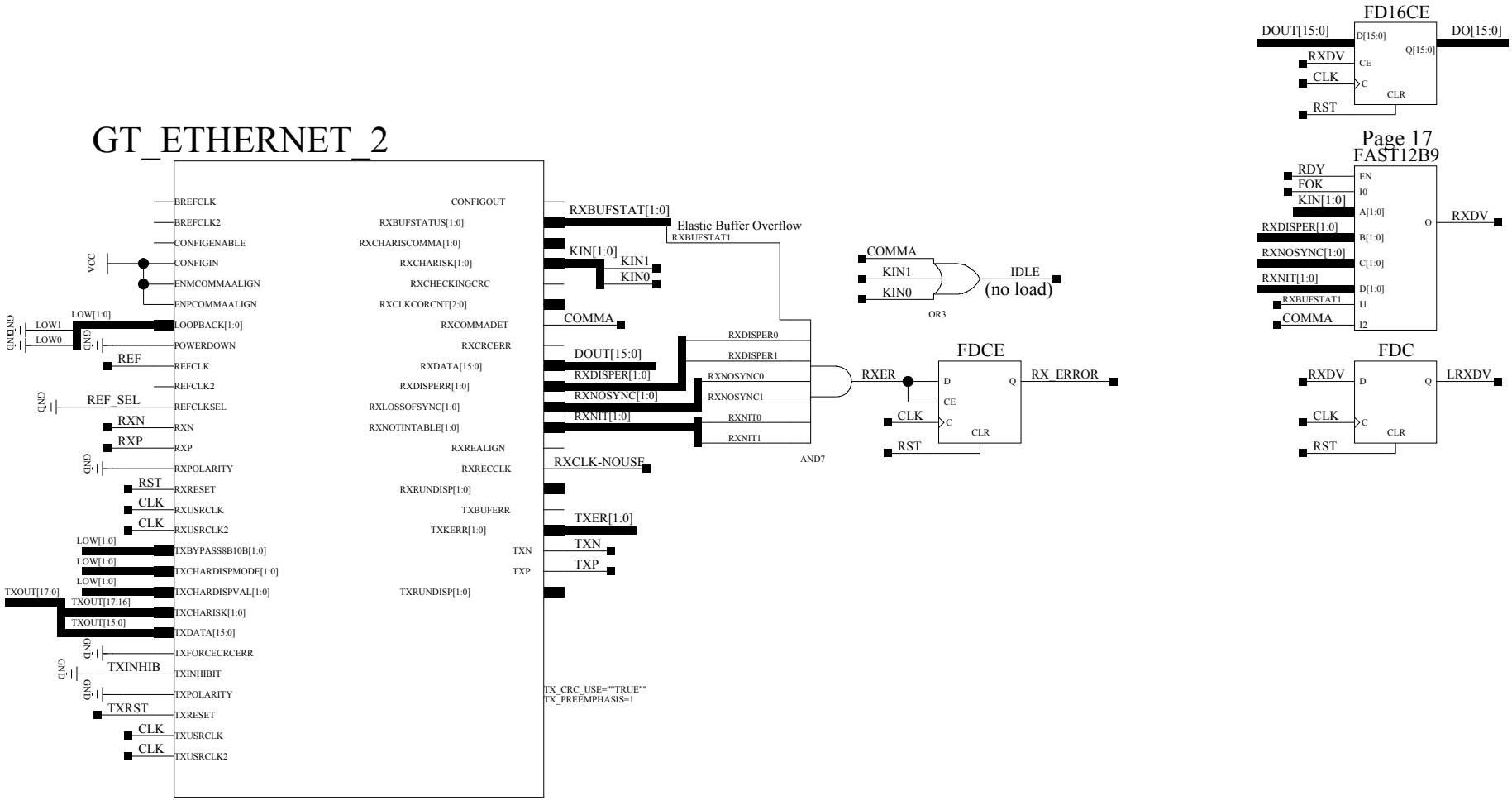


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

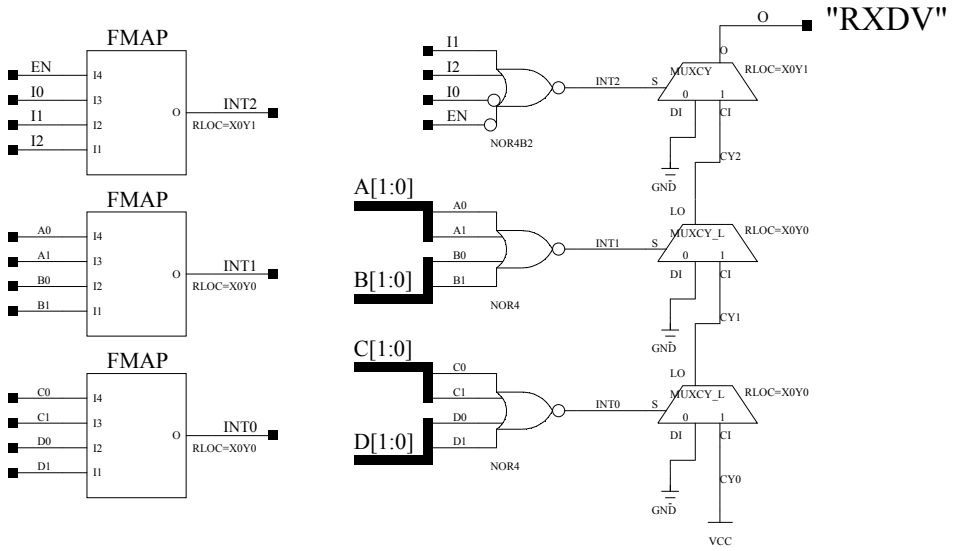
TITLE: SLINK CRC16 Calculation
DDU Slink Interface FPGA
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
GU	12F	D785C
DATE		FILE / PAGE
2-7-2005_17:50		CRC16 . 2 / 15A

Outgoing packets must have 1010... preamble logic and End Packet logic.
Incoming packets must also exclude Preamble and CRC in RxDV logic.
---> Not done yet! Consider a counter to skip 1st ~12 bytes after K word. Skip 4 CRC bytes too.

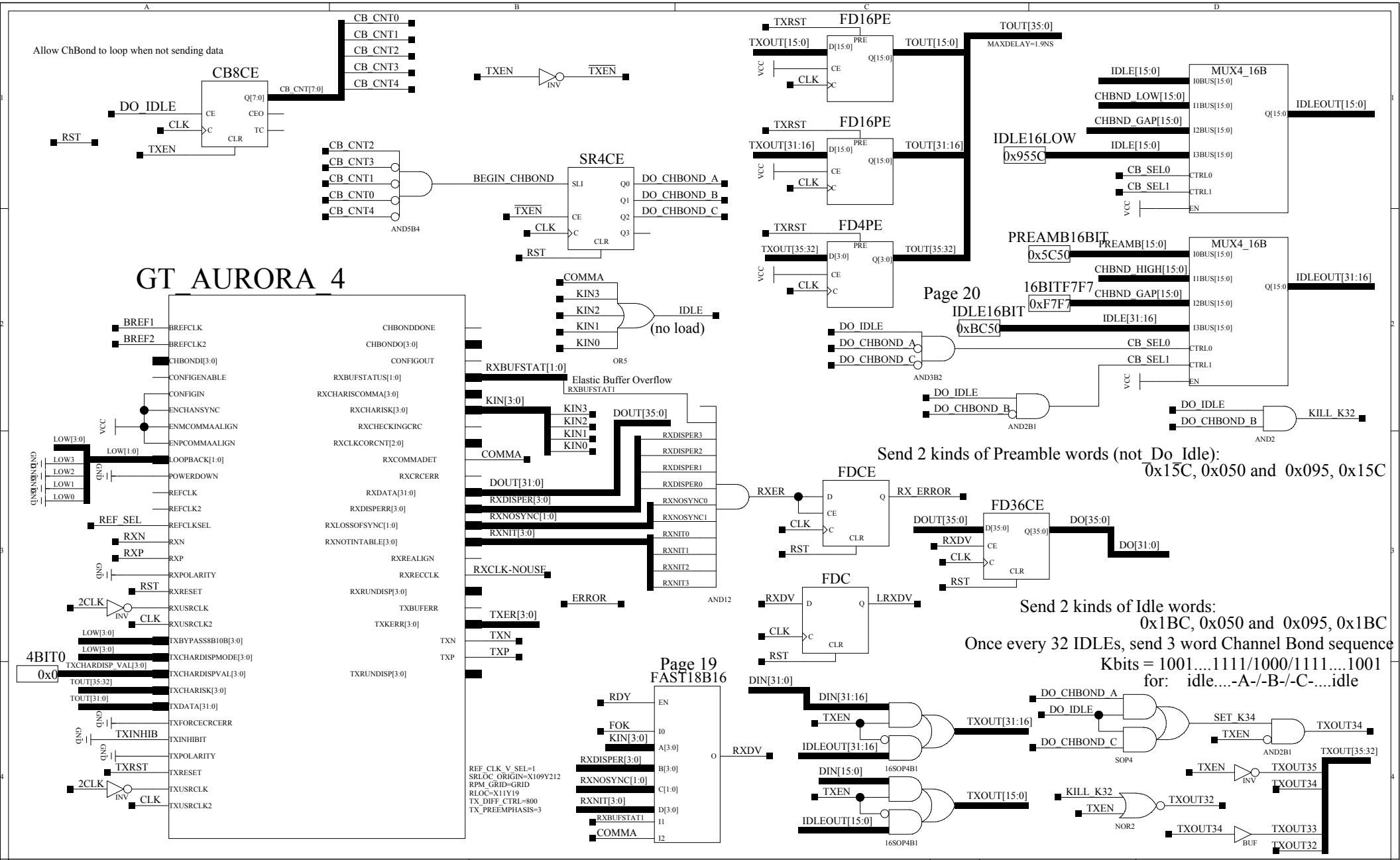


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Gigabit Ethernet Tranceiver DDU Controller Logic CMS CSC Electronics	BY: JRG DATE: 7-18-2005_16:14	PARENT PAGE: 2E FILE: OUT_GBE . 1
		PROJECT: D785C	PAGE: 16

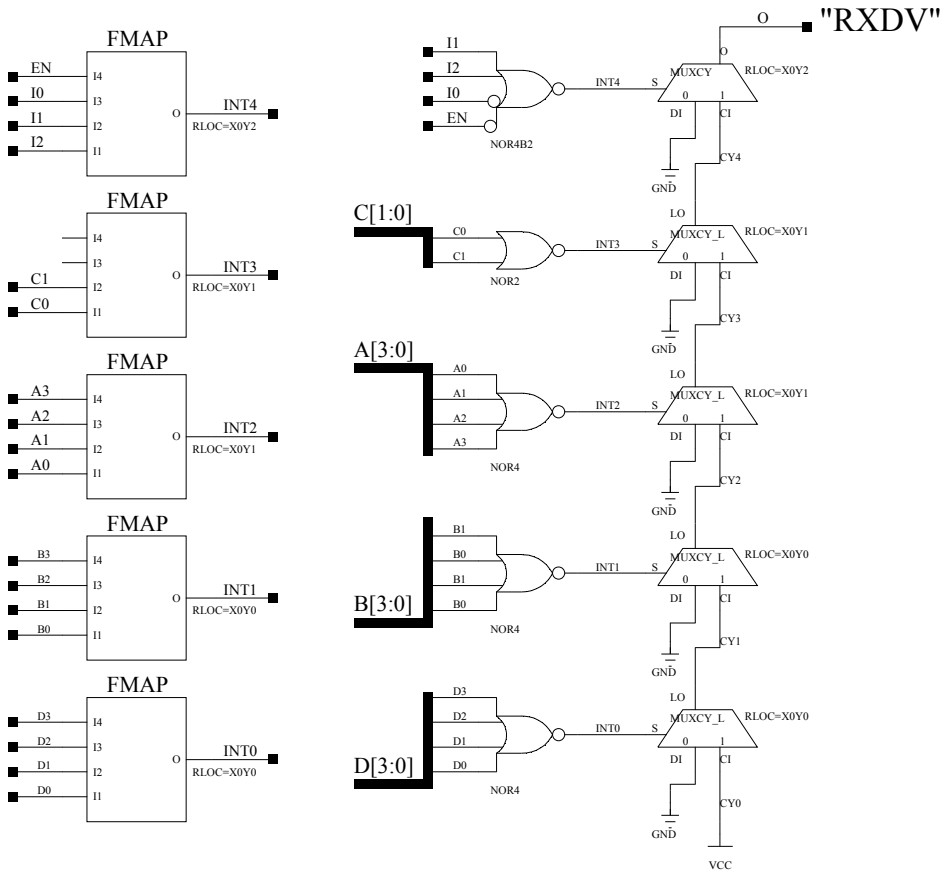


XILINX JRG

Title:	FAST12B9		
Comments:	Custom Logic for DDU similar to: AND12B9		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE Multi Gigabit Tranceiver DDU Controller Logic CMS CSC Electronics	BY JRG	PARENT PAGE 2E	PROJECT D785C	
		DATE 3-22-2012_15:32		FILE OUT_UNIT . 1	PAGE 18



XILINX

JRG

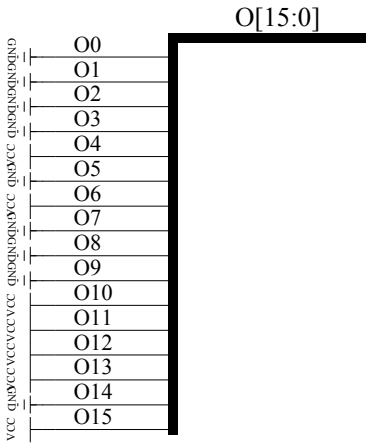
Title:	FAST13B10		
Comments:	Custom Logic for DDU similar to: AND12B10 with an OR2 (allows ON to override)		
Date:	19th December 2003	Ver:	1
Sheet Size: B		Rev:	A

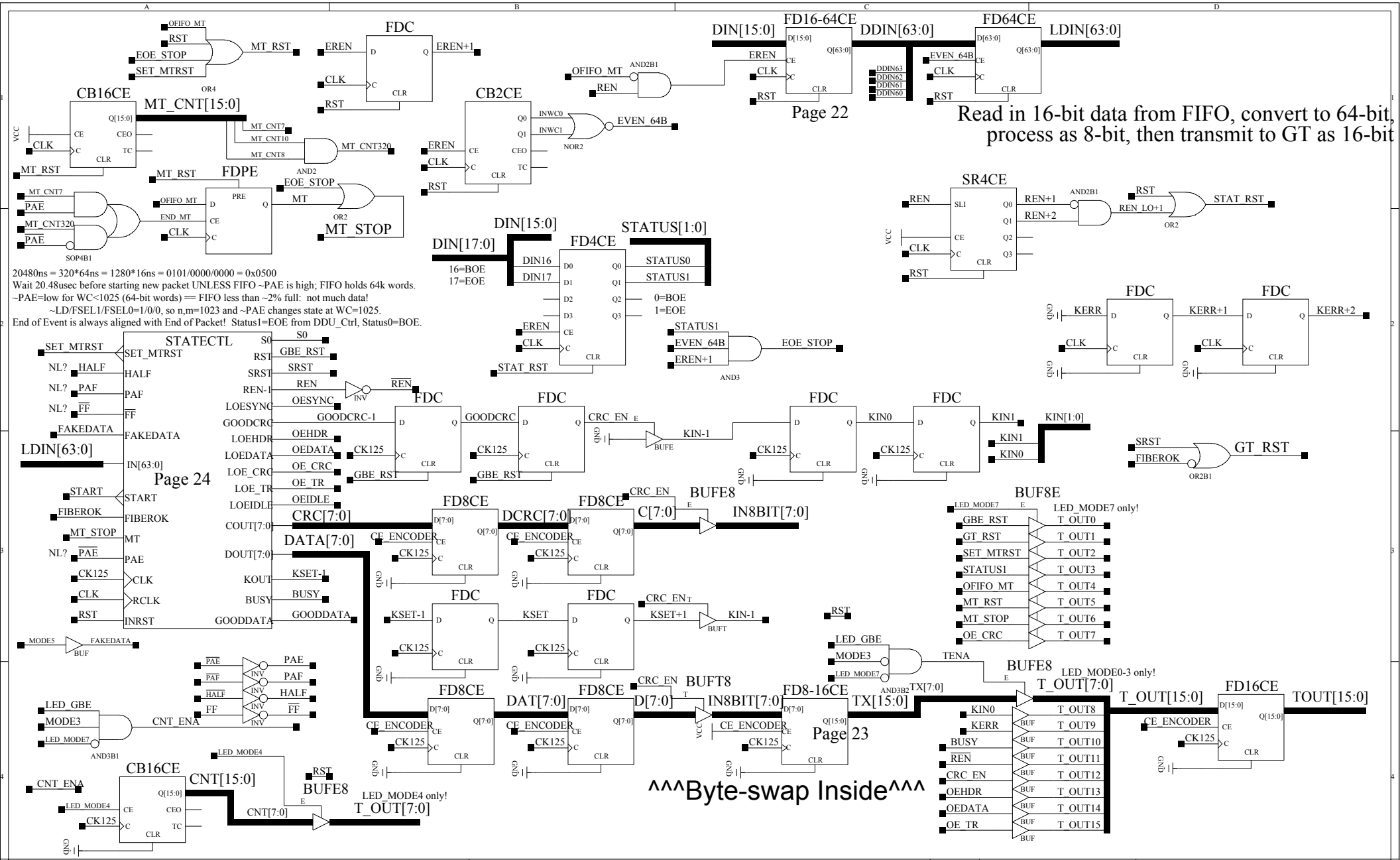
Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)

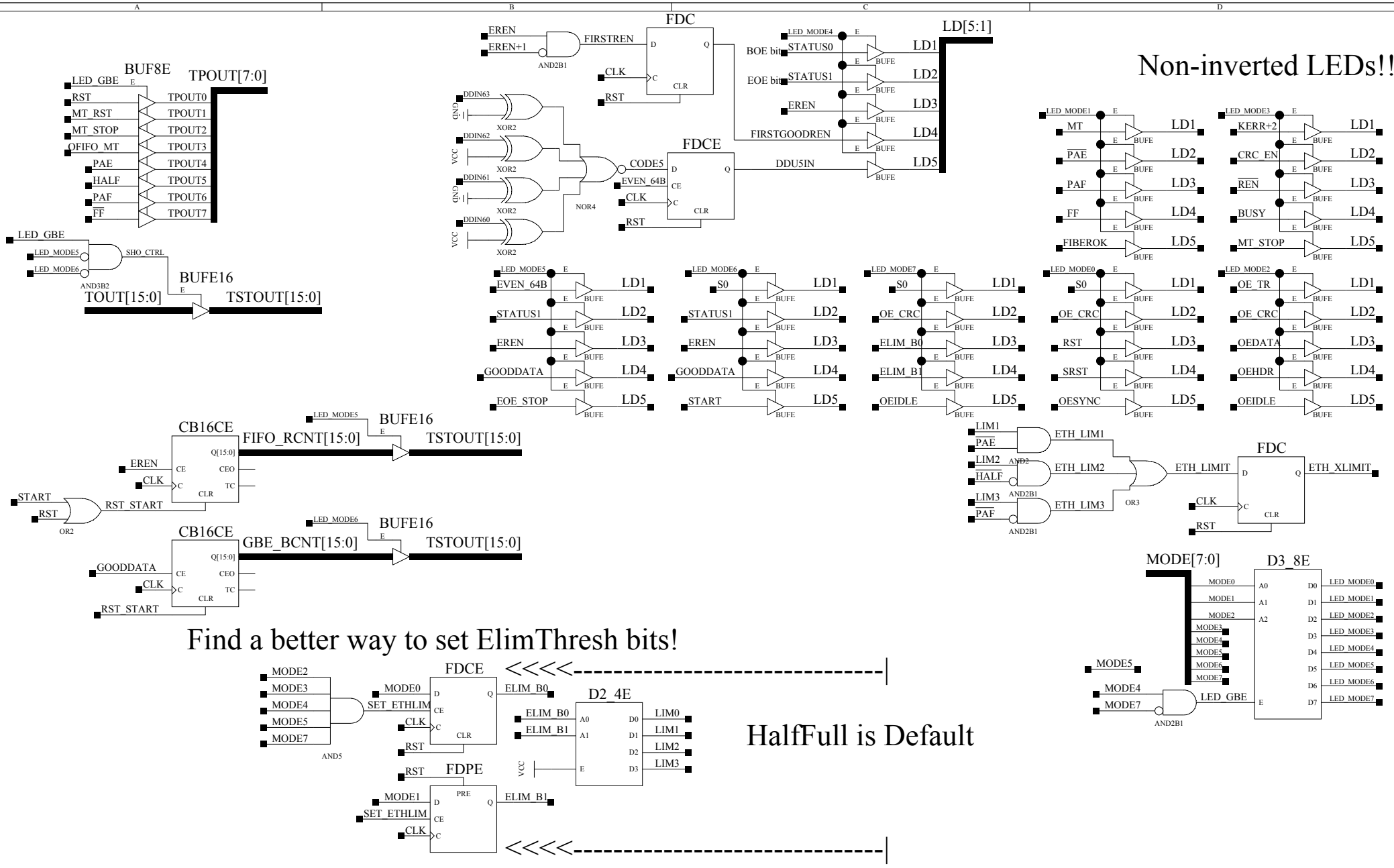
= 0x1BC + 0x050 (time-ordered)

= 0xBC50 (in parallel)

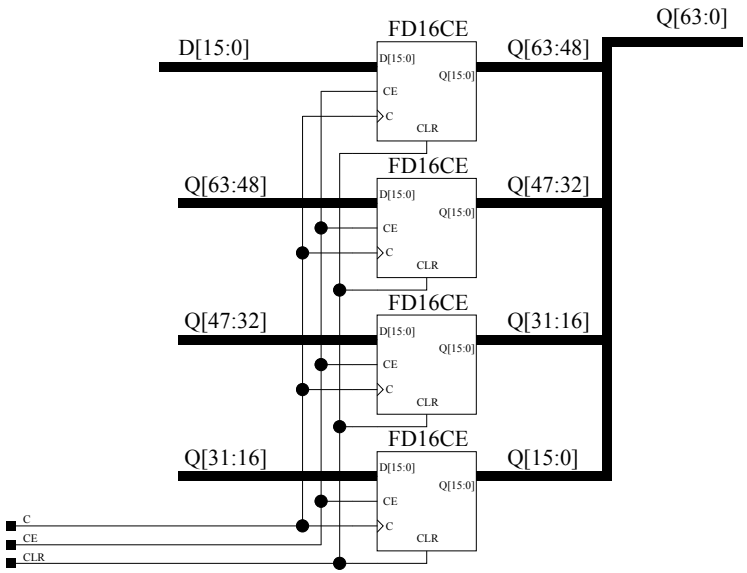




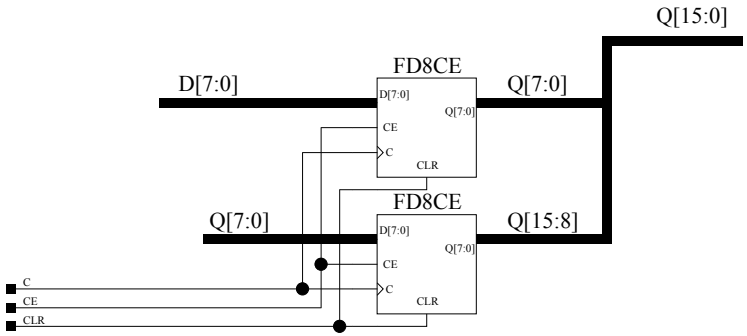
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Ethernet Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2F	PROJECT: D785C	
		DATE: 12-8-2006_14:29		FILE: ETHCNTRL . 1	PAGE: 21



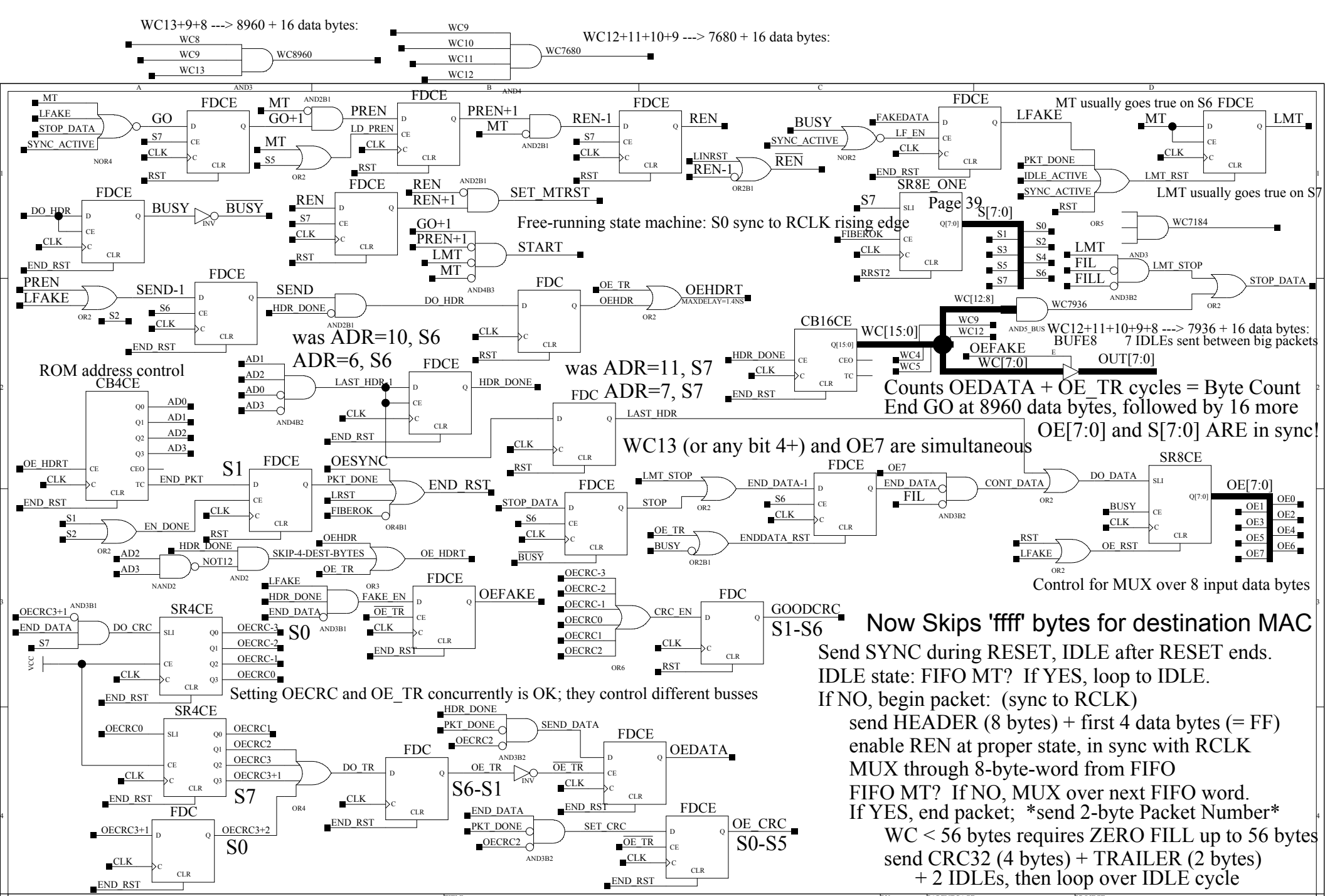
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Ethernet Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG	PARENT PAGE: 2F	PROJECT: D785C	
		DATE: 12-8-2006_14:29		FILE: ETHCNTRL . 2	PAGE: 21A



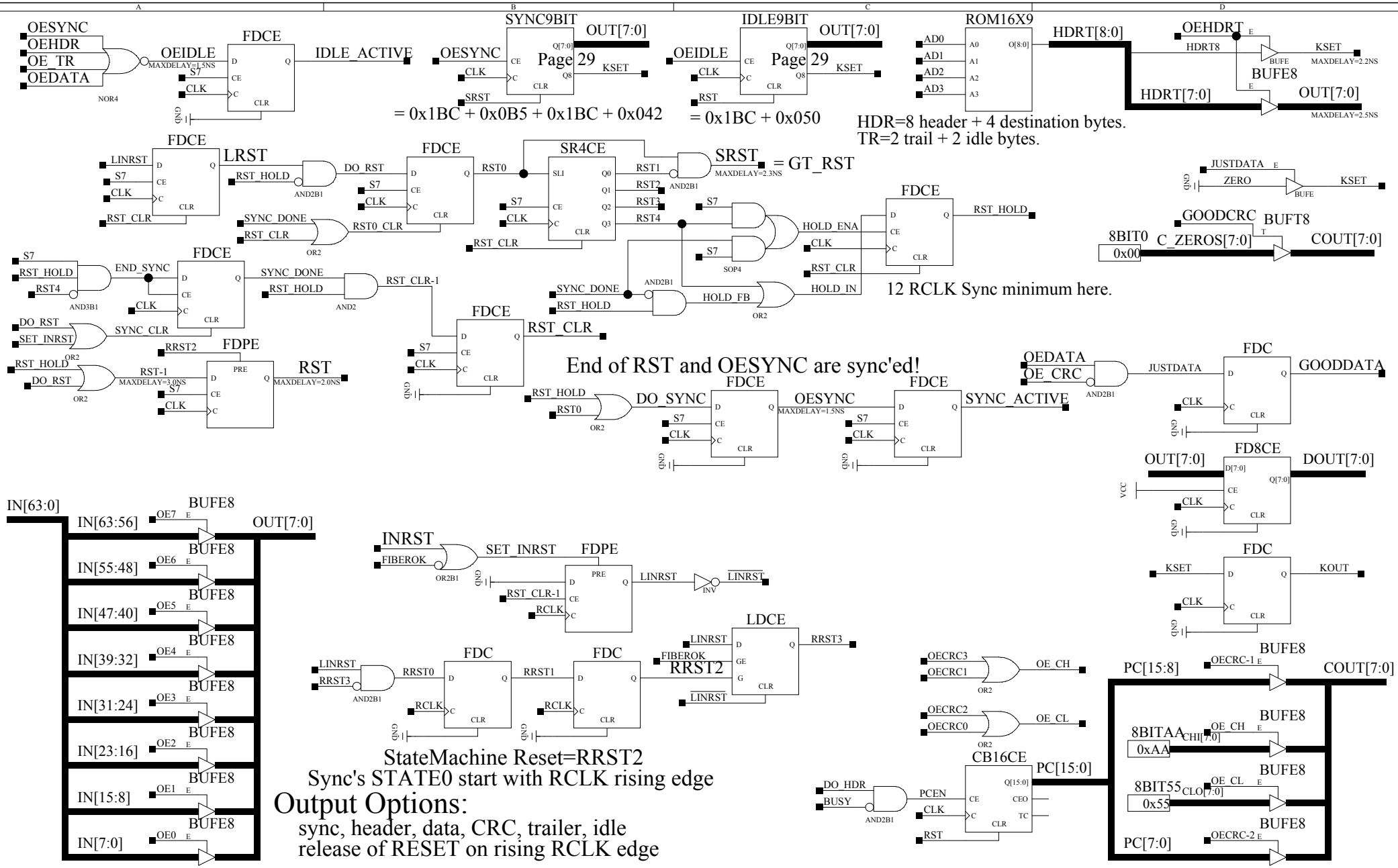
XILINX	JRG
Title: VIRTEX Family FD16-64CE Macro	
Comments: 64-Bit Bus Matching Register with Asynchronus Clear and Chip Enable	
Date: 2nd February 2004	Ver: 1
Sheet Size: B	Rev: A



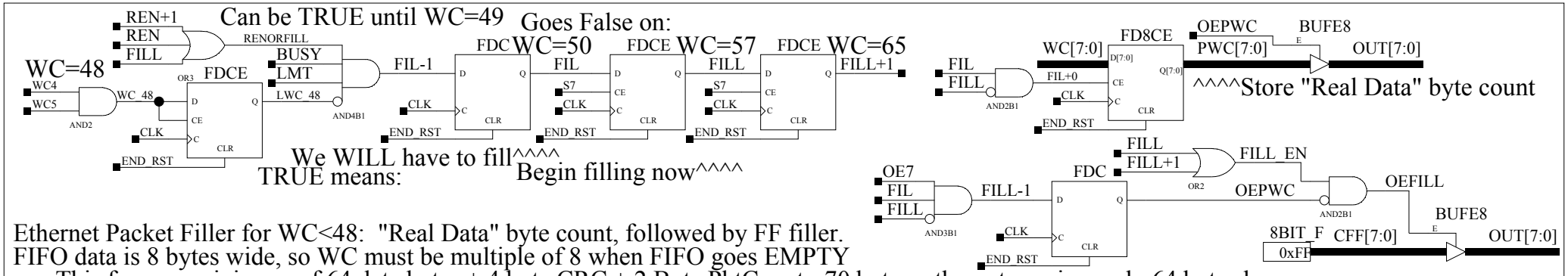
XILINX		JRG	
Title:	VIRTEX Family FD8-16CE Macro		
Comments:	8-16-Bit Bus Matching Register with Asynchronus Clear and Chip Enable		
Date:	4th February 2004	Ver:	1
Sheet Size: B		Rev:	A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 7-29-2005_13:26	PARENT PAGE: 21A FILE: STATECTL . 1
		PROJECT: D785C	PAGE: 24



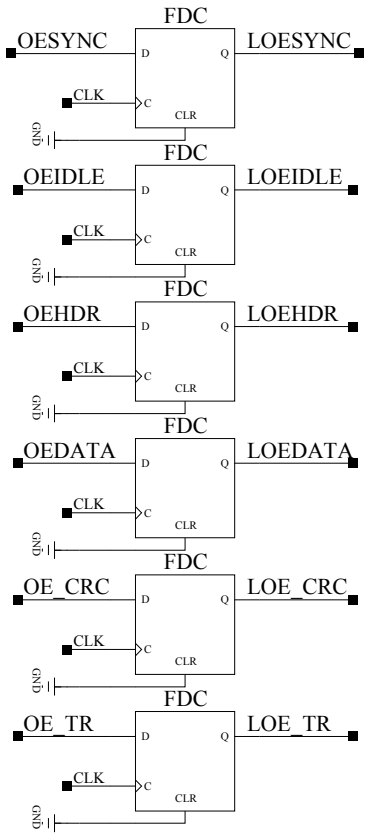
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: State Machine Control DDU Ethernet Logic CMS CSC Electronics	BY: JRG DATE: 7-18-2005_16:19	PARENT PAGE: 21A FILE: STATECTL . 2
		PROJECT: D785C	PAGE: 24A



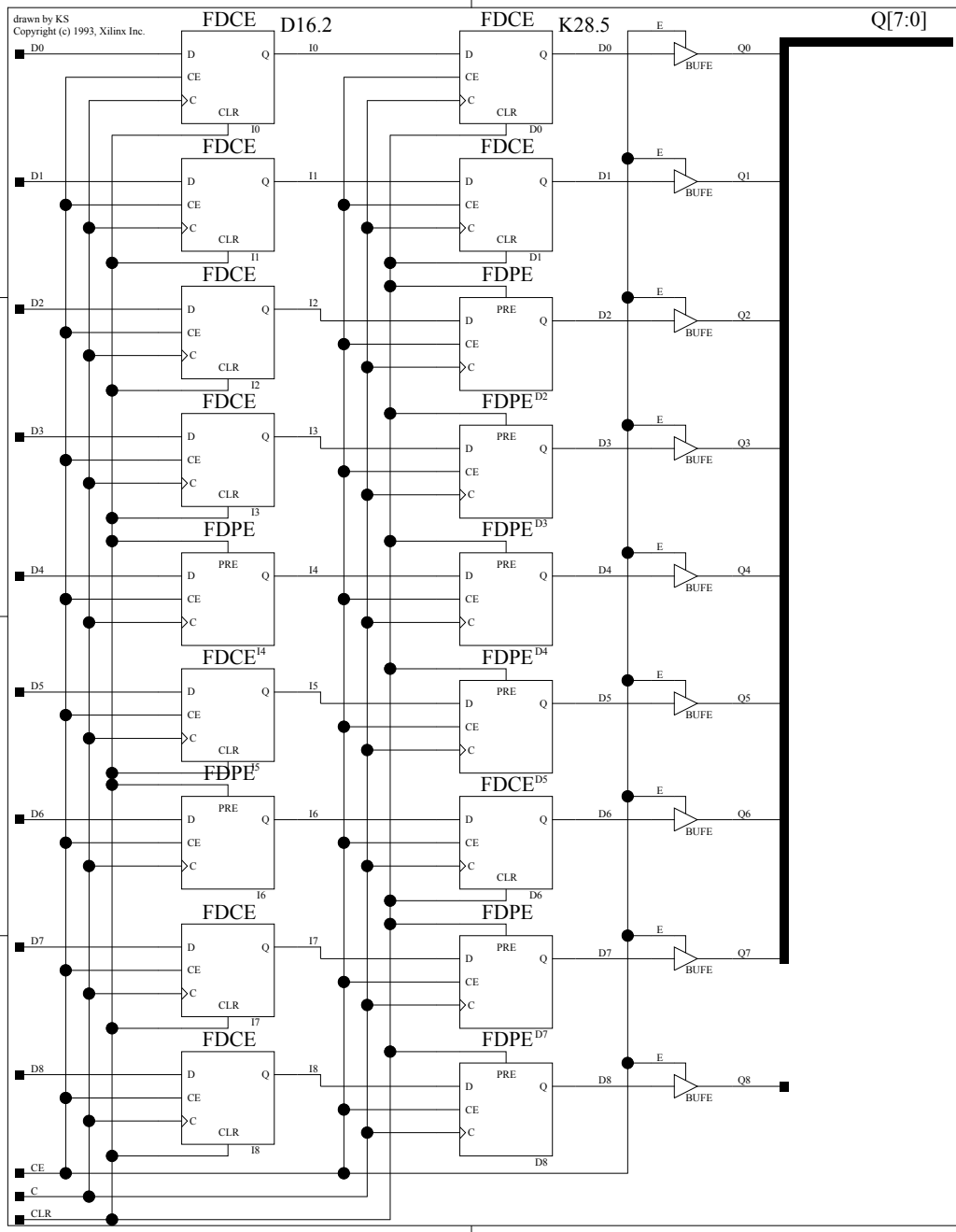
Ethernet Packet Filler for WC<48: "Real Data" byte count, followed by FF filler.
FIFO data is 8 bytes wide, so WC must be multiple of 8 when FIFO goes EMPTY
This forces a minimum of 64 data bytes + 4 byte CRC + 2 Byte PktCount= 70 bytes; ethernet requires only 64 bytes here.
Overfill ensures at least 15 FF bytes (after the "Real Data" byte count) in a "filled" packet.

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE	State Machine Control DDU Ethernet Logic CMS CSC Electronics
BY	JRG
PARENT PAGE	21A
PROJECT	D785C
DATE	1-26-2005_11:50
FILE	STATECTL . 3
PAGE	24B



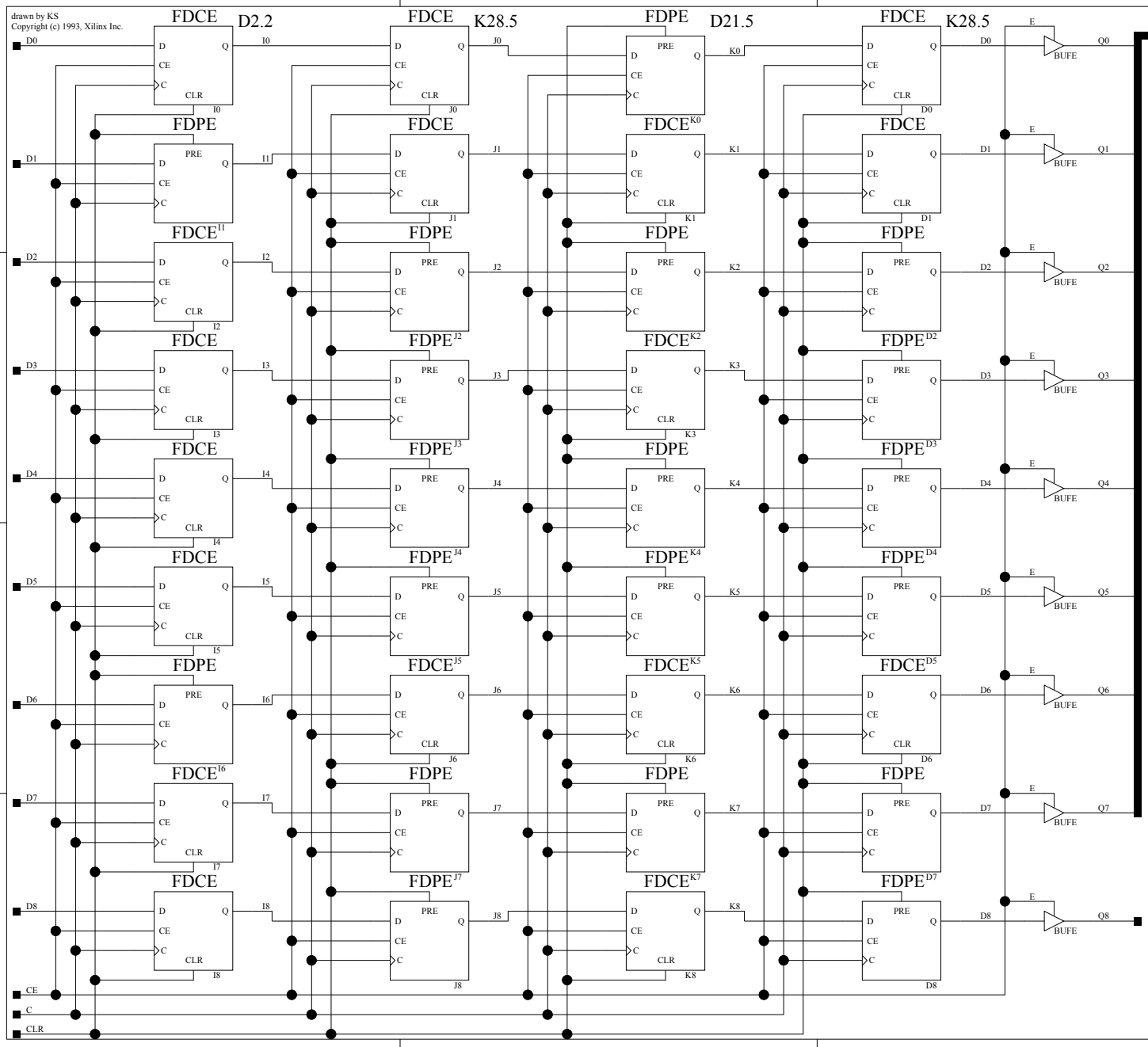
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	JTAG Control Signals DDU Ethernet Logic CMS CSC Electronics	BY JRG	PARENT PAGE 21A	PROJECT D785C
			DATE 5-25-2005_15:01	FILE STATECTL . 4	PAGE 24C



Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)
= 0x1BC + 0x050

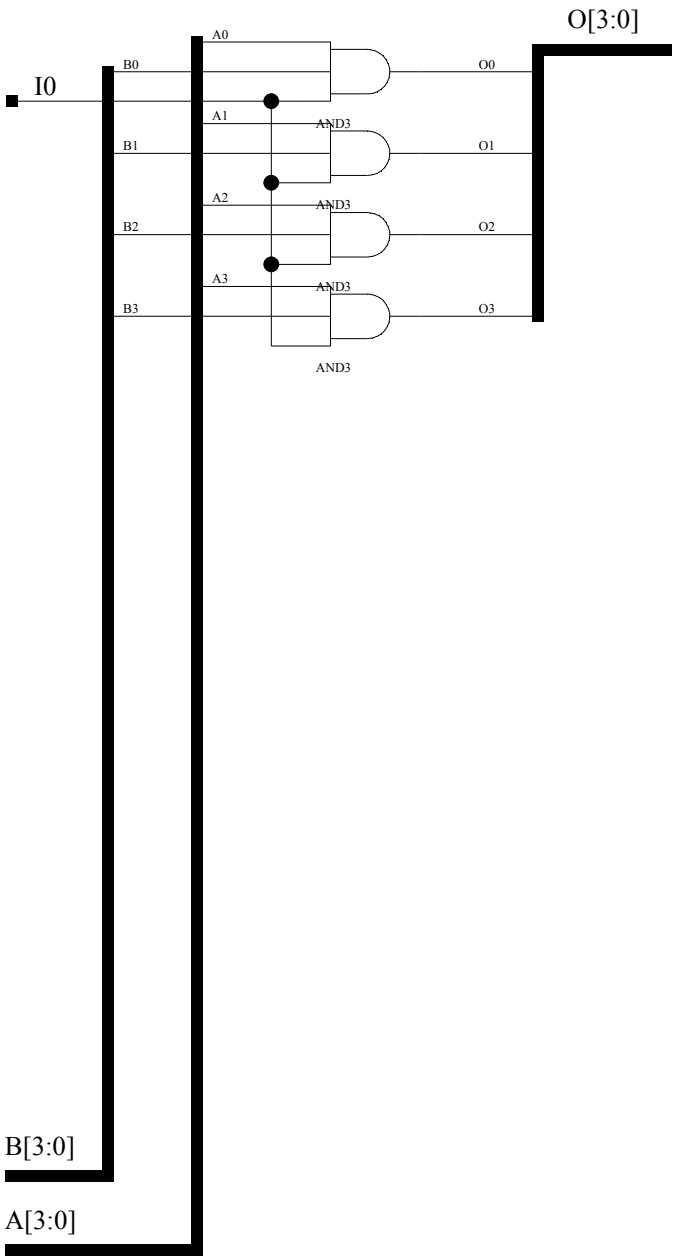
Title:	VIRTEX Family Ethernet Idle Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Idle cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A



Send 4 Sync bytes:

K28.5(10111100)+D21.5(010110101)
+K28.5(10111100)+D2.2(001000010)
= 0x1BC + 0x0B5 + 0x1BC + 0x042

Title:	VIRTEX Family Ethernet Sync Macro		JRG
Comments:	9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Sync cycle		
Date:	7th August 2001	Ver:	1
Sheet Size: B		Rev:	A



XILINX

Title: VIRTEX Family 4-AND3COM1 Macro

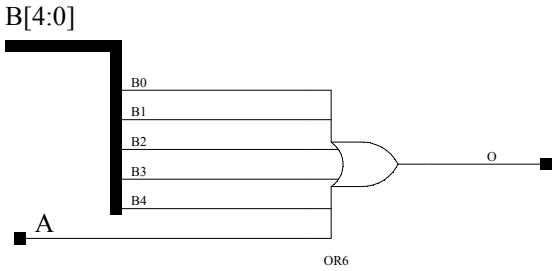
Comments: 4-AND3 Bus Gate plus 1 common bit

JRG

Date: 1st October 2003 Ver: 1

Sheet Size: A Rev: A

drawn by KS

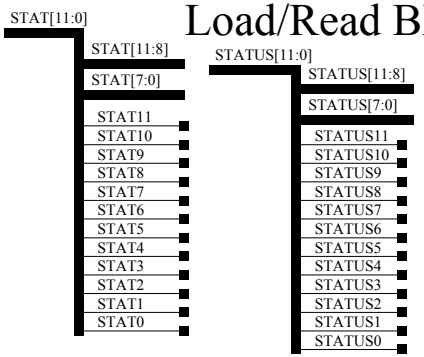


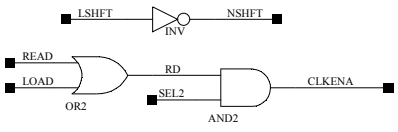
Title:	VIRTEX Family OR5+1 Macro
Comments:	OR5 Bus Gate w/Common
	JRG
Date:	27th December 2001
Ver:	1
Sheet Size: A	
Rev:	A

drawn by KS

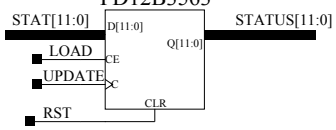
Load/Read BXN Orbit LOGIC

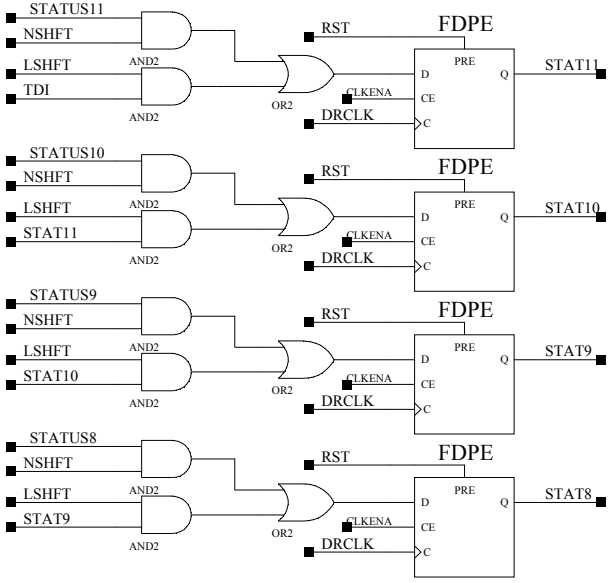
Default=924 BX per Orbit

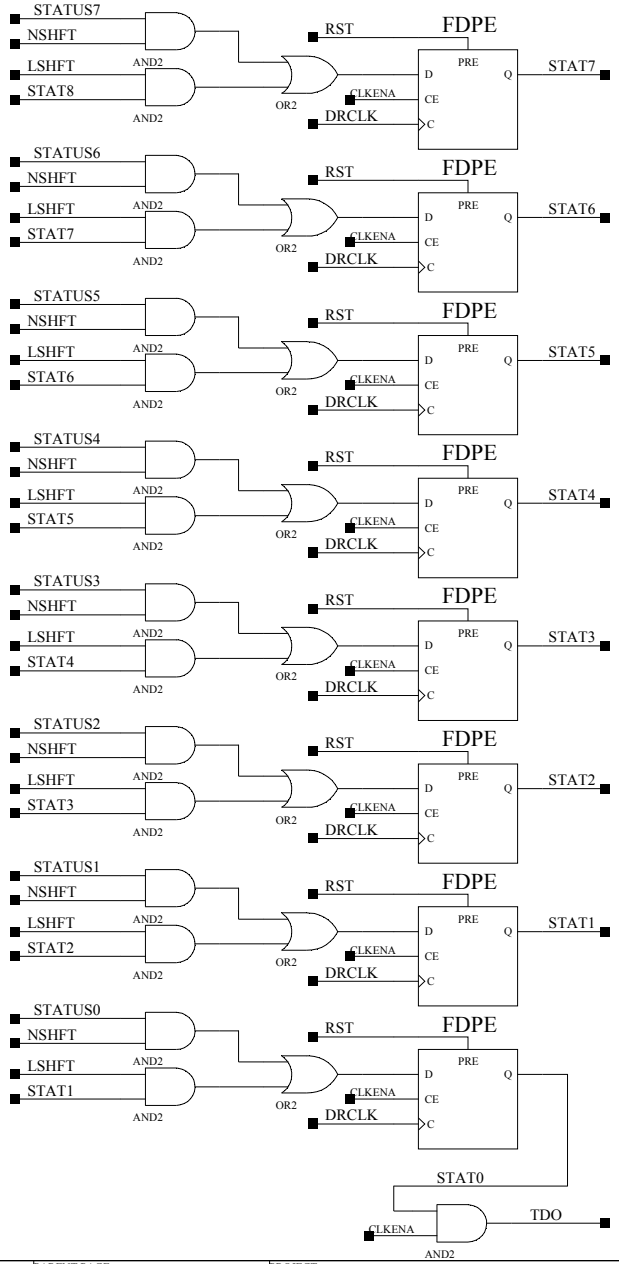




Page 34
FD12B3563

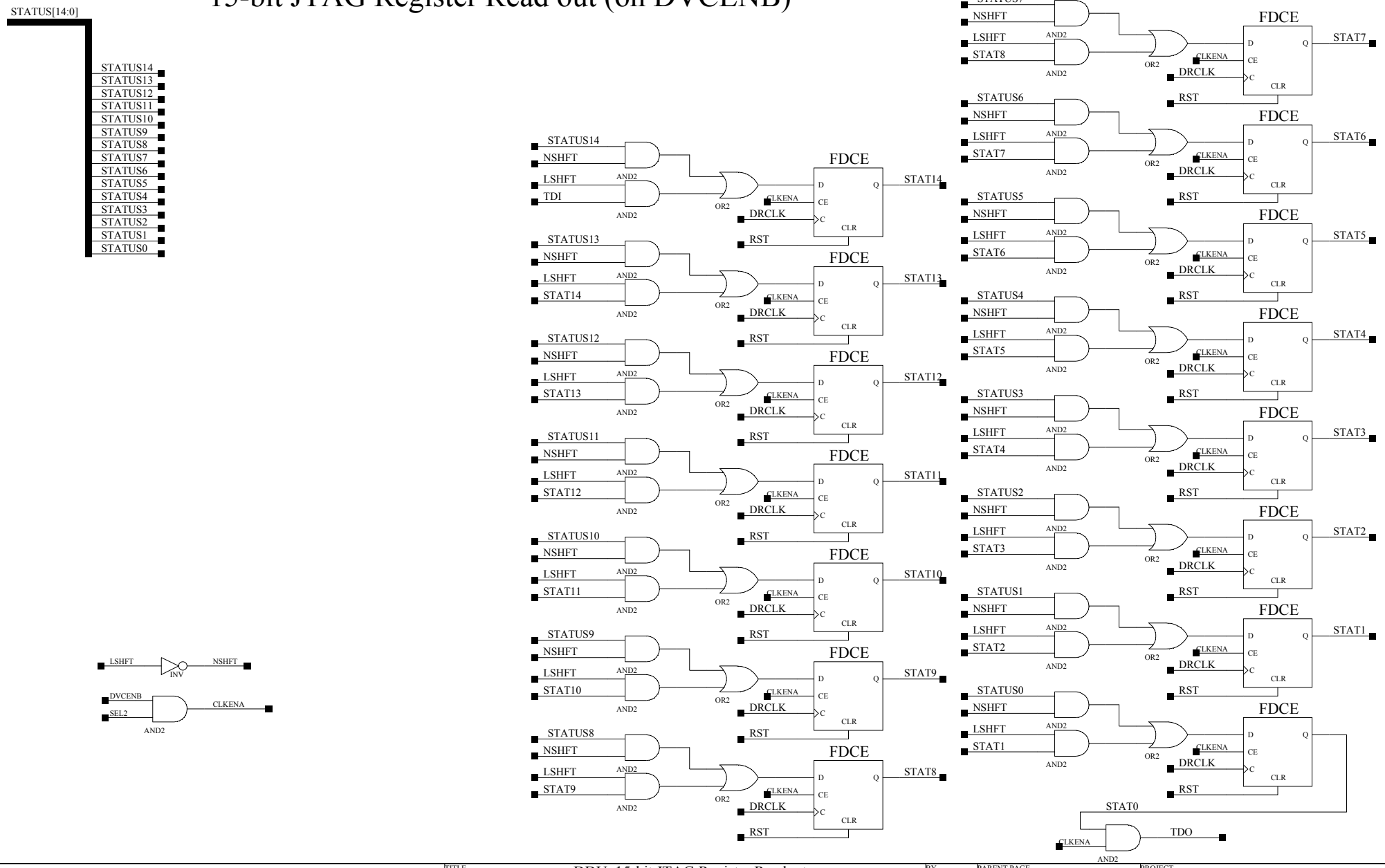






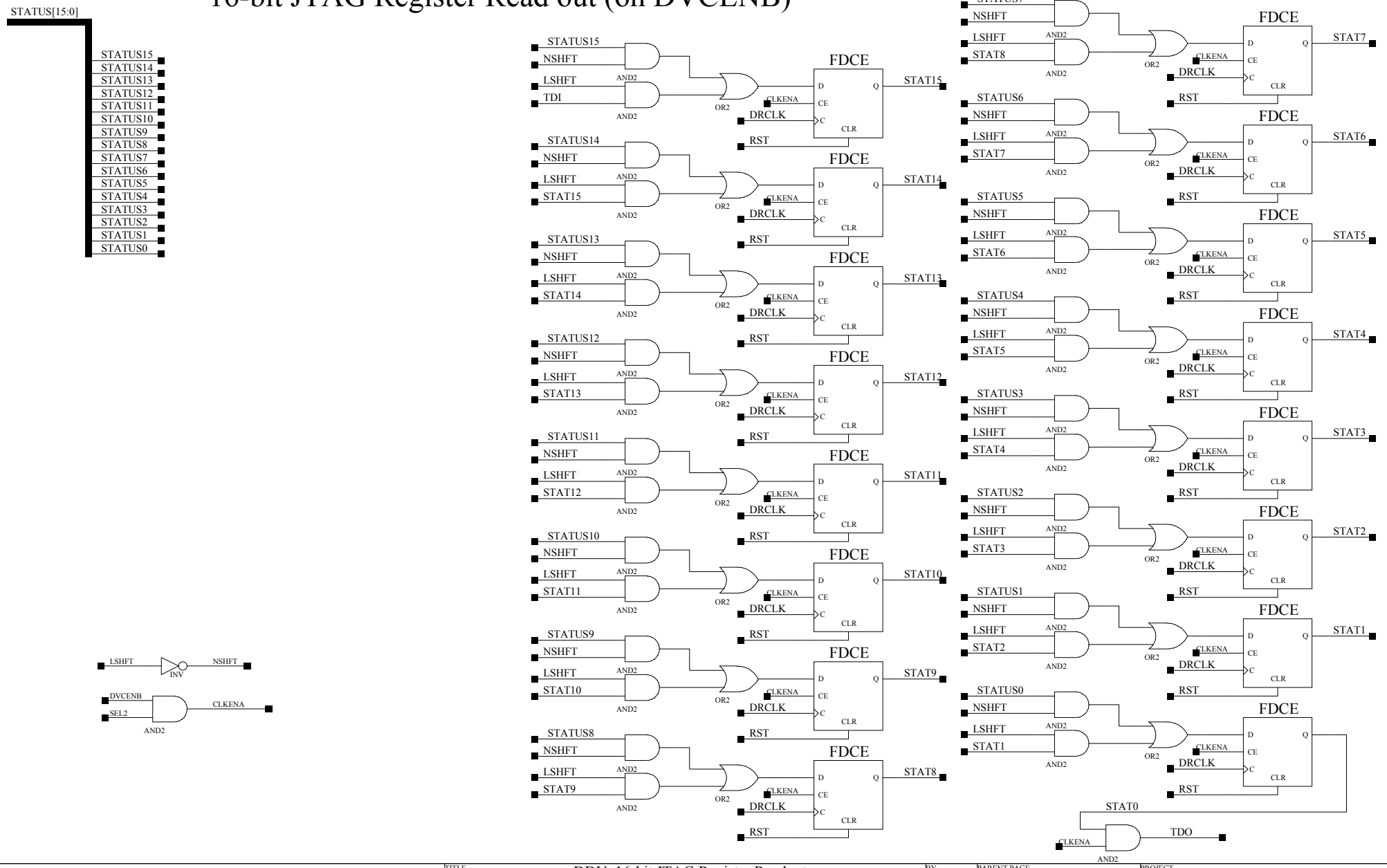
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU Load/Read BX per Orbit Register DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3F	PROJECT: D785C
		DATE: 9-19-2005_9:55	FILE: BXN_REG_1	PAGE: 29

15-bit JTAG Register Read out (on DVCENB)



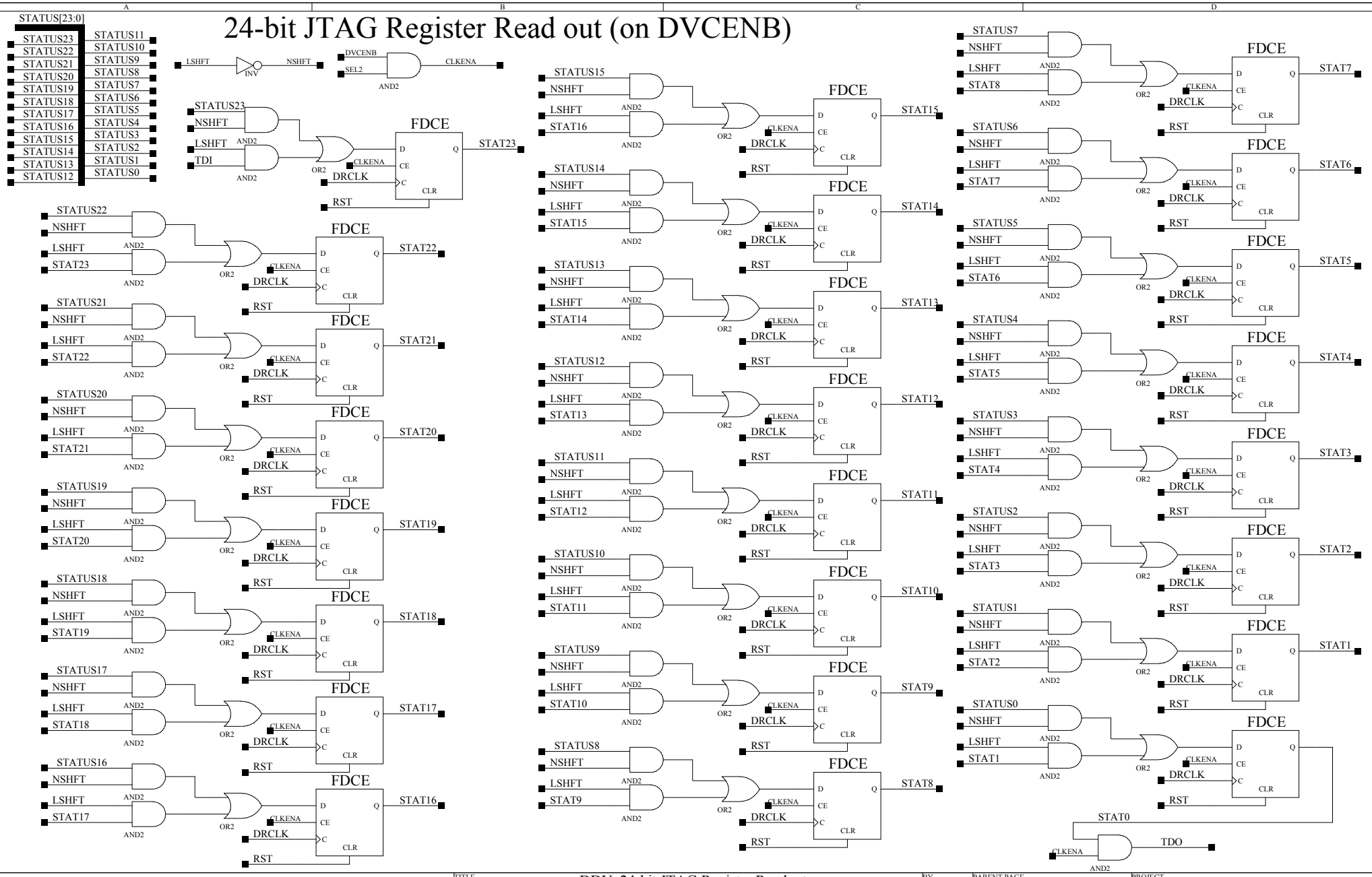
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 15-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG DATE: 1-26-2005_12:16	PARENT PAGE: 3D FILE: CHECK_15_1
		PROJECT: D785C	PAGE: 31

16-bit JTAG Register Read out (on DVCENB)



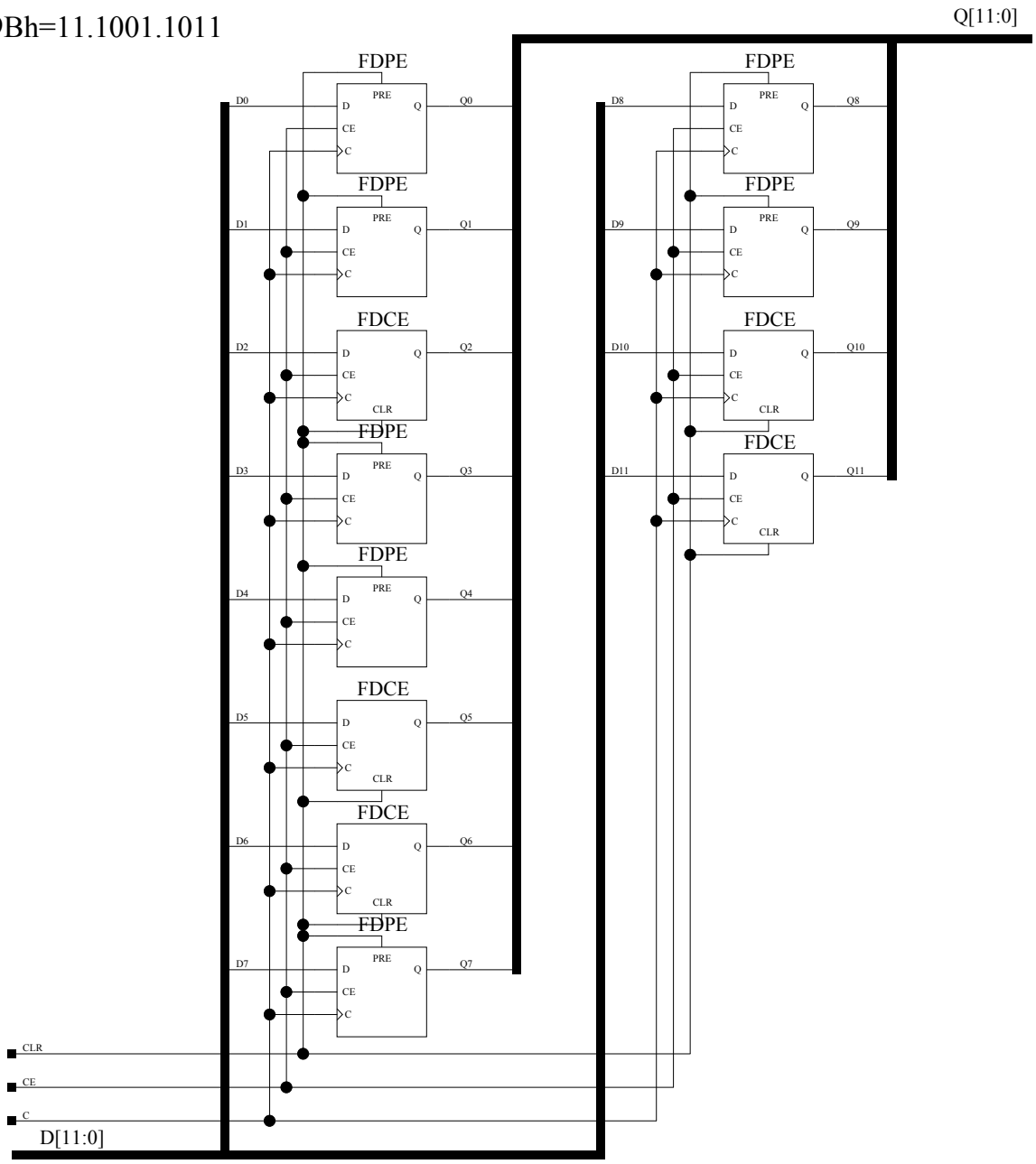
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 16-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:16	FILE: CHECK_16_1	PAGE: 32

24-bit JTAG Register Read out (on DVCENB)



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DDU 24-bit JTAG Register Readout DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 3D	PROJECT: D785C
		DATE: 1-26-2005_12:17	FILE: CHECK_24_1	PAGE: 33

def=923=39Bh=11.1001.1011



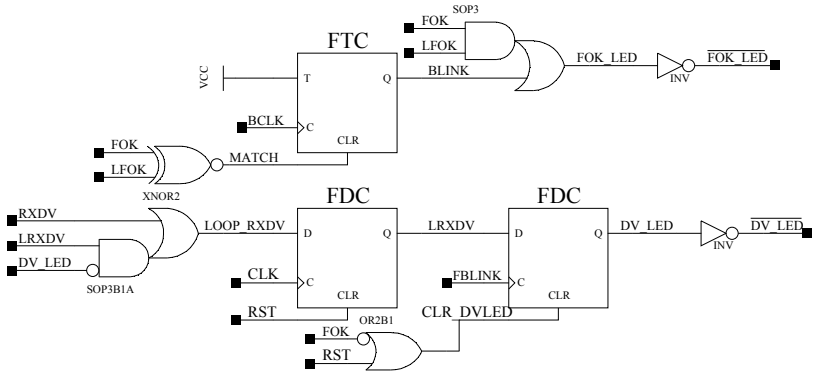
Title:	VIRTEX Family FD12b923 Macro		
Comments:	12-Bit D Flip-Flop with Preset to 923d and Enable	JRG	
Date:	8th May 2003	Ver:	1
Sheet Size: B		Rev:	A

FOK LED

--LIT == Link is alive and well
--BLINK == Link not ready
--OFF == Link not present

DAV LED

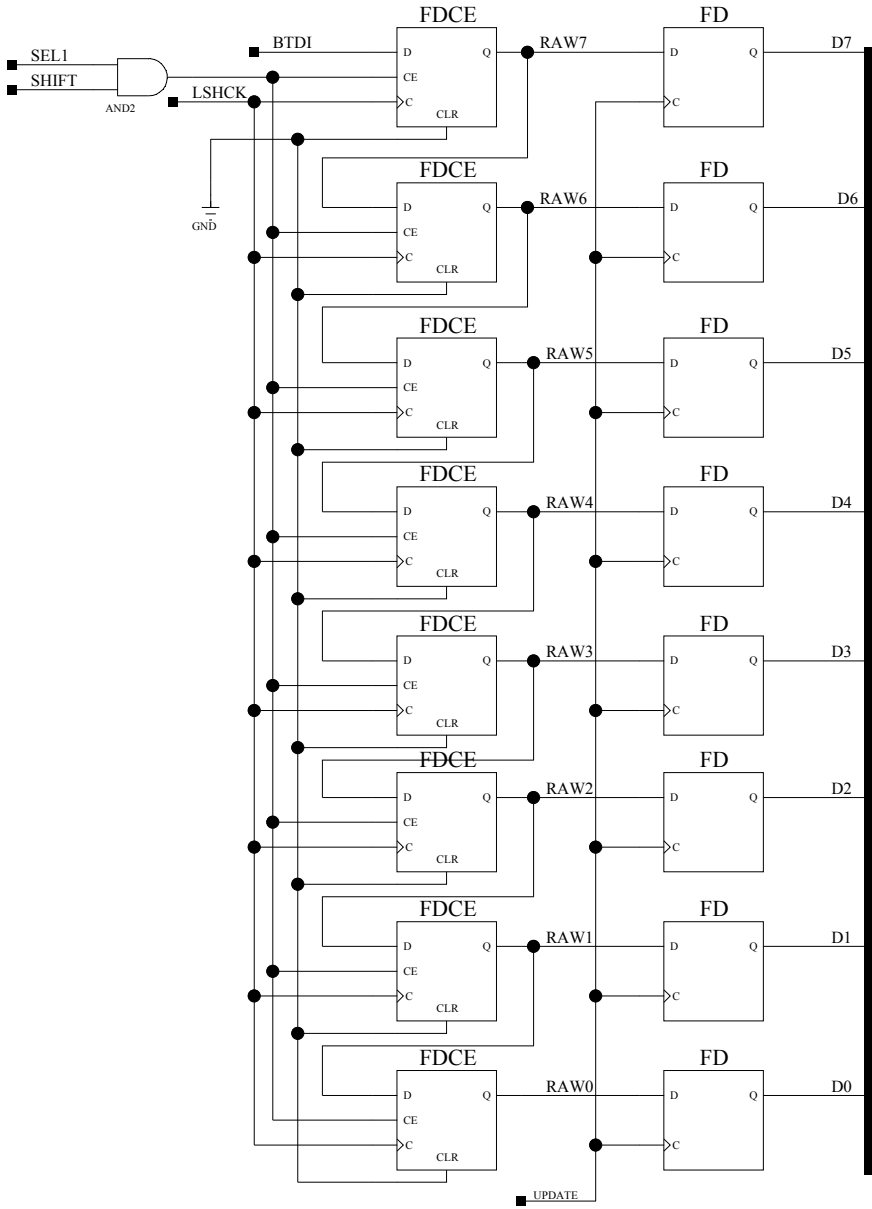
--LIT == Active Data Xmit
--OFF == No data to Xmit



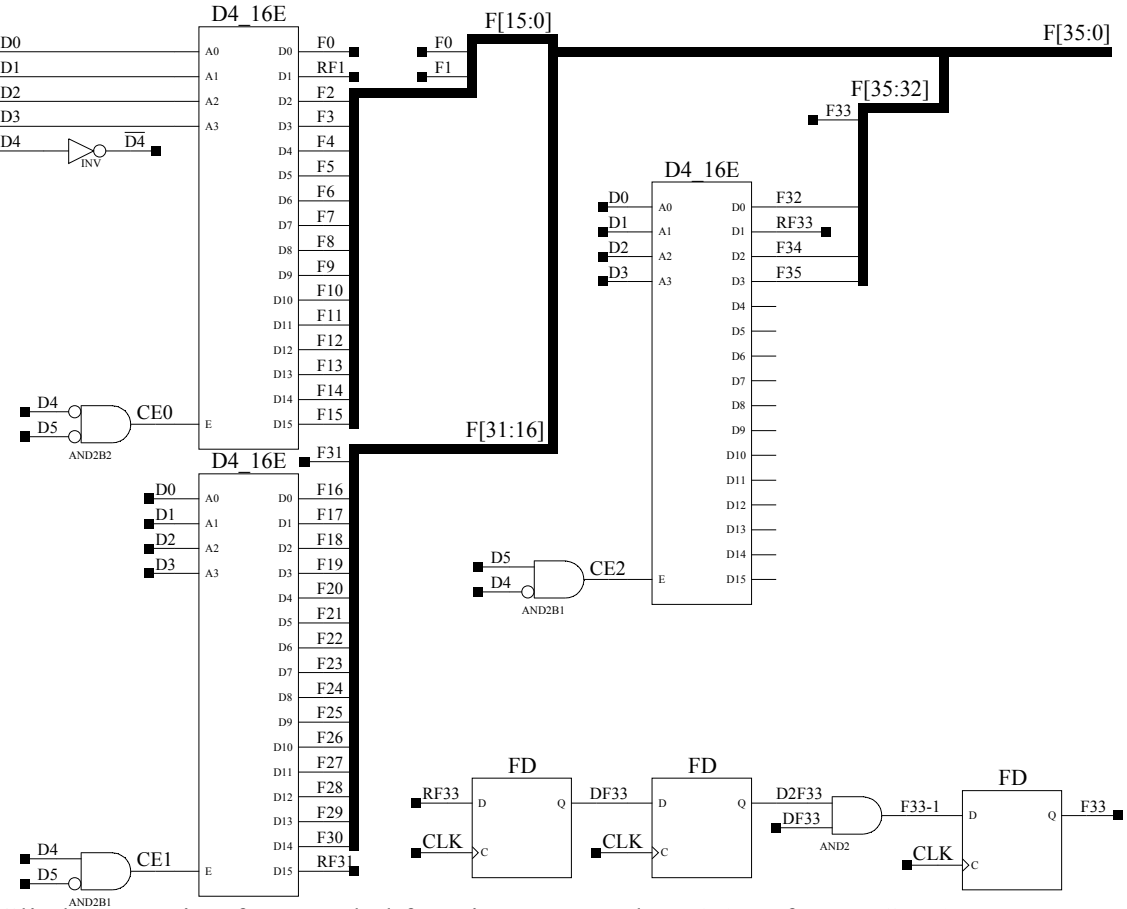
XILINX JRG

Title:	FIBERLED
Comments:	Custom LED Slow-Blink Control for Fiber Inputs
Date: 27th January 2004	Ver: 1
Sheet Size: B	Rev: A

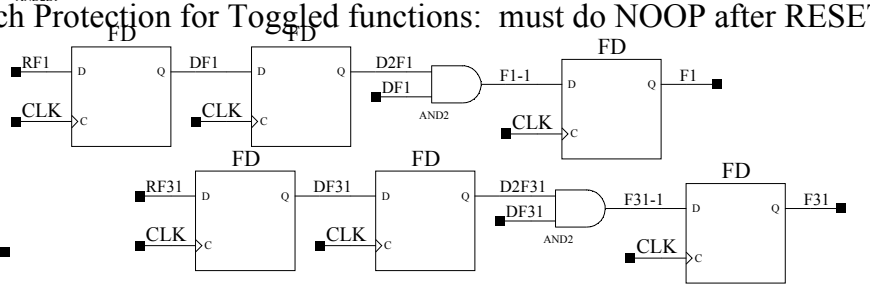
8 Bit Instruction Register



decode first 36 OpCodes (6 bits)

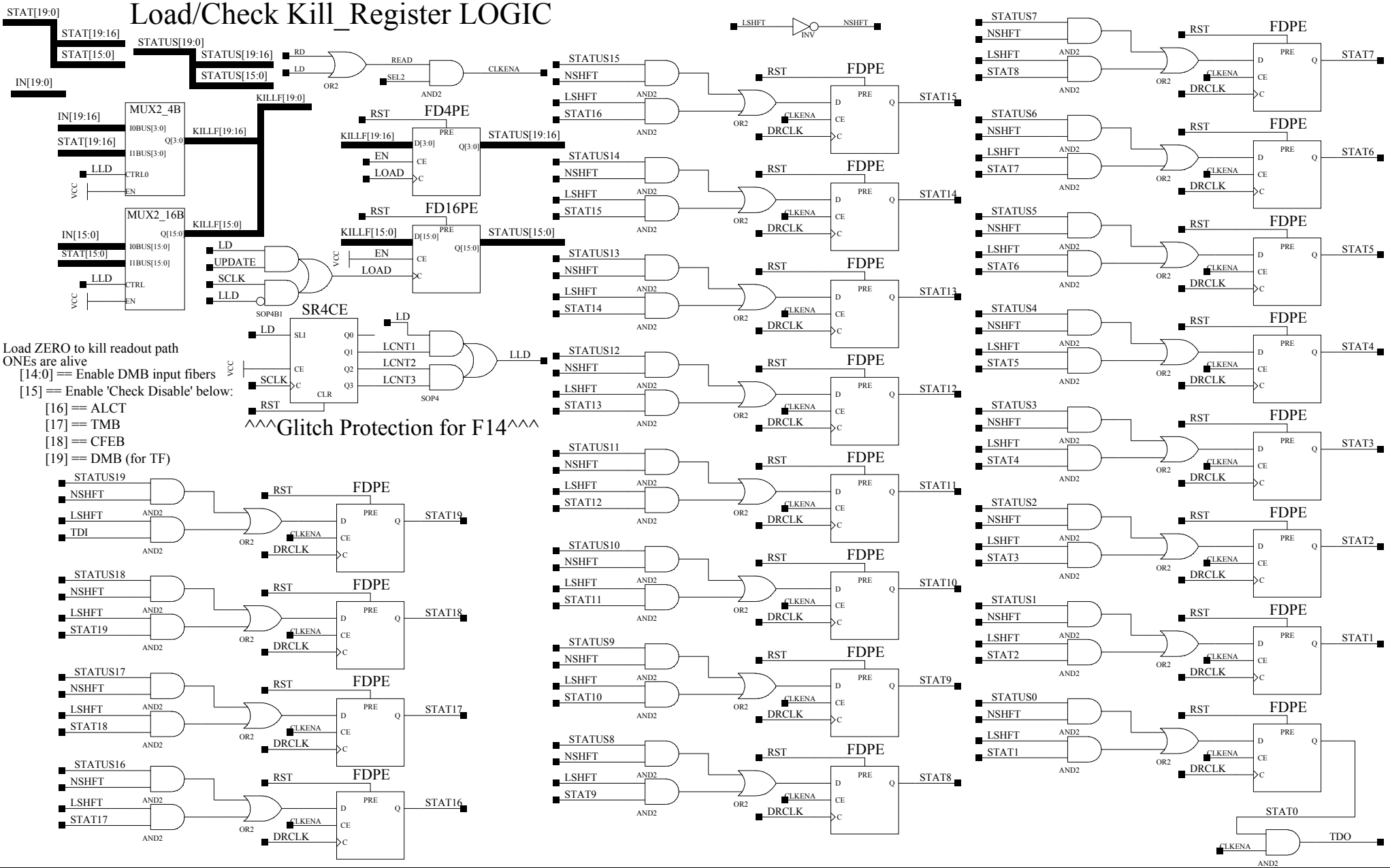


Glitch Protection for Toggled functions: must do NOOP after RESET!



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE JTAG Instruction Decode DDU Controller CMS CSC ELECTRONICS	BY JRG	PARENT PAGE 3D	PROJECT D785C
		DATE 1-26-2005 12:19	FILE INSTRGDC . 1	PAGE 36

Load/Check Kill_Register LOGIC



Load ZERO to kill readout path
ONEs are alive
- [14:0] == Enable DMB input fibers
- [15] == Enable 'Check Disable' below:
  - [16] == ALCT
  - [17] == TMB
  - [18] == CFEB
  - [19] == DMB (for TF)

^^^Glitch Protection for F14^^^

THE OHIO STATE UNIVERSITY
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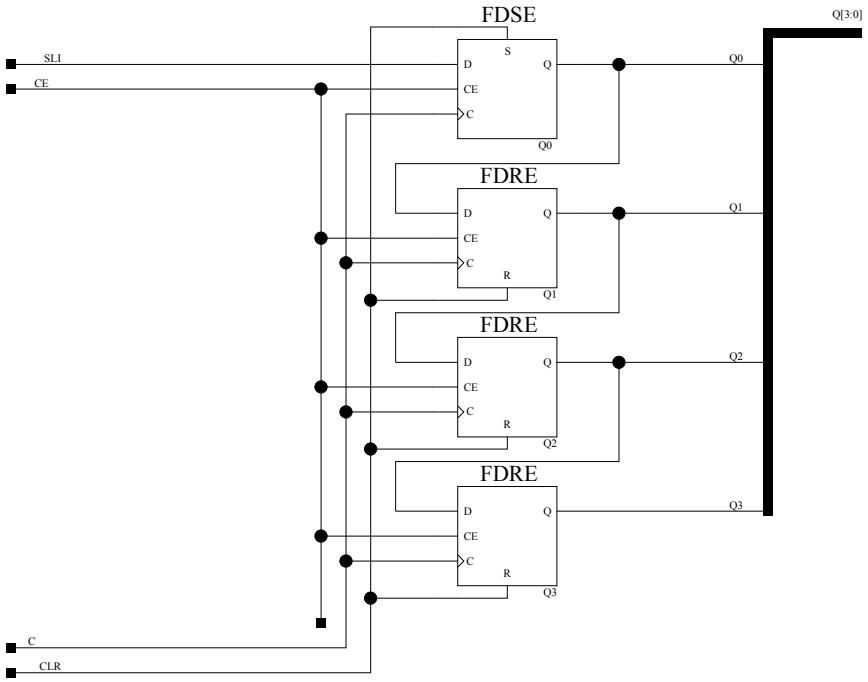
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU Load/Check Kill_Register Logic
DDU Controller
CMS CSC Electronics

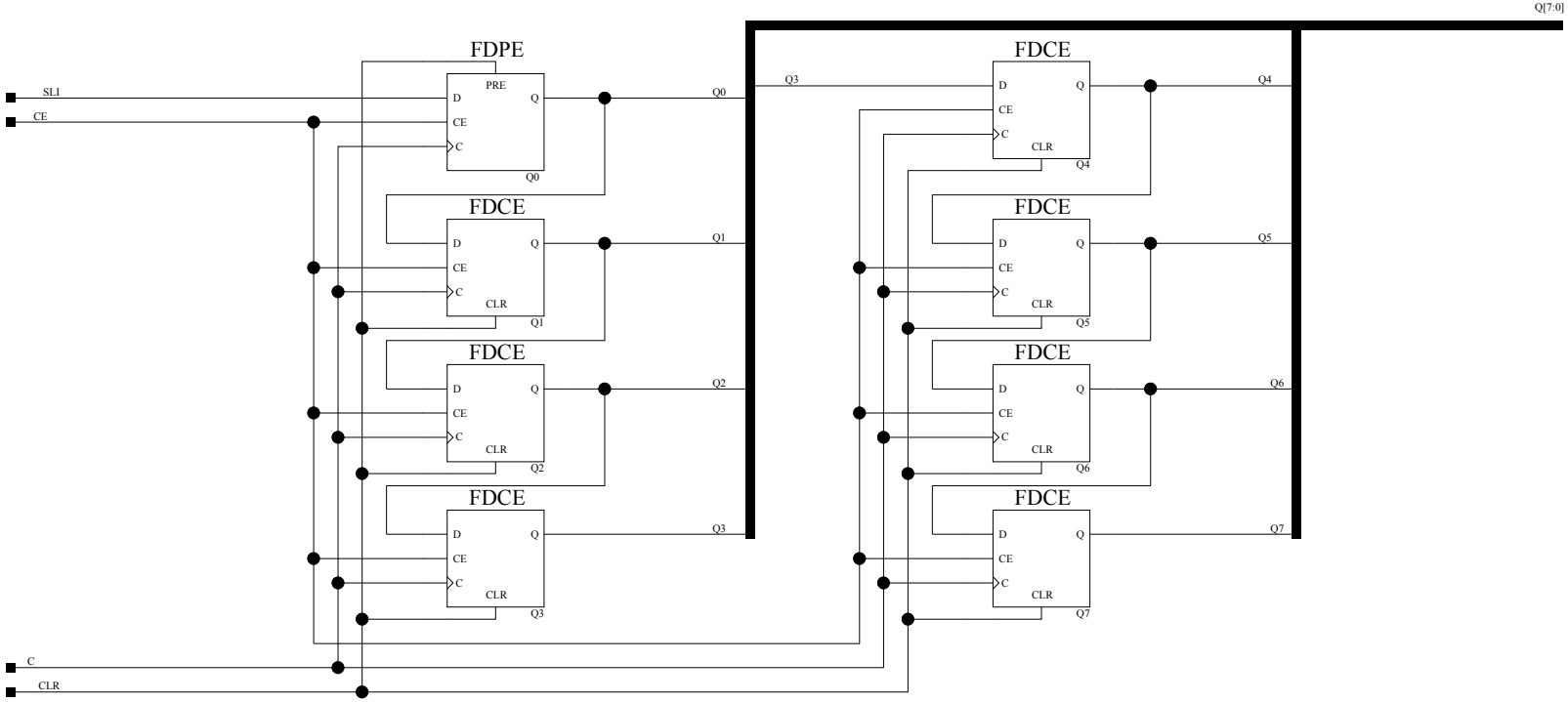
BY	PARENT PAGE	PROJECT
JRG	3D	D785C
DATE	FILE	PAGE
4-12-2007_11:03	KILL_REG_1	37



drawn by KS

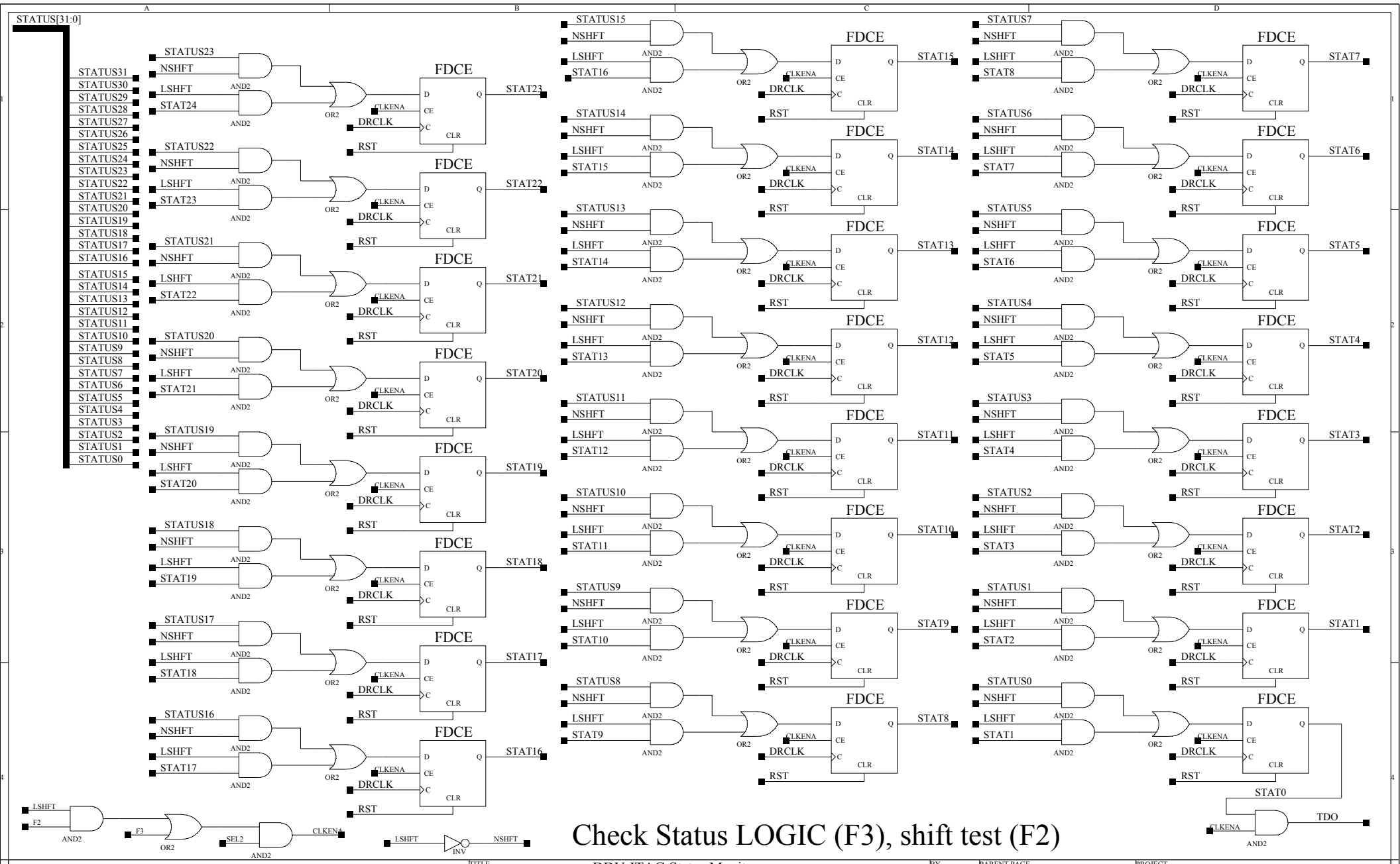
XILINX

Title:	VIRTEX Family SR4CE Macro	JRG
Comments:	4-bit Serial-In Parallel-Out Shift Register w/ Enable, loads a single "one" on Sync Reset	
Date: 7th August 2001		Ver: 1
Sheet Size: B		Rev: A



Title:	VIRTEX Family SR8CE Macro	JRG
Comments:	8-bit Serial-In Parallel-Out Shift Register w/ Enable, loads a single one on Async Clr	
Date:	7th August 2001	Ver: 1
Sheet Size: B		Rev: A

drawn by KS



Check Status LOGIC (F3), shift test (F2)

THE OHIO STATE UNIVERSITY
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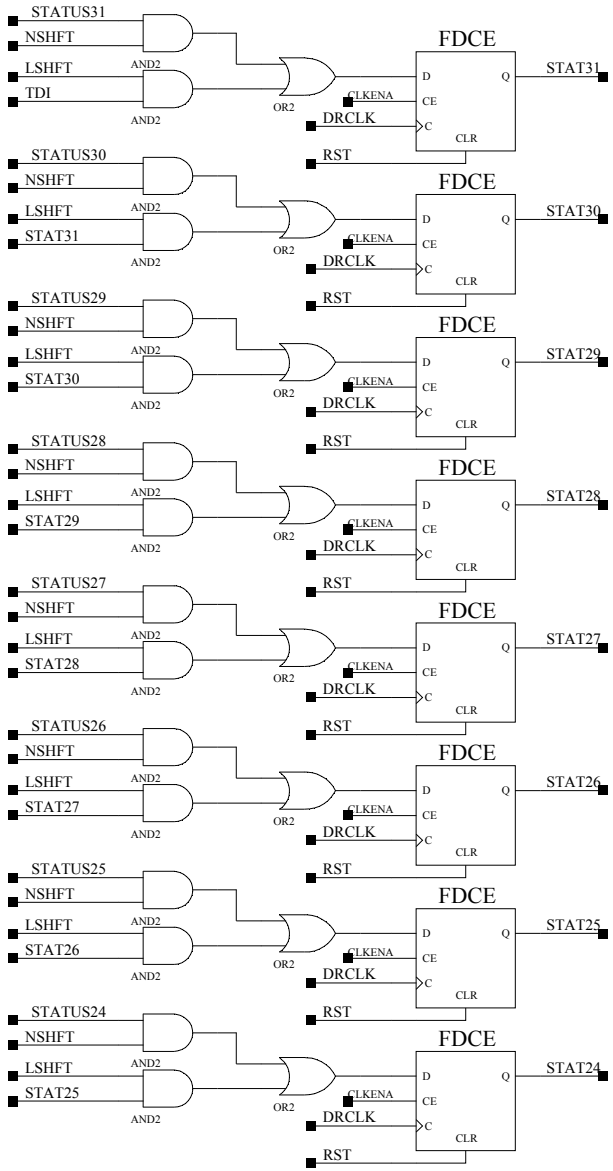
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU JTAG Status Monitor
DDU Controller
CMS CSC Electronics

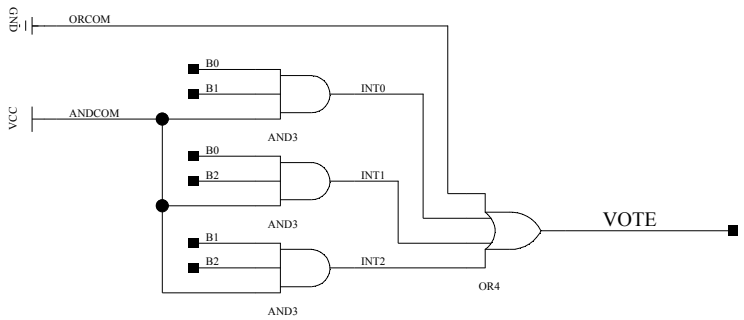
BY	PARENT PAGE	PROJECT
JRG	3D	D785C
DATE		FILE / PAGE
1-26-2005_12:27		STAT_MON_1 / 40



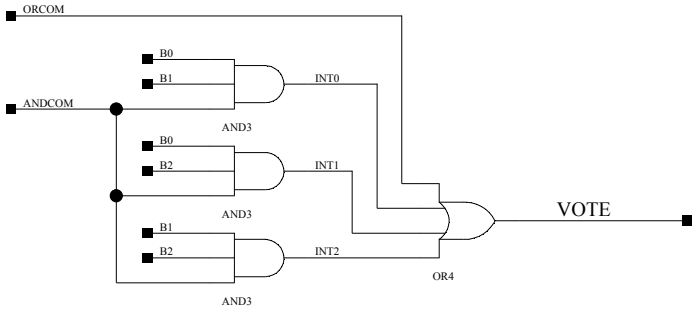
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DDU JTAG Status Monitor
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	3D	D785C
DATE		FILE / PAGE
1-26-2005_12:27		STAT_MON_2 / 40A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Vote 2 out of 3 DDU Controller CMS CSC Electronics	BY: JRG	PARENT PAGE: 12C	PROJECT: D785C
		DATE: 1-26-2005_12:28	FILE: VOTE3 . 1	PAGE: 41



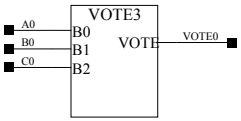
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Vote 2 out of 3, PLUS common AND and OR bits DDU Controller CMS CSC Electronics	BY: JRG DATE: 7-18-2005_16:56	PARENT PAGE: ?	PROJECT: D785C FILE: VOTE3P . 1 PAGE: 42

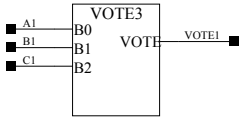
A[15:0]

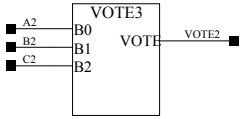
B[15:0]

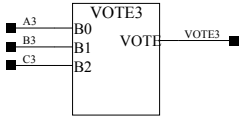
C[15:0]

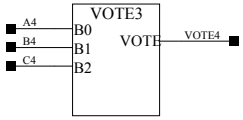
VOTE[15:0]

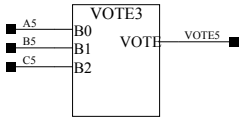


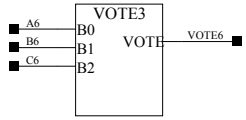


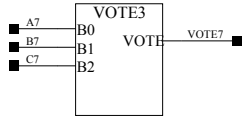


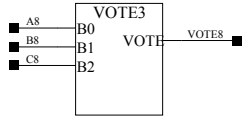


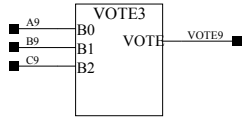


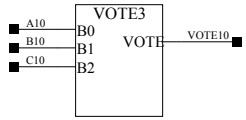


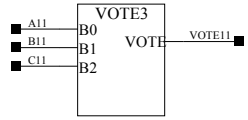


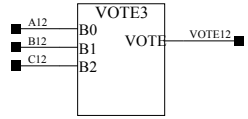


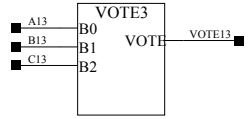


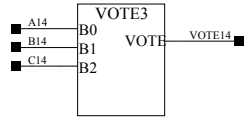


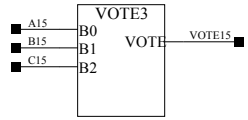












THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Vote 2 out of 3 on a 16-bit bus
DDU Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
JRG	12J	D785C
DATE	FILE	PAGE
1-29-2009_14:47	VOTE3_16 . 1	43