

DDU5CTRL

(file 0dductrl)

8-4-2014_16:21

CMS CSC DDU5, Central Control FPGA

CF056A02

Version 56

v48: GbE skips Empty Events for Global runs
v49: add SYSTEM_RDY diagnostics on LA0 mode 11; r2: add ChBond code for DCC r7: ChBond fix
v50: hold back Resync until Empty for TFDDU; v51: new ChBond method; r2: ChBnd runs free sync RST
r3: add special Idle sequence for DCC; r4: change special Idle
v52: prevent backpressure response during DoFW phase, may allow 7 words to DCC
r2: replace all EvtCntRst functions with RST; r3: edit RstStop logic, remove ~DoDat; fix DDU_IS_EMPTY startup logic
r4: tune DDU_IS_EMPTY wait for EOE logic v53: change LinkRdy->DCCwait logic, store both for EOE status register
v54: add DCC Preamble (default) plus ForceIdle logic states r2: fix WantRen logic, tune DoIdle & OSTAT fields
v55: DMB format and SrcID + S-Link changes for 2014 r2: force GbE FOK input signal High. r3: fix bug & try again
r4: fix kill_alct/tmb handling in TrgTrail logic, modify FOK_GBE bypass to use ModeBit4, set ModeBit7 to ignore S-Link Wait
r5: fix logic for DMB HalfFull (low true) in Stage2
v56: modify Trail bits 15:8 (status-copy) for CMS DAQ compatibility
r2: fix bug in trailer bus definition

Set All I/O to 3.3V

PART=XC2VP7-6-FF672

PROM=2*XC18V04-VQ44 (PARALLEL)

DDU5ctrl\DDU5ctrl\ddu5ctrl
C051DD99
C151DD99

PromID: 05026093h
FPGAid: 2124A093h

PROGRAM takes < 55 ms (31ms this FPGA)

DDUCNTRL

- 1: Mode Bit 0
- 2: Mode Bit 1
- 3: Mode Bit 2 LED0 on top, pins on away-side from LEDs
- 4: Mode Bit 3 RST_1=Asynchronous Reset for FPGA1 and ALL FIFOs
- 5: Mode Bit 4; High for GBE debug, Low otherwise
- 6: GbE test, send counter on GBE link
- 7: Set L1A Fake mode, Kill TTC L1A/BXR/ECR if SW8 is off
- 8: FPGA version on LEDs

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DDU Format Since DDUctrl v15:

H1: 0x/51/NN.NNNN/XXX/1.II/VK
H2: 0x/8000/0001/8000/HHHH
H3: 0x/LLLL/0000/ZZZZ/GGMY

T-2: 0x/8000/FFFF/8000/8000

T-1: 0x/SSSS.SSSS/QQQQ/PPPP

TR: 0x/A/?/WW.WWWW/RRRR/UUMK

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes
DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070: 240560 Bytes
^^Ignores TMB Data^^ GBE ByteCount = 8*DDU_WordCount 8 TS assumed

DDU5CTRL -- Project History

- To Do:
- COMPARE BXN (DMB/TMB too)
 - Watch for TRG buff overflows
 - Determine correct values to store in Flash Mem
 - > BX offset, KillCh's, FIFO thresh, Board ID
 - Test DCC/SlinkWait feedback function & thresh's
 - > Make DMB stop too
 - Verify that CFEB-CRC is fixed for B-code case
 - No logic for BUS1, DCC SBDATA & TDxxx, 4 LSF, 4 LRL
 - Make Verilog module to get Fiber/DMB_RD in one CLK?
 - Multiple TRG_L1err ought to request a Sync Reset?
 - * Same for consecutive events with a TRG_L1err?

- Check Phase of CMD to CLK40
- * pg. 2G & 3I
 - CFEB-DMB sync check pg. 12C
 - CFEB-L1A check disabled, pg. 12D: not! Found a fix...
 - options for Monitoring on pg. 3H, 12E?
 - Does CFEB-Check-Disable cause TF/SP mimic?

TST	Clock	BUFGMUX
0P	drck1	5P *4P -TR
2P	2clk	5S *1S
3S	clk	7S *7S
0S	clk625	2S- *2S
7P	ck125	1P *0S -BL
5P	clk40	0S *3P
4S-	clk156	4S- *4S
1S	drck2	3P *5S
6S-	sclk	6S- *6S

* denotes LOCed position

New Ideas: Store & check DMB source ID's from each fiber?

Default Startup Order:

- Release DLL (no wait)
 - 4) DONE
 - 5) En. Outputs
 - 6) Release WE
- Feed SLINK status into FMM logic (for UF).
- In case of StuckData send PRST? How to distinguish SEU? Later event still gets LostHdr or Timeout, could self-correct. Add "PRSTed" VME register to track occurrence.
- In case of L1Amismatch, let it run and see if it is better a few~10 evts later. Possible to self-correct as above...? Can only work if DMB really lost event data.

DDU Format since DDUctrl v15:

H1: BOE1 type L1A Number BXN ID_FOV K-Status 0x/51T/NN.NNNN/XXX/11/VK

H2: 49-bit -unique constant DMBBn(U5) 0x/8000/0001/8000/HHHH

H3: LiveDMB(U5) Ostat DMB-DAV(U5) BOEstat DMBcnt 0x/LLLL/oooo/ZZZZ/GGMY

T-2: 64-bit unique constant 0x/8000/FFFF/8000/8000

T-1: DDU(LFOE Status DMBErr DMBWarn(U5)) 0x/SSSS.SSSS/QQQQ/PPPP

TR: EOE WordCount CBCWord EOEstat K-Status 0x/A/?/WW.WWWW/RRRR/UUMK

DDU WC, 3 DMB with 1 CFEB (nC FEB=3): 26Ah = 618 dec, 4944 Bytes

DDU WC, 4 DMB with 1 CFEB (nC FEB=4): 336h = 822 dec, 6576 Bytes

DDU WC, 7 DMB with 1 CFEB (nC FEB=7): 59Ah = 1434 dec, 11472 Bytes

DDU WC, 8 DMB with 1 CFEB (nC FEB=8): 666h = 1638 dec, 13104 Bytes

DDU WordCount (64-bit words) for "No Data" event: 0x006.

DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes

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DDU WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070: 240560 Bytes

^^Ignores TMB Data^^ GBE_ByteCount = 8*DDU_WordCount _8 TS assumed_

DDU WC, 11 DMB with 1 CFEB (nC FEB=11): 8CAh = 2250 dec, 18000 Bytes

DDU WC, 12 DMB with 1 CFEB (nC FEB=12): 996h = 2454 dec, 19632 Bytes

DDU WC, 15 DMB with 1 CFEB (nC FEB=15): BFAh = 3066 dec, 24528 Bytes

v1-2: from ddu4ctrl_v28, FIFO Full JTAG Reg is 16-bits

Last w/DDU_FOV=4 ----> v10-12: Add RCLK1, Tune OutUnit GT resets, tune DCC_WAIT modes & add Kill opti

v13-14: Fix LVT/LVA, kill DMB-CFEB-Sync, bring DMB Results to CRCerr; tune DMB checks, GbE Prescale & SLinkWtEn from VM

v15-16: fix DMBwarn, add VME_FakeL1enable; put DMBLIVE[14:0] in HDR3; put DMBwarn/err in TR-1, Tune TRG_Trail_Err resets, FOV

v17-18: tune DMB_Full, RST_InStat, EndTimeRST, PRST, add InRd-C-Code JTAG path (F20), GbE Packets now 7952 by

v19: Require SLinkWaitEn for CFEB_L1err check; v20: set RCLK0 to FAST24, CKFB to SLOW6---->rev2: SLOW

v21: add C-code-err Begin/End to JTAG F20, set CLK40-0 to FAST16, DMBliveErr & In_Time_Out go to BOE_S

v22: add DMBLIVE reg's on F25/26, CLK40-1 is FAST16, L1A uses OFD_1; rev2: CLK40's use F16-OFDD

Good! rev3: tune PDMBLIVE_EN & RST_STRT logic v23: add KillCFEBchecks & require FKILL15 to EnableCheckDisa

Good! v24: tune DMBlive timing (yellow FMM), bring signals to LEDm10/LA0

v25: tune L1err & InFerr "DMBliveOK", fix TTMB_Err, tune RstBOE, check CFEB L1A only on 1st sample (not critic

v26: BXorbit=3563 now, add IDMB_FULL flag on ERB. v27: tune CFEB_L1er, 8/16 sample flag, WarnMon & BX off

v28: add Big debug reg. on F21, Timeout reg. on F28 use LnextFIFO, replace LLLREN w/LFOE for TimeoutRd

make ERA-St/End-To perm. . v29: fix Mult.L1Err logic, add InSingWarn/InML1Err, tune DDUsyncErr, L1A-fake kills TTC-L

v30: tune Critical Error, InRdWarn, SpyOvfl & LextStop logi

v31: tune CFEB-DAV check (OR DAVs from DMB Hdr1 & Hdr2), add SP/TF compatibility & diagnostic log

v32: change CfebCalDisable default to True, remove DDU_DLL_Err from FMMerr (InRdErr4), modified ErrB13 for perm DDU_DLL_

add DDU CSC-Board occupancy monitor-F34? r2: add zeroing logic at RST for Occ.Mon. -r3: fix LRST log

v33: change SourceID=760=2F8h for TF-DDU v34: Inverted CCB_CMD bus & L1A **for TF-DDU ONLY!

v35: Autodetects TF-DDU, now compatible w/wo TF; add SyncHold & CloseL1A logic; r2, removed redunda

RdyIn2 requirement for SEN bits. r3-4, OSyncRst on -Clk40, tune OFIFO Mon, req. VMEctrv17+ & InCtrlv22r

v36: non-TF DDU's have SrcID=BrdID, NoLiveFibers now readout on L1A. r2: change TF_SIG to FDRE, Reset CheckCRC with NewTFD

v37: diagnostic changes....Tune DMBL1err(notALCTerr), BadCtrl(notMissTrg), LIE(addMissTrg

DMB/TMB/ALCTerr account for MissTrgTrail, DMB-to on Era15, XtraTrgTrails on Erc5+13,DDUfmm 3-bits held Reset until System

v37r2-3: tune CfebL1aErr/SyncErr & DMBcritErr logic, MultL1err logic, InSingWarn=Era10,ValidDMBfull=ErB0,DMBtimeout=Er

v38: DMBcritErr=Erc7, improve Htmb/alct timing.C-codeErr goes to InMxmitReg, InTimeout goes to EndTimeBusyR

r2: make DAQovfl for FF case only, include C-CodeErr w/MultXmitErr, CFEBcrc flags Reset on BOE, C-code-L1er=FIFOb

LDMB_CRCok held at least 4 cycles

r3: add DMB-TO/FIFOfull to TMB/ALCTerr Regs, adjust their time to L2DMBrd; TrgWC only Comp 8 bits, A-T-Switch Req. NoSpwd

r4: fix LWCb8 Reset logic for long ALCT case (still not inc. in WC check thoug

v39: 64bit_err reset on BOE, TrgWC now uses all 9 bits, CloseL1A range now 1usec, BIG L1Afifo w/better Warn/Busy Lo

r2: add hysteresis for L1A_AF/Busy state, tune DAQovfl logic, tune SysRdy/BUSY logic. r3: tune L1pipe/StuckData lo

-r4: tune CRC_Cnt_Err monitor logic; r5: tune SCAovfl Reset & CountSample timin

v40: DMB & Trig.CRCs use MUX to load Zeroes (not Tbufs), change DDUfb res

-r2: add time constraint to DDUFB reg to eliminate DDUcRC logic lag, r3: tune BuffOvfl & EthLim lo

v41: SCA_Ovfl separated from DMB_Err & SomethingBad. r2: tune KillFiber glitc

v42: change to proposed format for ALCT; r2: FOV=6, on TFSig kill ALCT/TMBerr, correct SBXN f

3564-4096 difference in BX<40 case (from CloseL1A logic) r3: change to new ALCT/TMB data forma

r4: fix TRG bugs in stage2 r5: reduce RST logic delays, may have caused TrgTrail detect problem

added bit usage notes in FIFOCRTL, 27nov2007 v43: tune CMD Strobe timing; r2, adjust TMB/ALCT Fful b

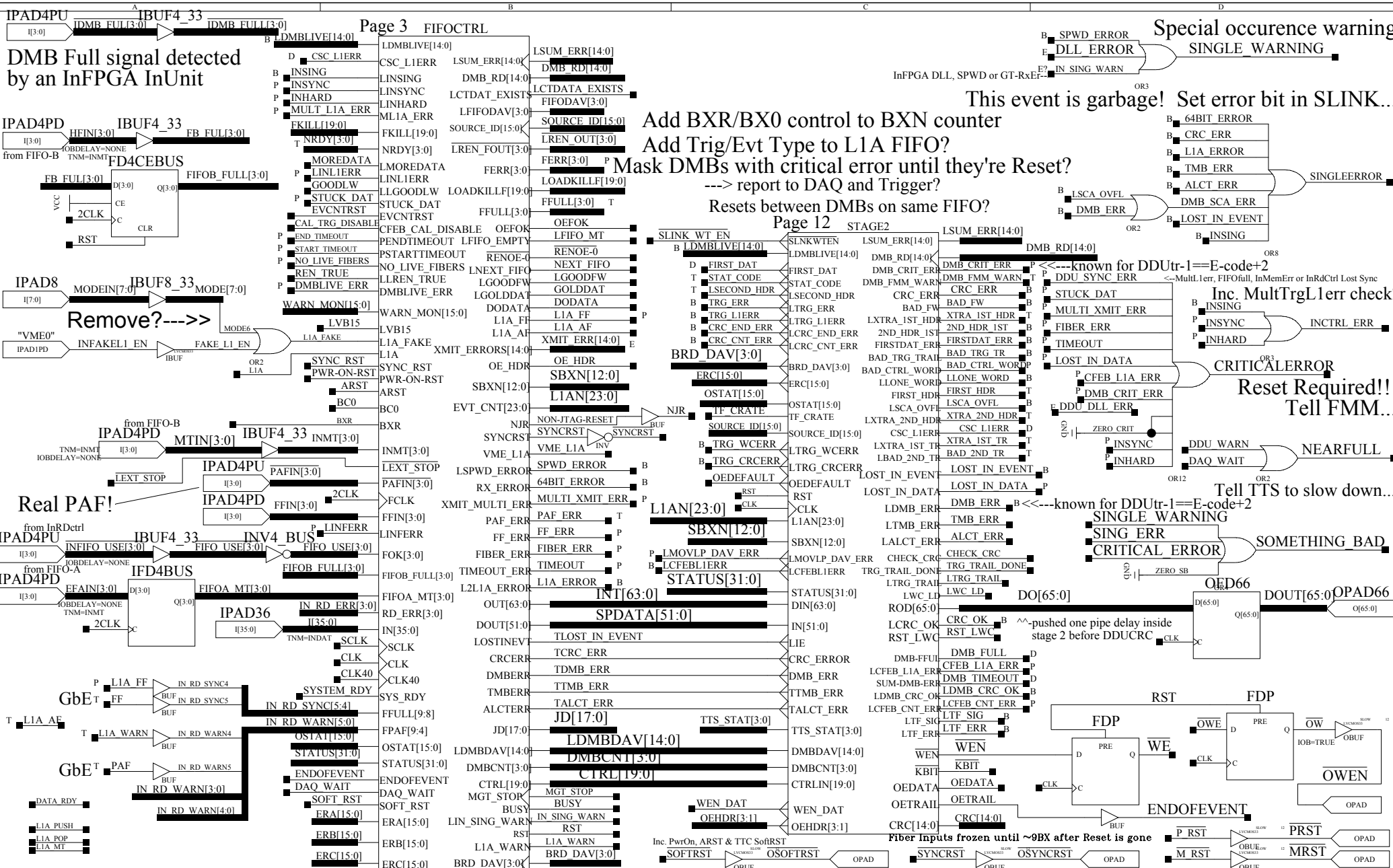
r3: fixed bug in TrgL1err reporting. v44: change TF-DDU definition (0xc0 in Flash-Page

v45: tune TrigTrailProb, CfebCntErr logic, add CSC RepeatErr logic to LsumErr reg & take it to JTAG F

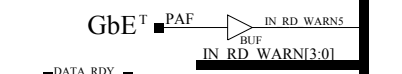
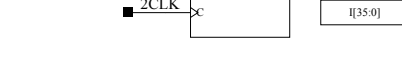
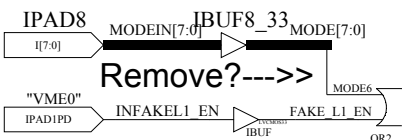
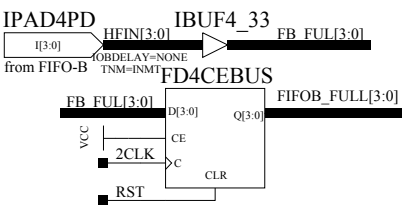
r2: remove DMBwarn from FMMwarn logic. r3: add vote3 for DDUcRC r4: remove CRC voting, delay S-Link clock by 3.

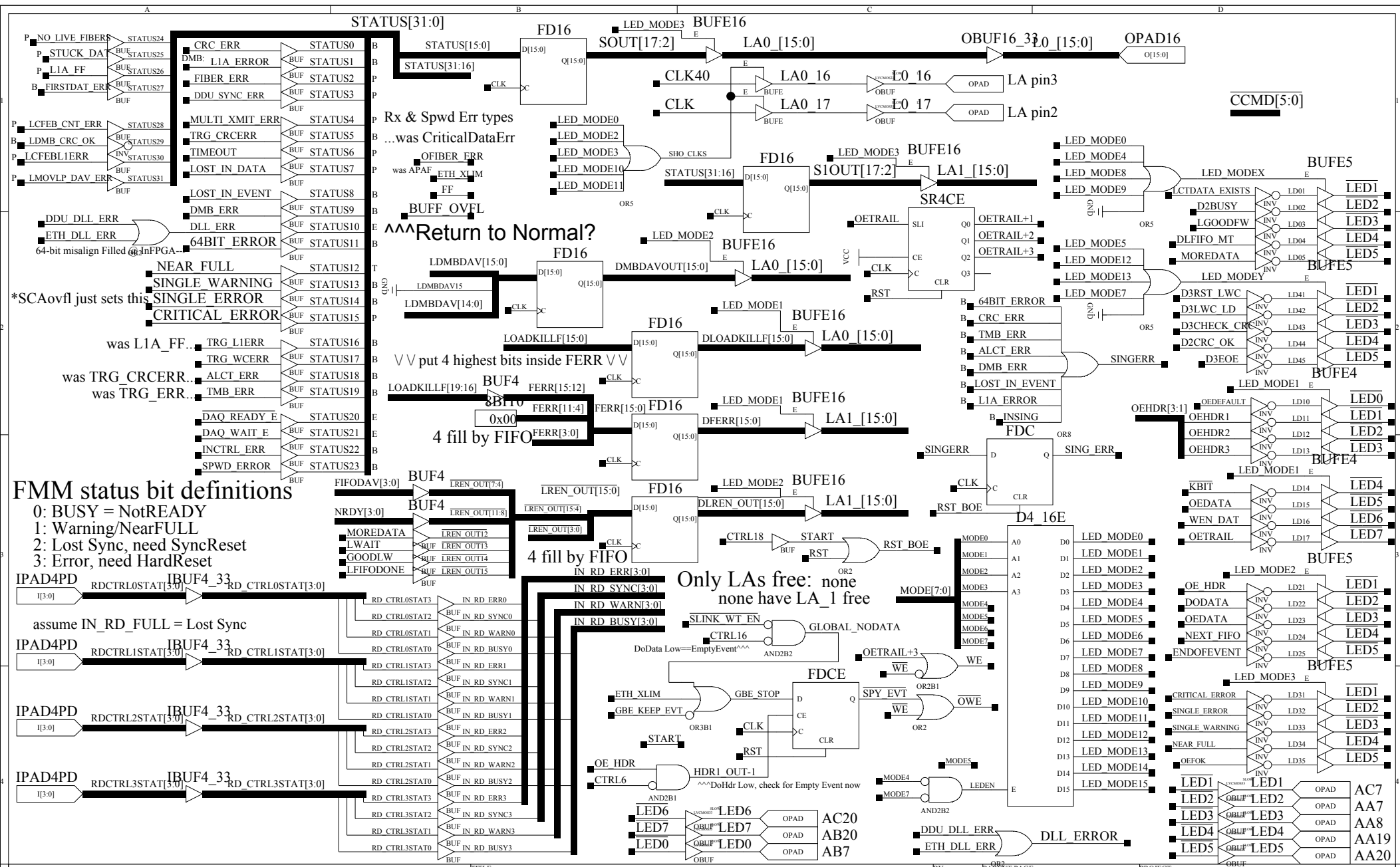
v46: tests ck156, SLink clk from DCM --> SLink. r2: shift OWCLK by +3.2ns v47: move ROD pipe reg. in stage2 before DDUcRC

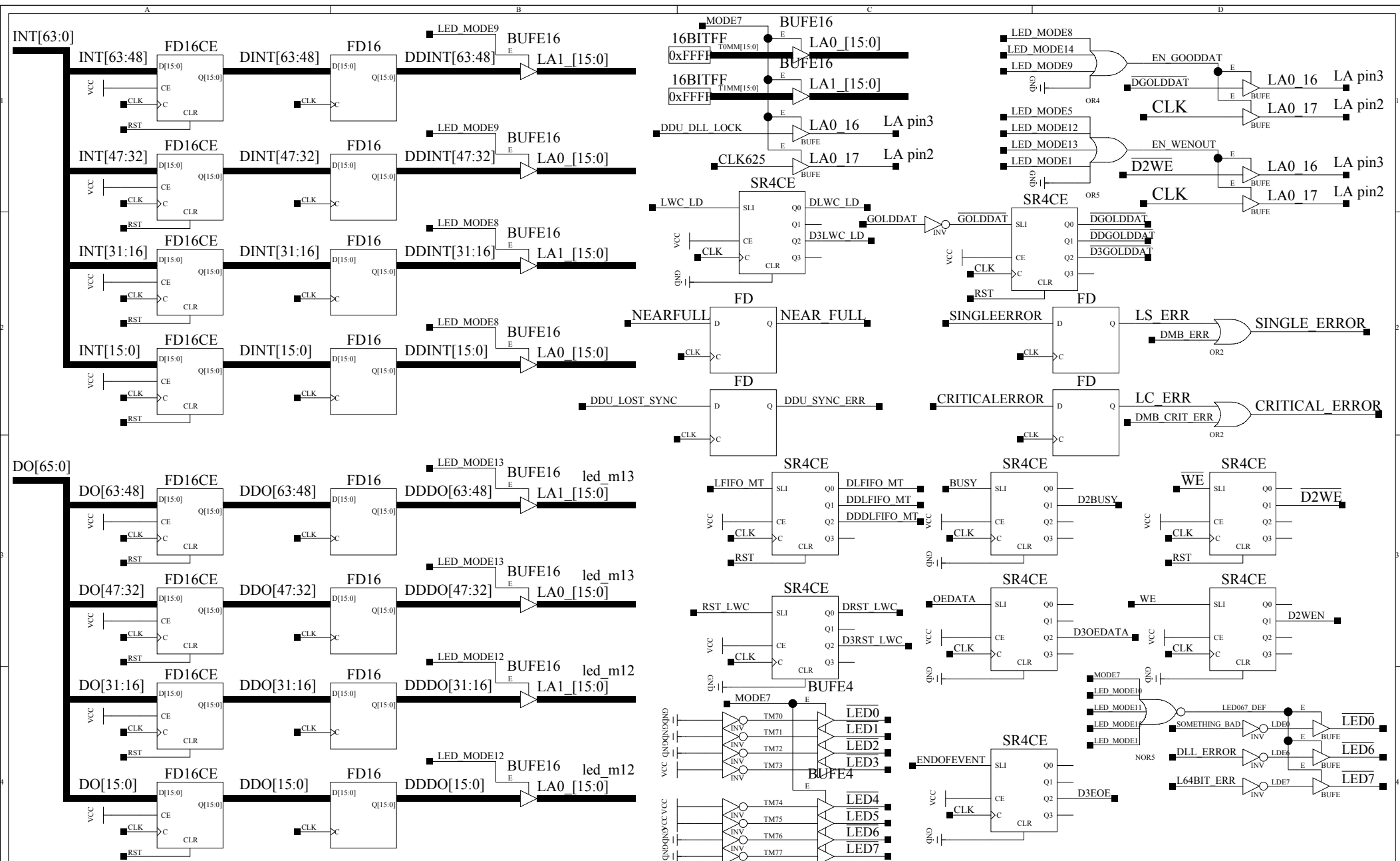
CSC_L1Err<--Bring to VME-JTAG Reg?

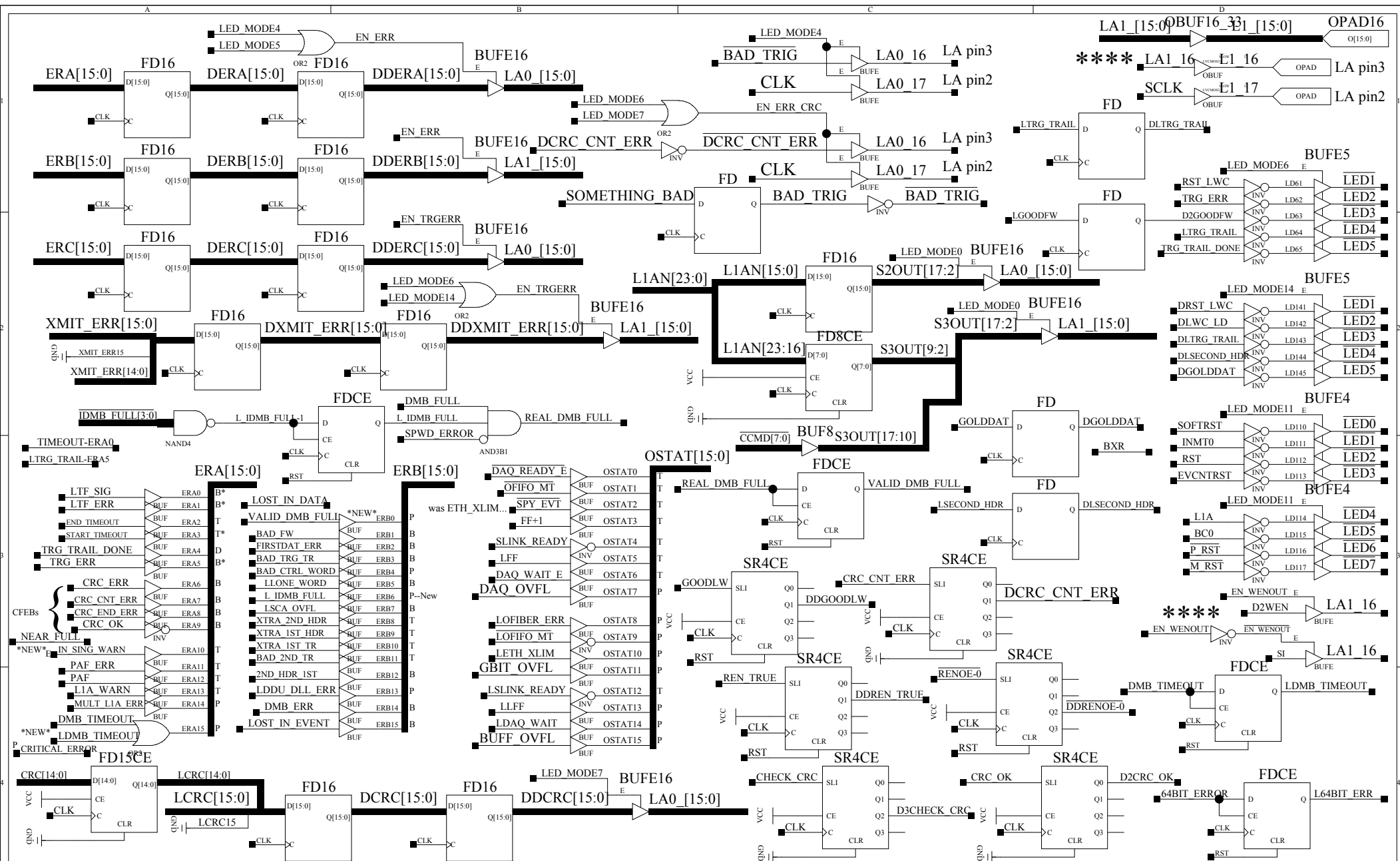


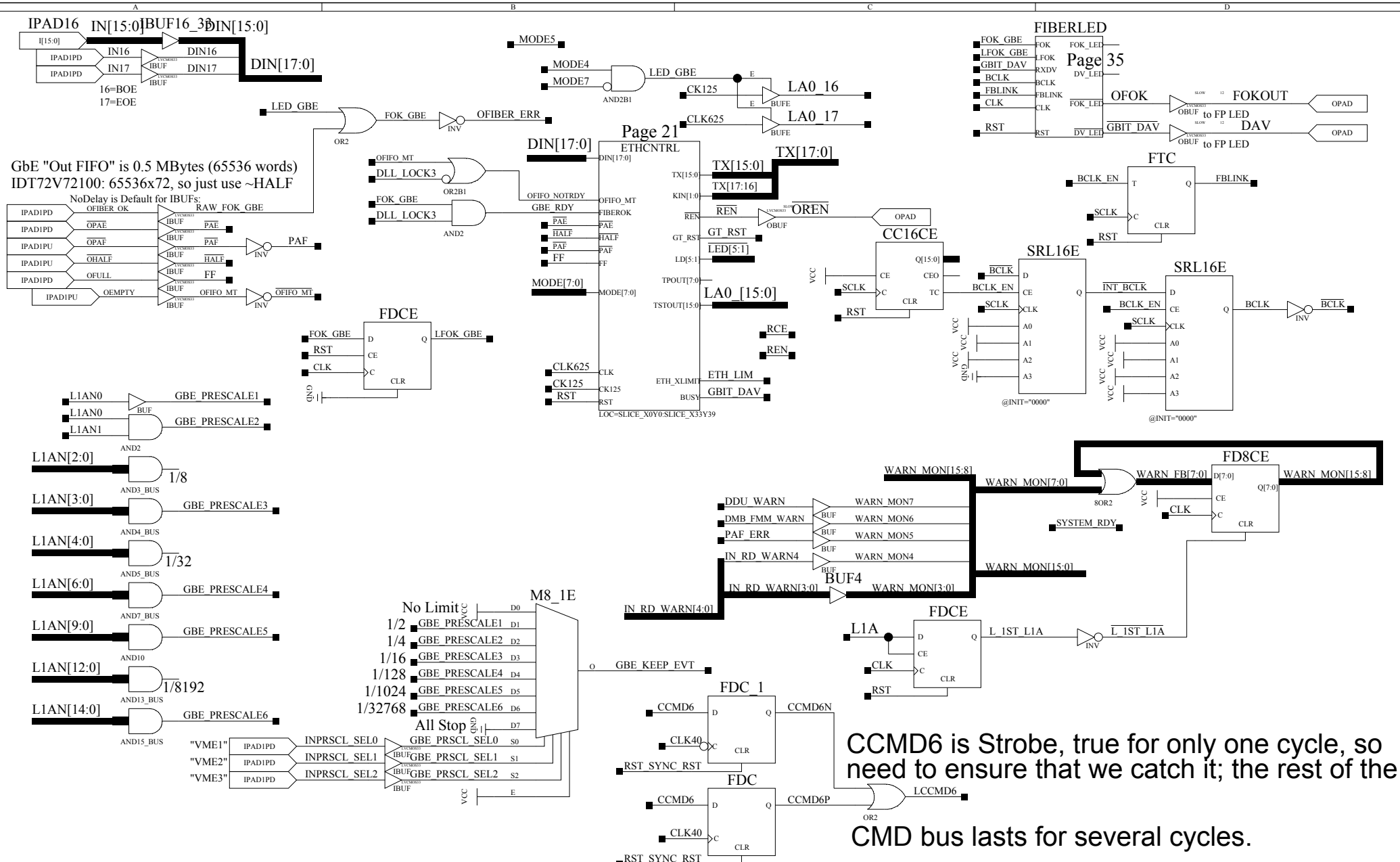
DMB Full signal detected
by an InFPGA InUnit

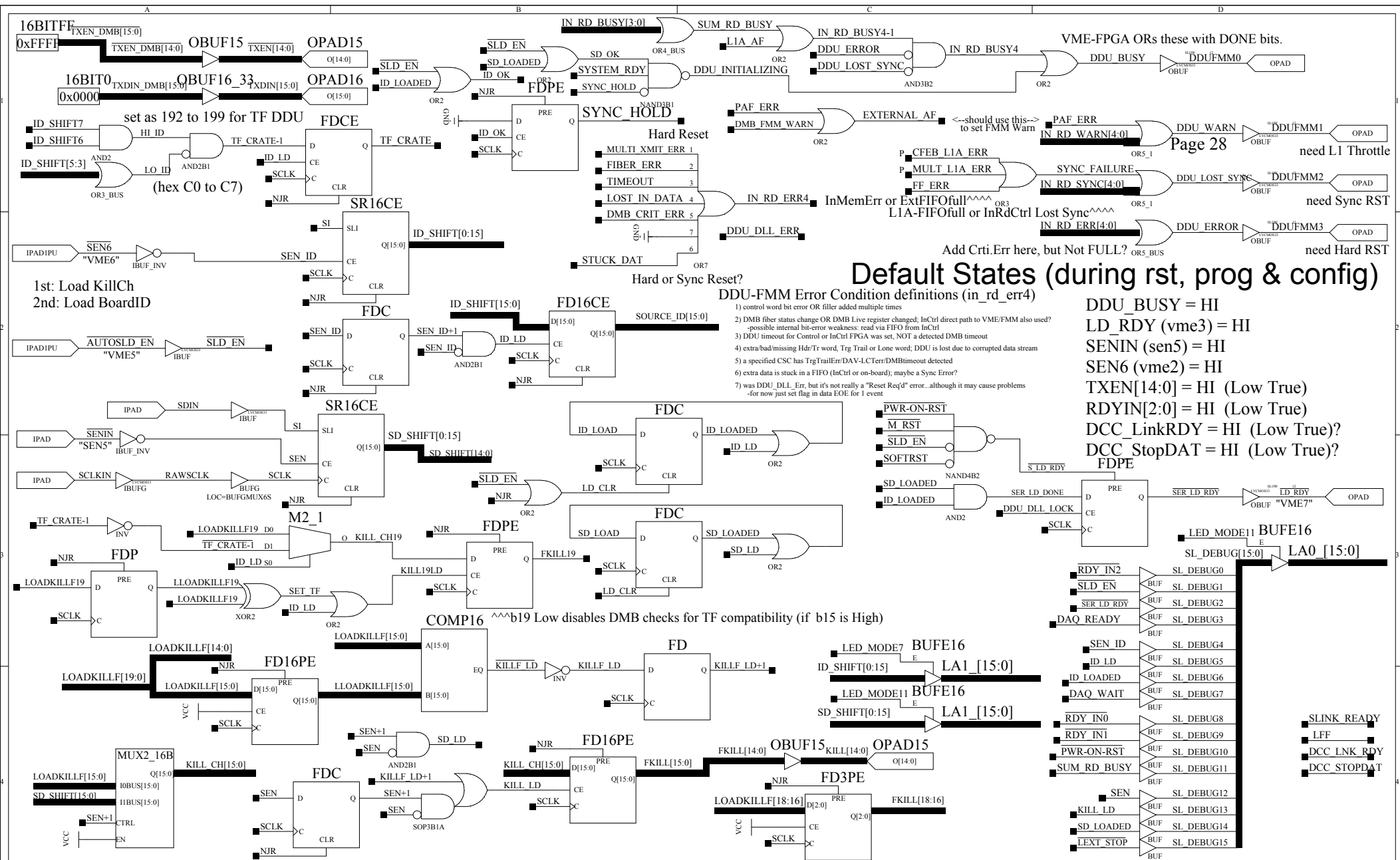




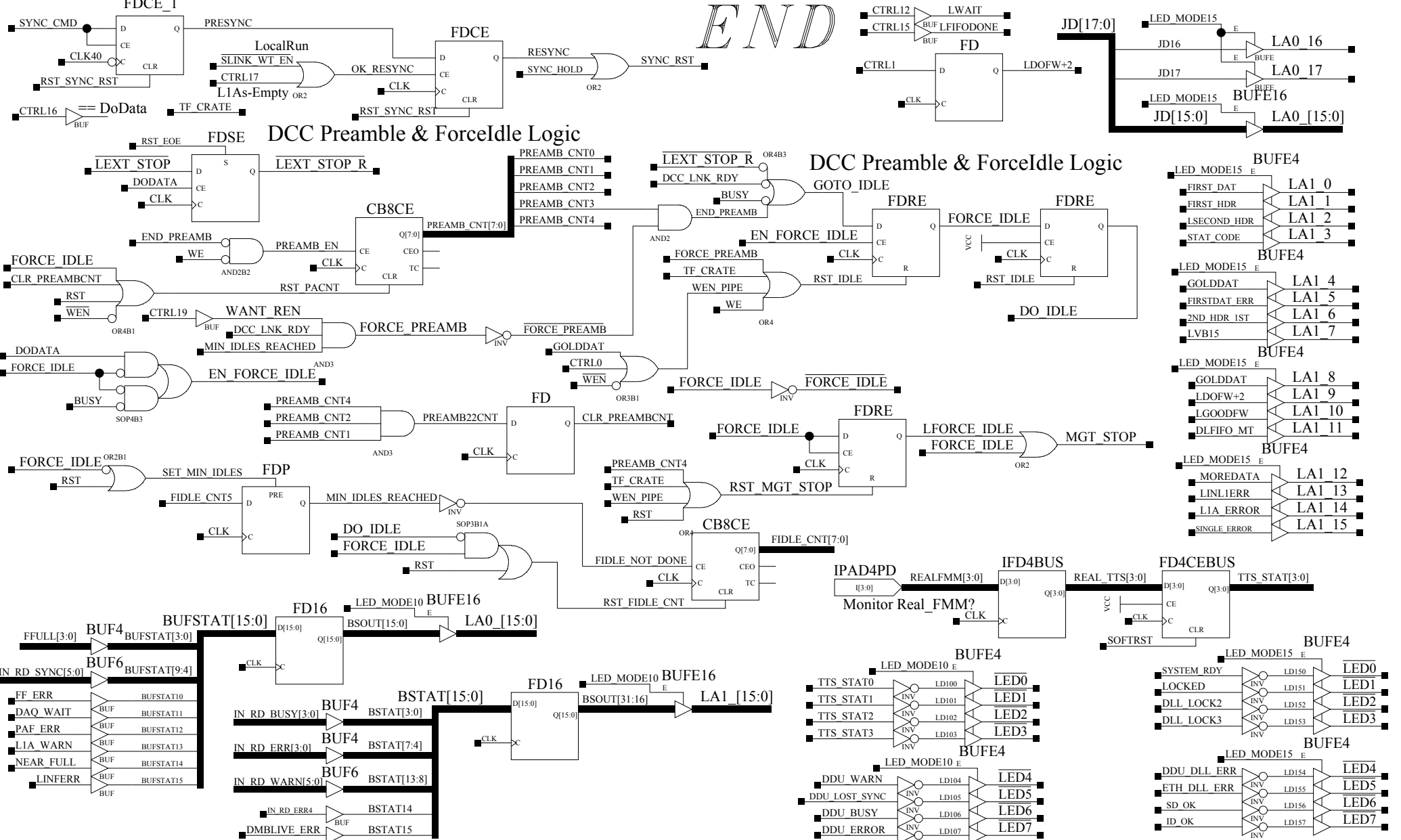






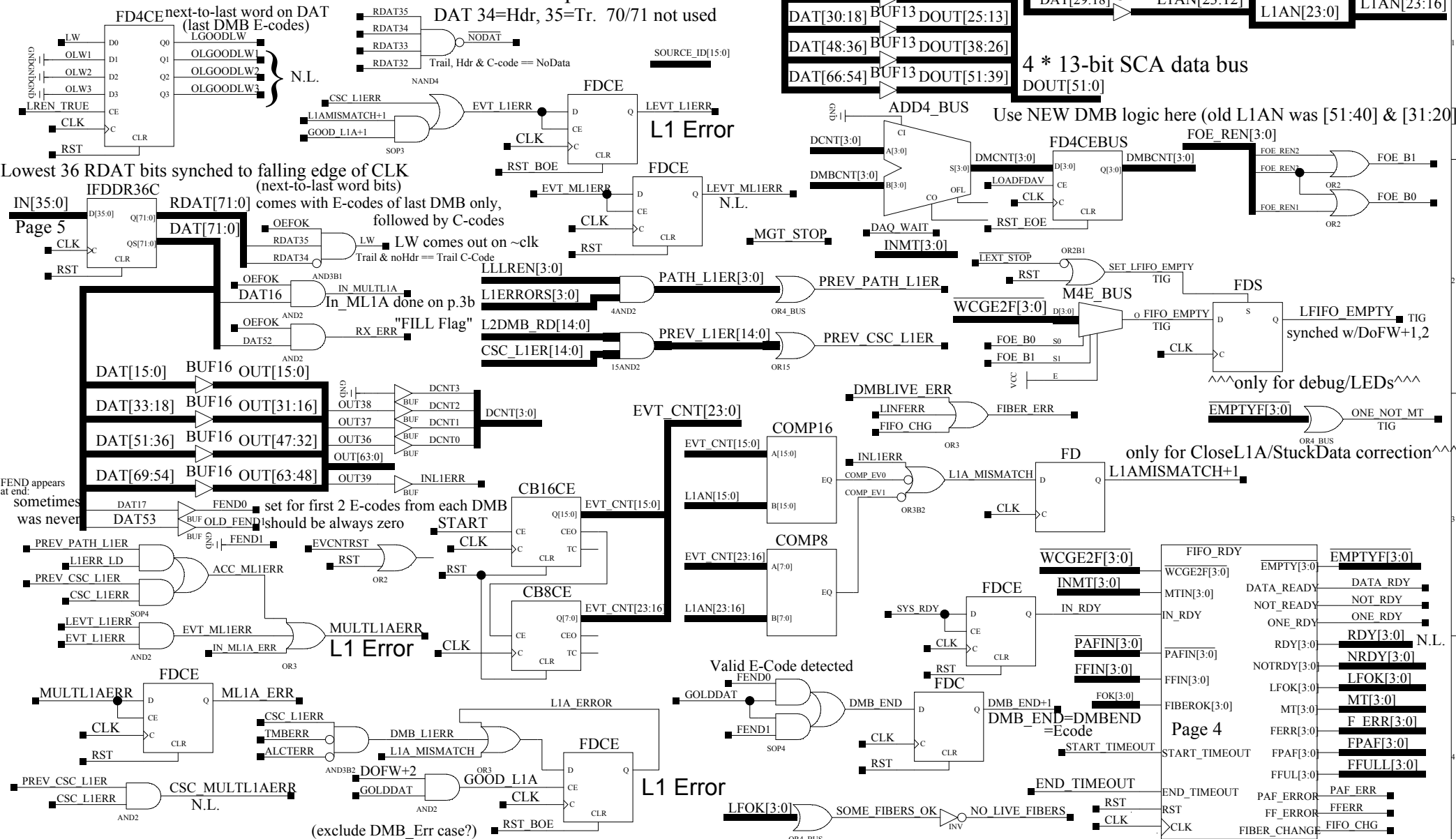


Logic for TFDDU, hold back the Resync until DDU completes all L1As (CTRL17) for Global runs. CTRL17 = DDU_Is_Empty

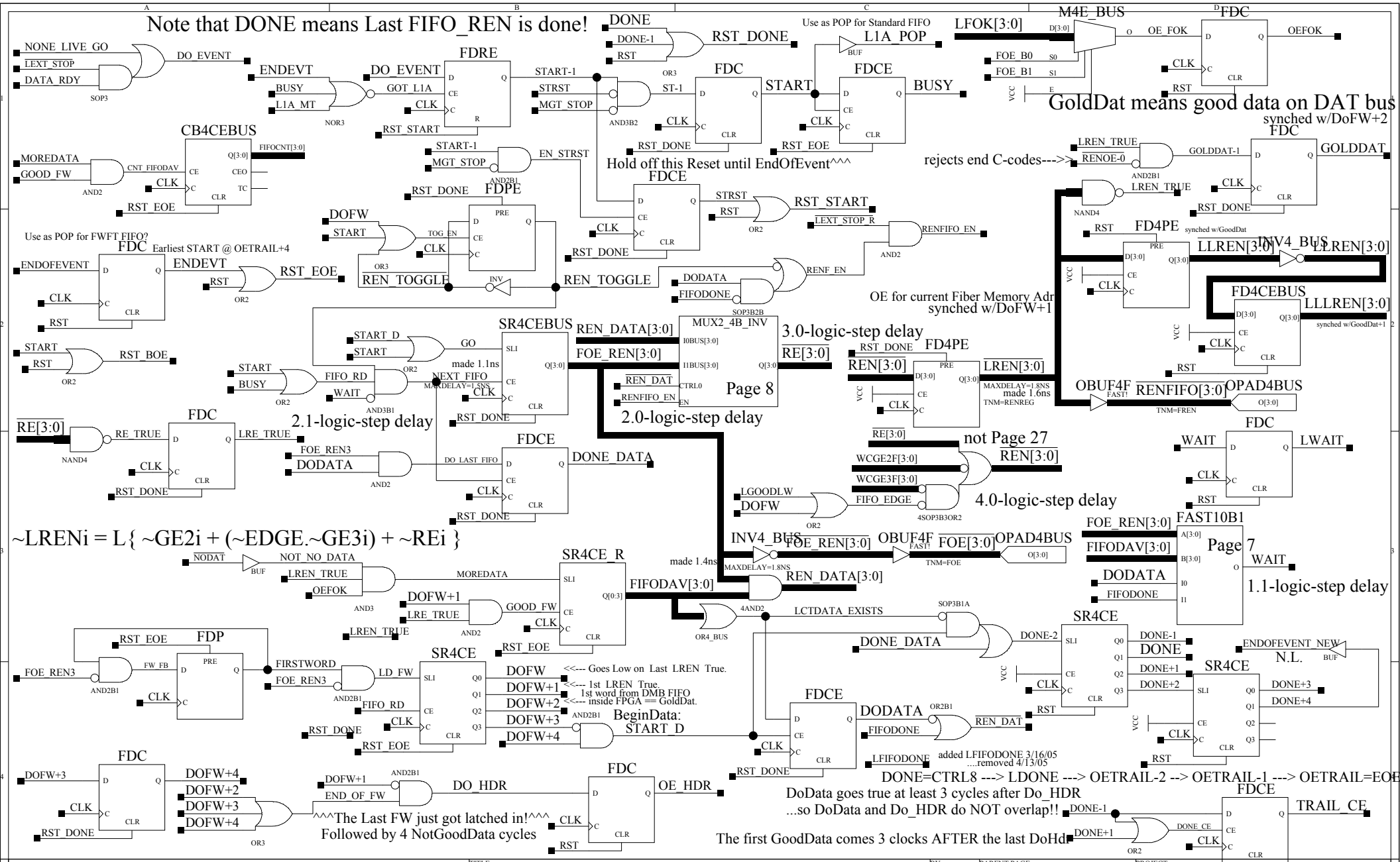


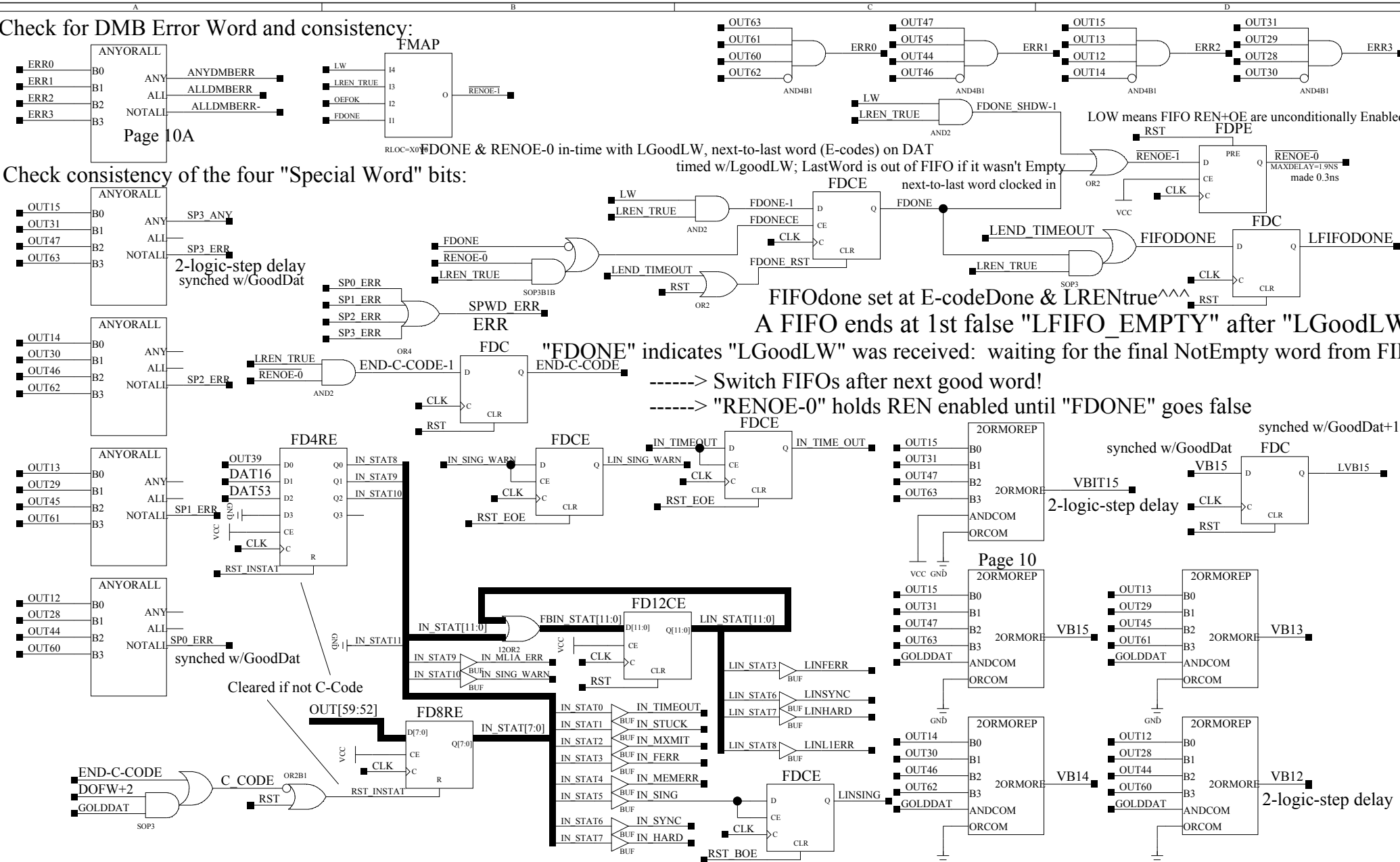
CLK $\wedge$ -- DIN[35:0] -- CLK $\vee$ -- Q[35:0] DIN[71:36] -- CLK $\wedge$ -- Q[71:36] QS[35:0]

Use these busses for CFEB CRC and Special Word checks-->



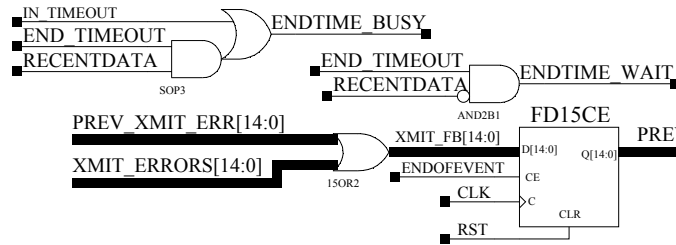
Note that DONE means Last FIFO_REN is done!



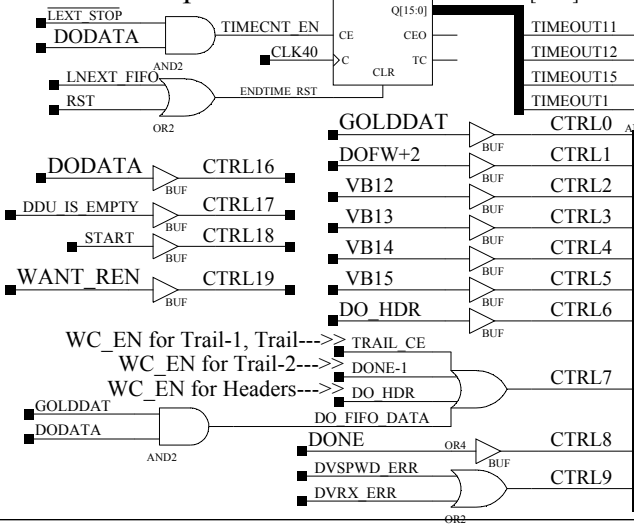


Control Bit List:

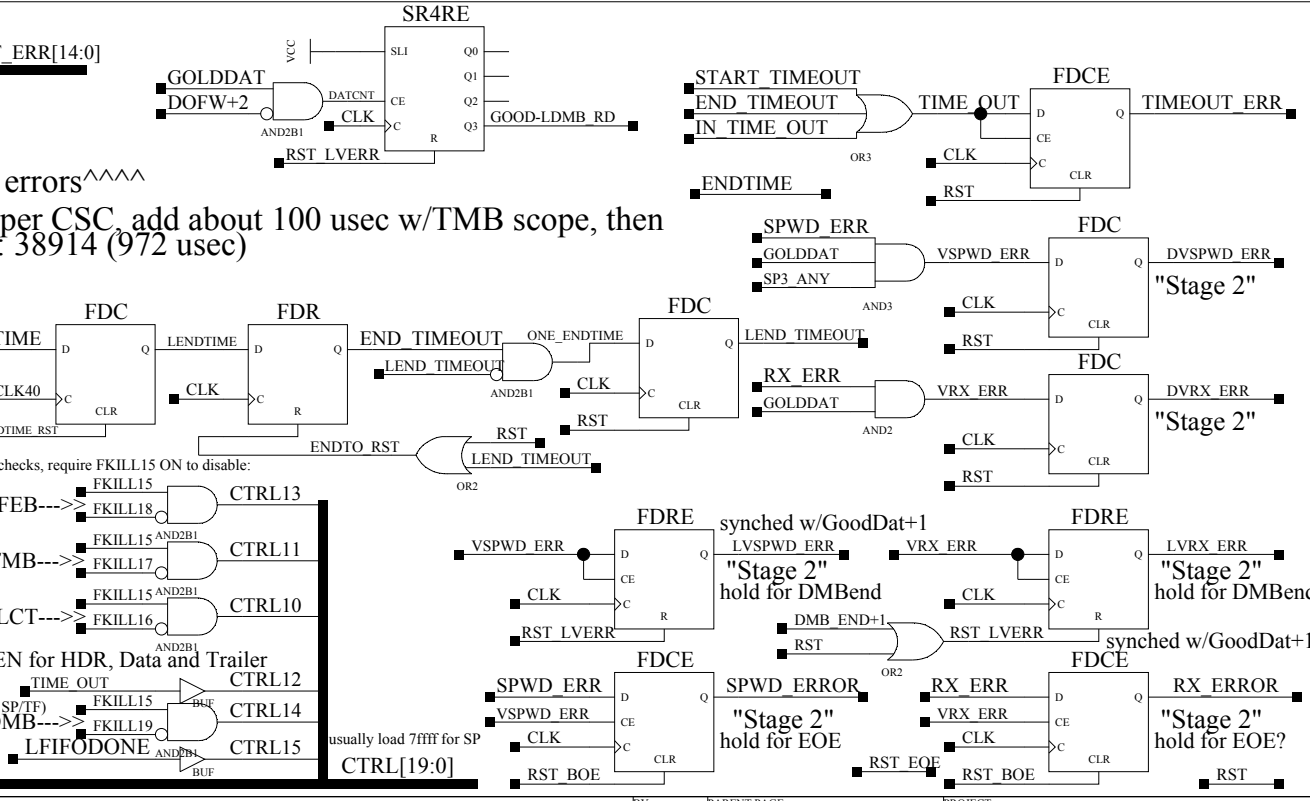
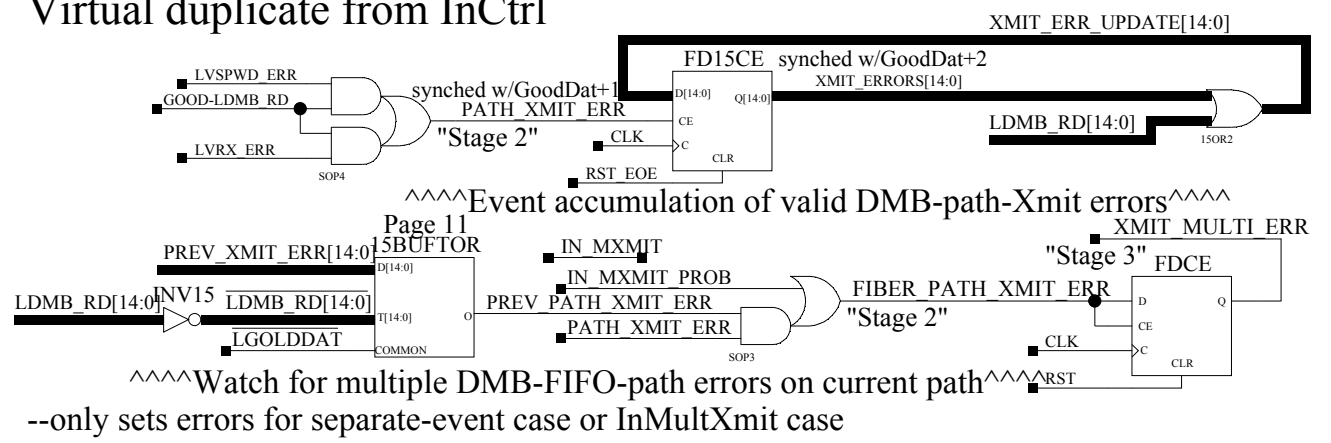
- 0: Gold Data (Active DMB has REN, OE, notMT, LFOK)
- 1: DMB First Word Mode
- 2: Latched Voted Special Bit 12 {2 or more out of 4}
- 3: Latched Voted Special Bit 13 {2 or more out of 4}
- 4: Latched Voted Special Bit 14 {2 or more out of 4}
- 5: Latched Voted Special Bit 15 {2 or more out of 4}
- 6: Do Header Mode (Header to Output)
- 7: Word Count Enable (DDU Header, DMB Data)
- 8: End of Event (DONE--->OETrail)



~~~~~Permanent accumulation of DMB-path-Xmit errors~~~~~  
FIFO Done Timeout: 132 usec=5281 is the worst case per CSC, add about 100 usec w/TMB scope, then 25ns clock period here  
another \*4 for 4 CSCs: 38914 (972 usec)

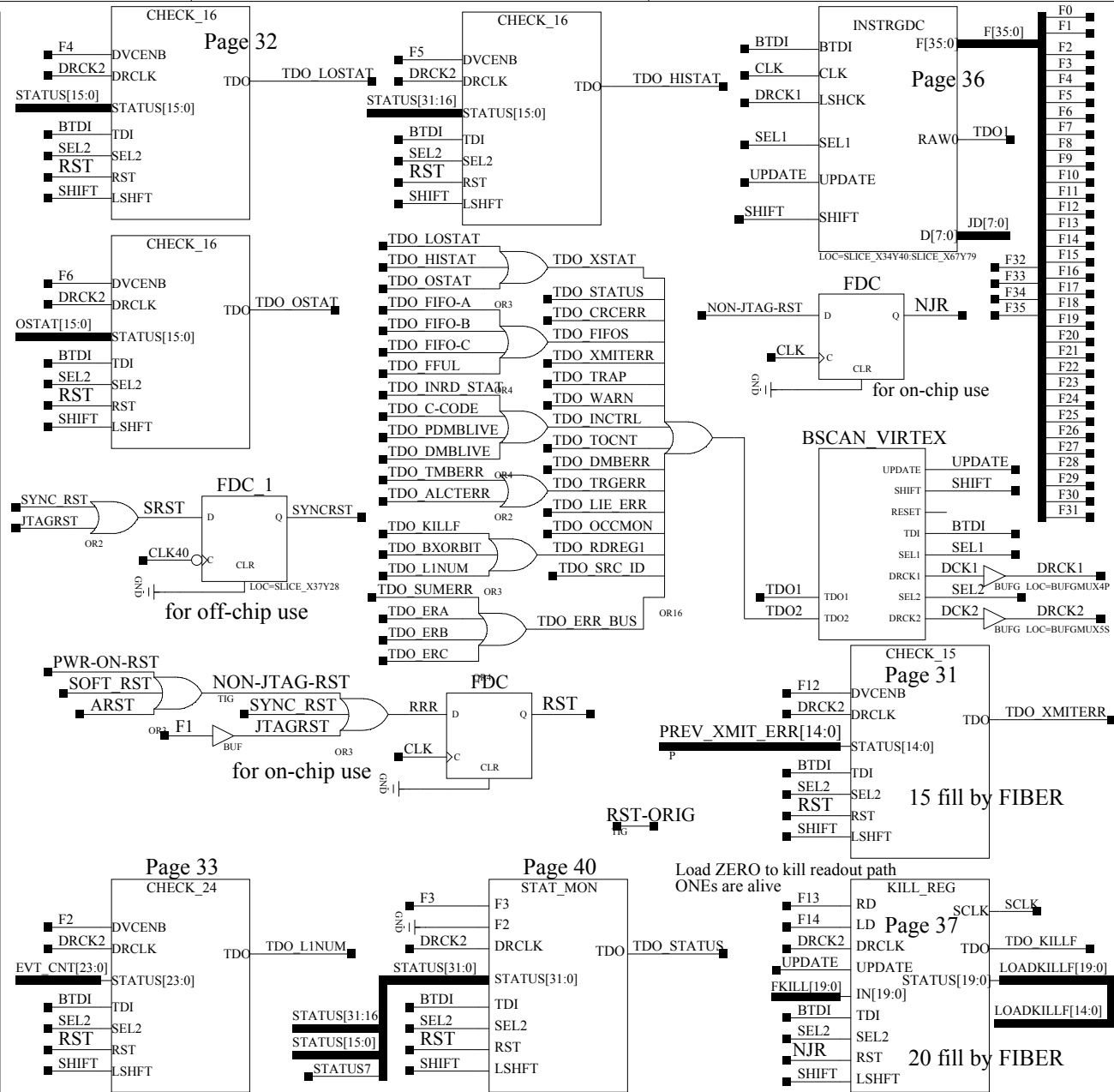


## Virtual duplicate from InCtrl

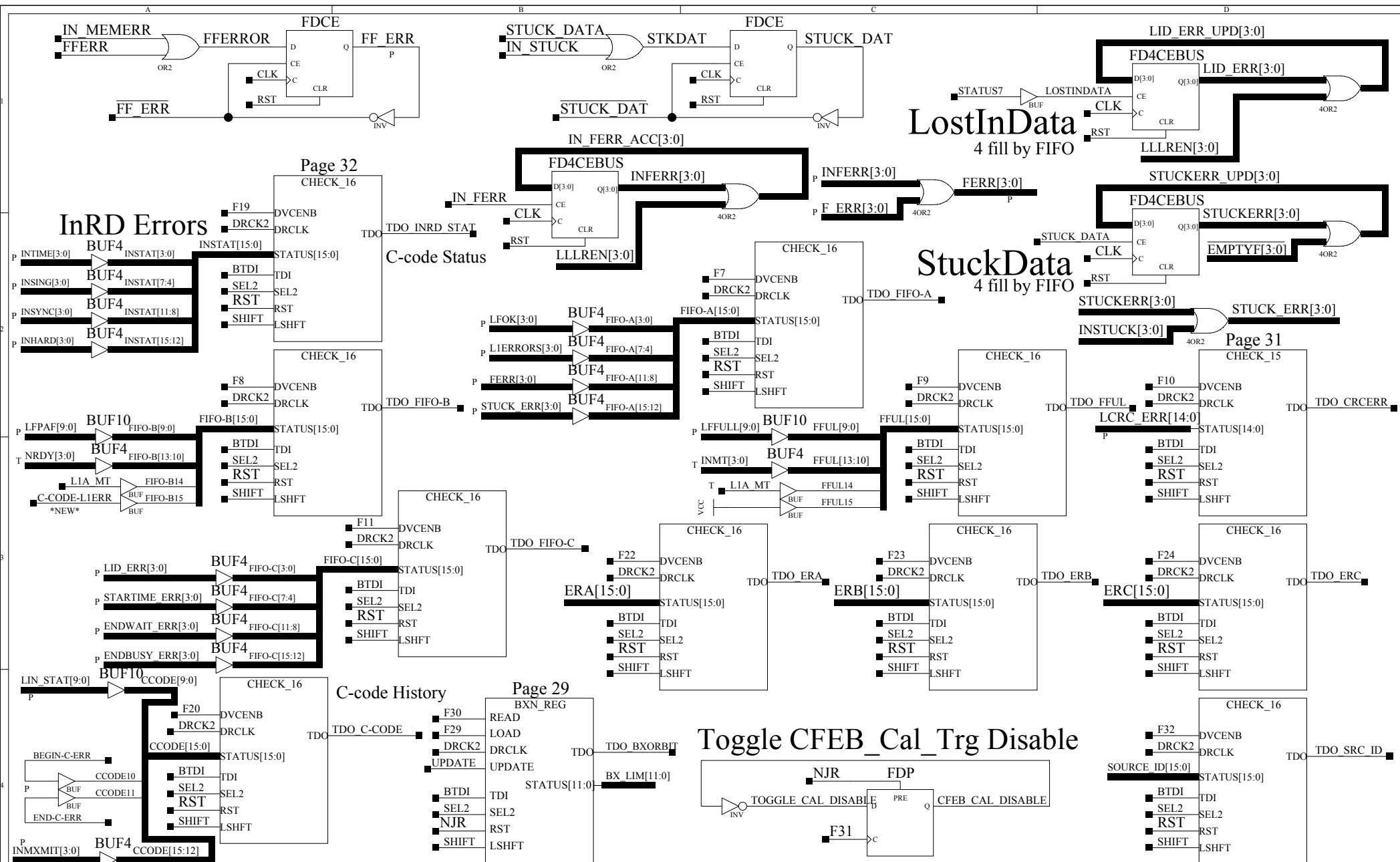


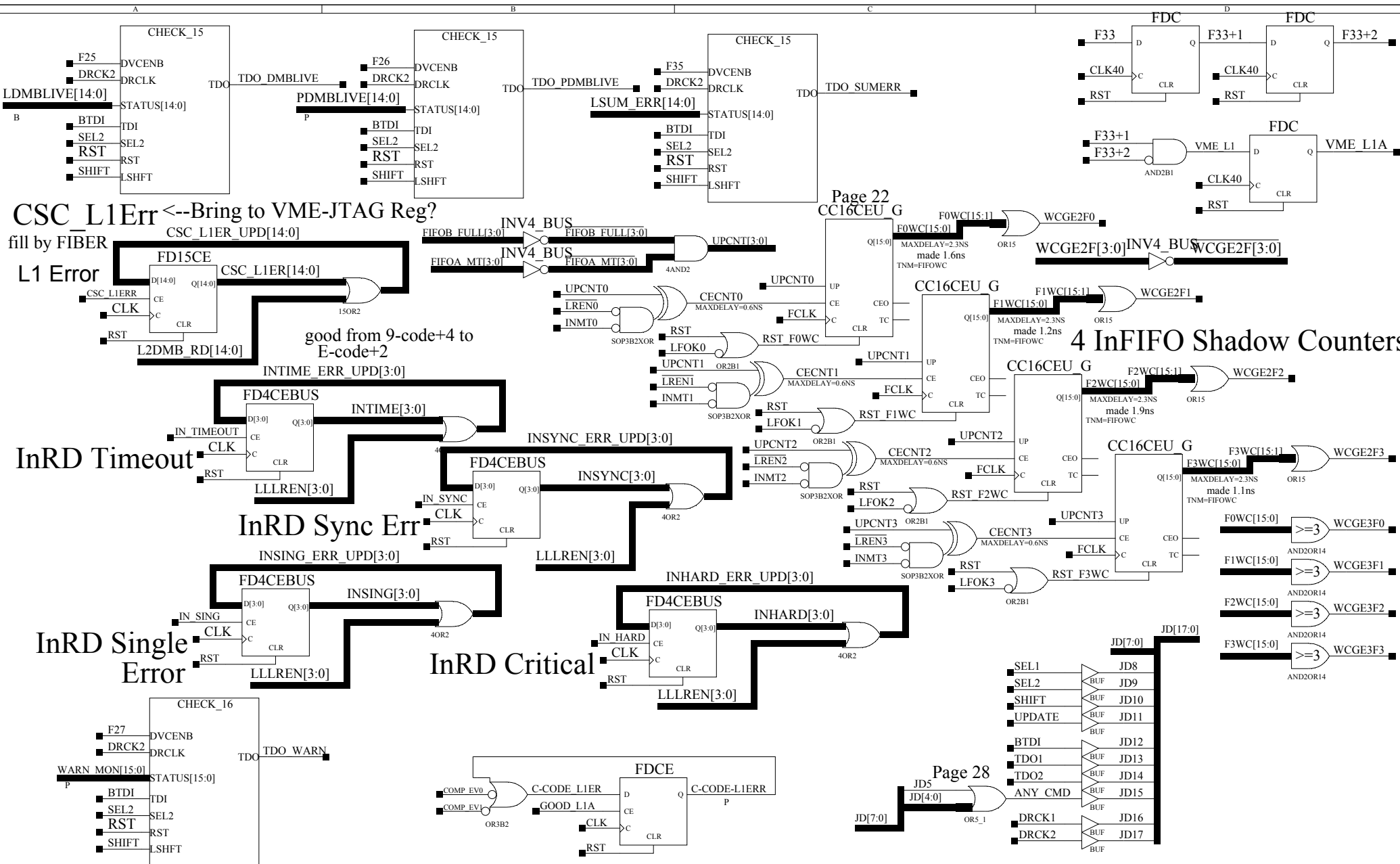
# JTAG Instruction Decode

| OpCode | Function                            | [OpName]                     |
|--------|-------------------------------------|------------------------------|
| 0      | No Operation                        | [NOOP]                       |
| 1      | FPGA Reset                          | [toggle]                     |
| 2      | Read Current DDU L1A Number         | [24-bit scaler]              |
| 3      | Check status (capture and shift)    | [32 bits]                    |
| 4      | Check status, low-word              | [16 bits]                    |
| 5      | Check status, high-word             | [16 bits]                    |
| 6      | Output Path Status                  | [16-bits]                    |
| 7a     | Check FOK (active input FIFOs)      | [lowest 4 bits]              |
| 7b     | L1A Mismatch (FIFO headers)         | [4-bits]                     |
| 7c     | Check FIFO Err (active FIFO change) | [4 bits]                     |
| 7d     | Stuck Data Errors (input FIFOs)     | [highest 4-bits]             |
| 8a     | Almost Full FIFOs                   | [lowest 10-bits]             |
| 8b     | FIFO Empty/GE2 Status               | [highest 6-bits]             |
| 9a     | Full FIFOs                          | [lowest 10-bits]             |
| * 9b   | Raw FIFO Empty                      | [highest 6-bits]             |
| 10     | CRC Errors                          | [15-bits]                    |
| 11a    | Lost In Data                        | [lowest 4-bits]              |
| 11b    | Timeout: start                      | [4-bits]                     |
| 11c    | Timeout: end-wait                   | [4-bits]                     |
| 11d    | Timeout: end-active                 | [highest 4-bits]             |
| 12     | Data Xmit Errors                    | [15-bits]                    |
| 13     | Check KILL_Register                 | [20 bits]                    |
| 14     | Load KILL_Register                  | [20 bits]                    |
| 15     | DMB Errors                          | [15-bits]                    |
| 16     | TMB Errors                          | [15-bits]                    |
| 17     | ALCT Errors                         | [15-bits]                    |
| 18     | Lost In Event                       | [15-bits]                    |
| * 19   | InRD Status                         | [16-bits]                    |
| * 20   | InRD C-code & MxmitErr History      | [16-bits]                    |
| * 21   | Critical Error Trap Reg.            | [192 bits]                   |
| 22     | Error Register A                    | [16-bits]                    |
| 23     | Error Register B                    | [16-bits]                    |
| 24     | Error Register C                    | [16-bits]                    |
| 25     | Read DMB_LIVE                       | [15-bits]                    |
| 26     | Read P_DMB_LIVE                     | [15-bits]                    |
| 27     | Read WARN_MON                       | [16-bits]                    |
| * 28   | Max Timeout Count                   | [16-bits]                    |
| 29     | Set BX per Orbit                    | [12-bits]                    |
| 30     | Read BX per Orbit                   | [12-bits]                    |
| 31     | Toggle CFEb_Cal Auto_L1             | [default enable]             |
| 32     | Read DDU Source ID                  | [16-bits]                    |
| 33     | DDU-only VME_L1A                    |                              |
| * 34   | Read CSC Board Occupancy scalers    | (loops for 60 words, 32-bit) |
| 35     | Sum of Errors for each CSC          | [15-bits]                    |



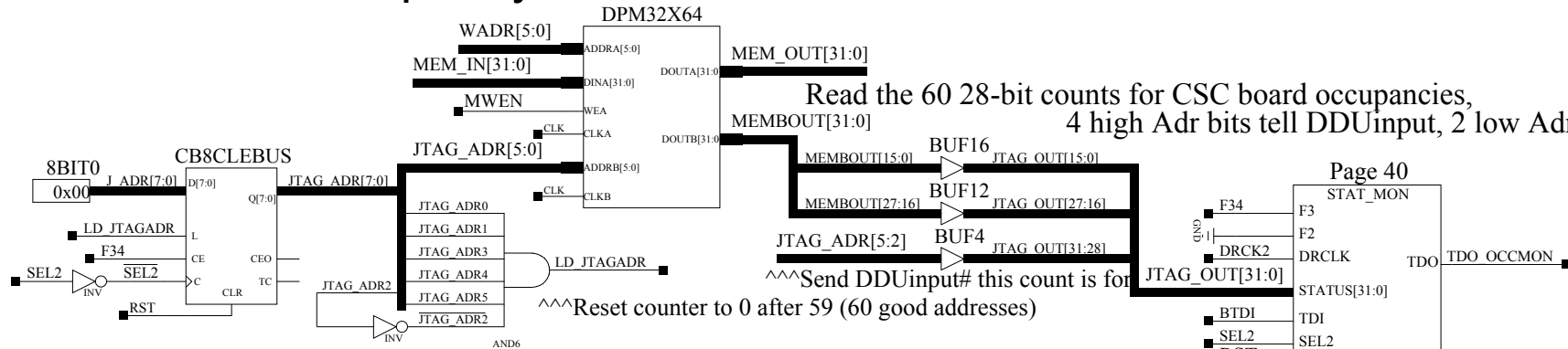






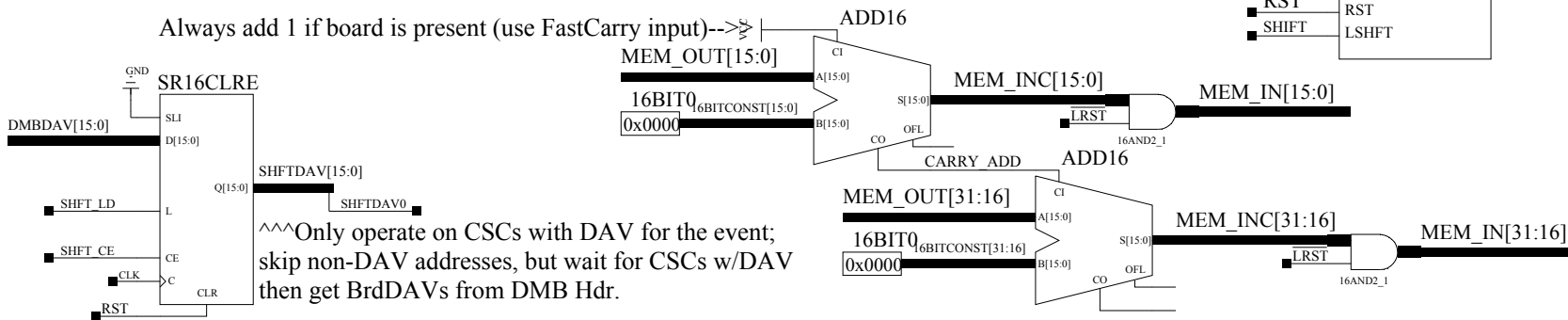


# CSC Board Occupancy Tracker: 15 fibers x 4-boards each



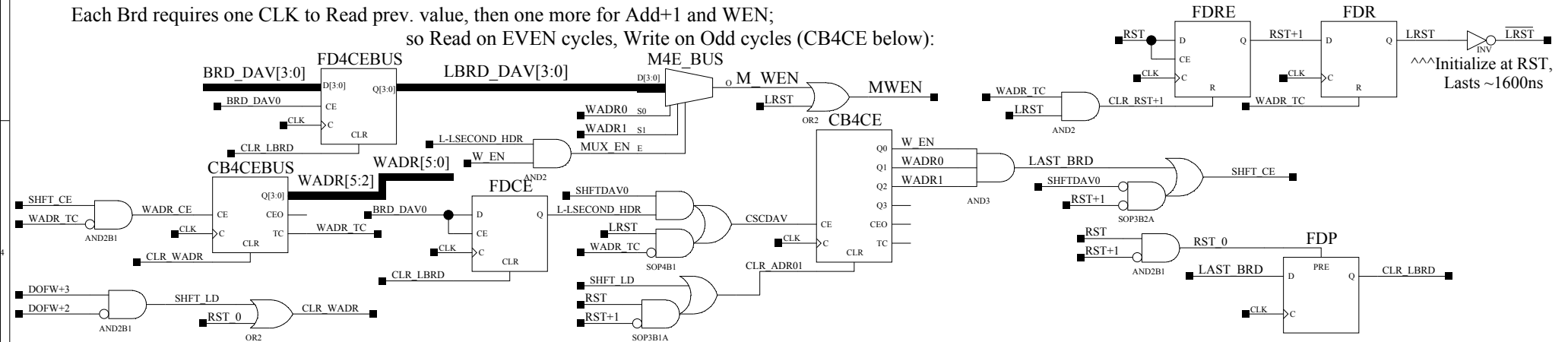
0 = DMB  
1 = ALCT  
2 = TMB  
3 = CFEB

Always add 1 if board is present (use FastCarry input)--> 8



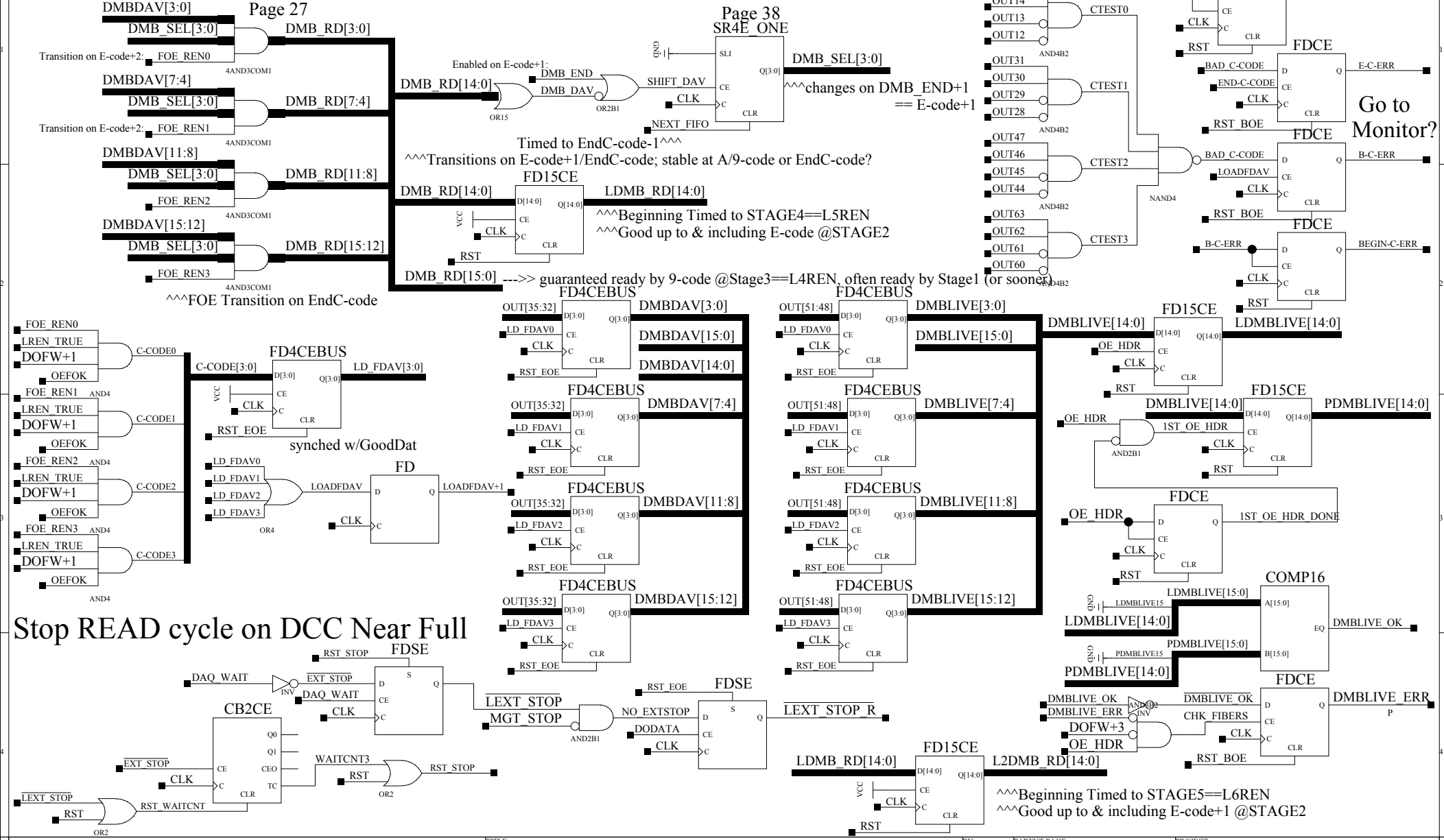
^^^Only operate on CSCs with DAV for the event;  
skip non-DAV addresses, but wait for CSCs w/DAV  
then get BrdDAVs from DMB Hdr.

Each Brd requires one CLK to Read prev. value, then one more for Add+1 and WEN;  
so Read on EVEN cycles, Write on Odd cycles (CB4CE below):

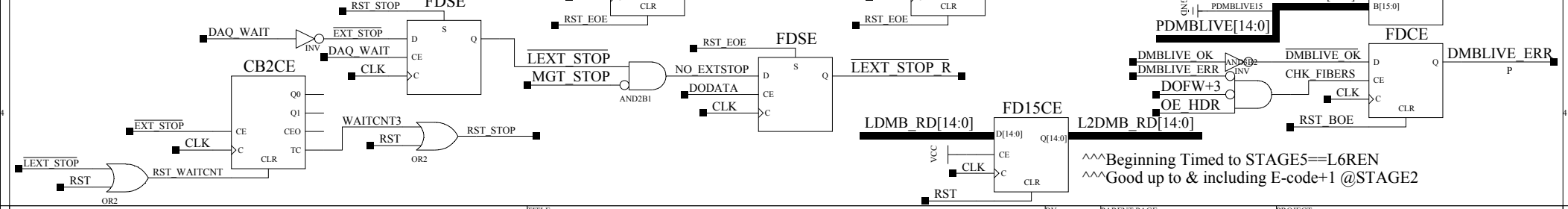


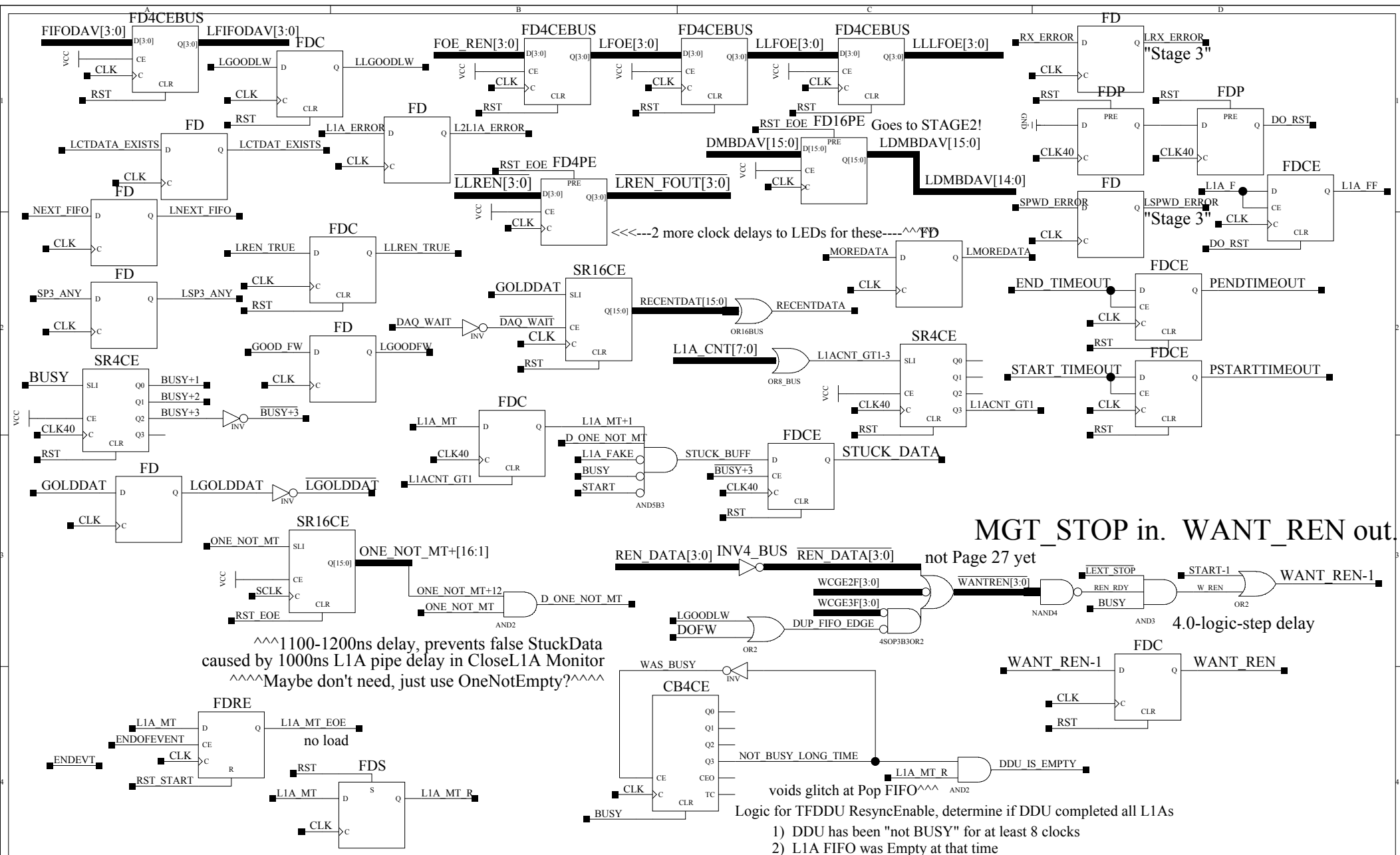
^^^Initialize at RST,  
Lasts ~1600ns

# Use DMB\_RD to determine which FIBER we're currently reading



## Stop READ cycle on DCC Near Full

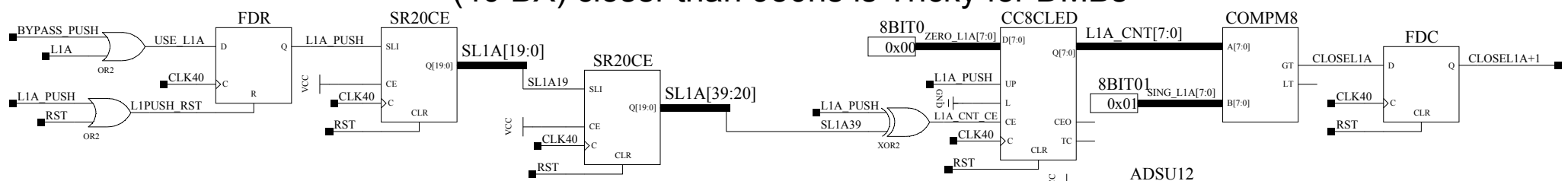




END

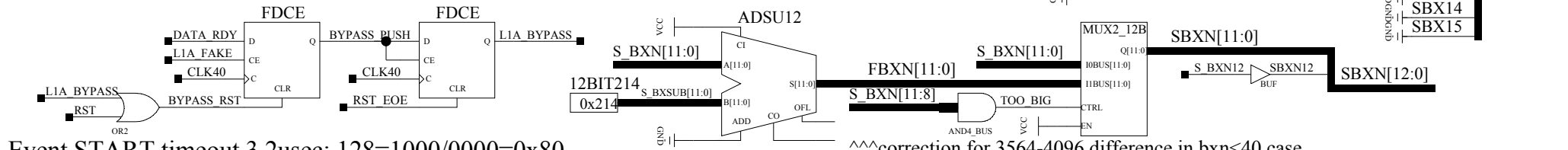
# L1A Proximity Tracker: 1000ns Close L1A Monitor

## (40 BX) closer than 950ns is Tricky for DMBs

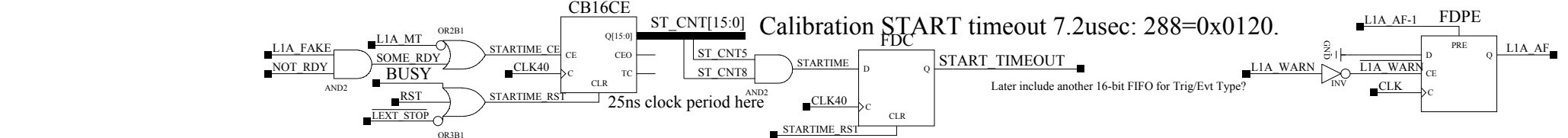


Pipe all L1As for 1000ns, if more than 1 then set CloseL1A bit^^^

Finally, perform BX-40 to correct BXN and store CloseL1A as BXN bit-12 (& correct for BX<40 case). Then use SBXN12 output (Close\_L1A ) for Stage2 DMB checks: 1000+ ns L1As means that first 2 CFEB samples should always have good L1A#



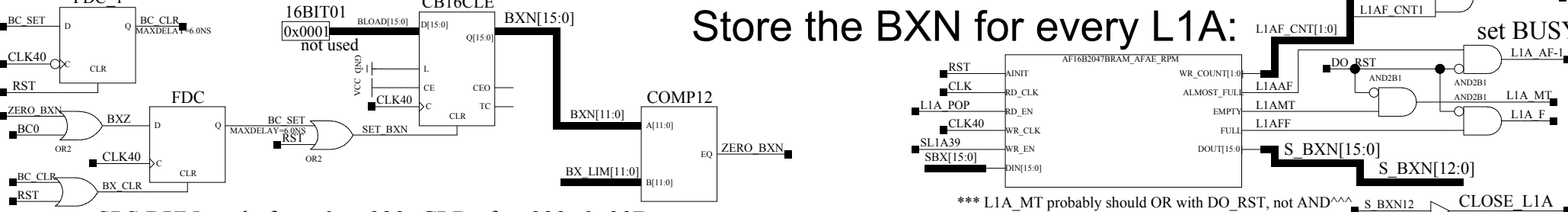
Event START timeout 3.2usec:  $128=1000/0000=0x80....$  ^^correction for 3564-4096 difference in bxn<40 case



LHC BXN cycles from 0 to 3563

Set to BX=0 one cycle after BX LIM:  $3563=1101/1110/1011=0xDEB$

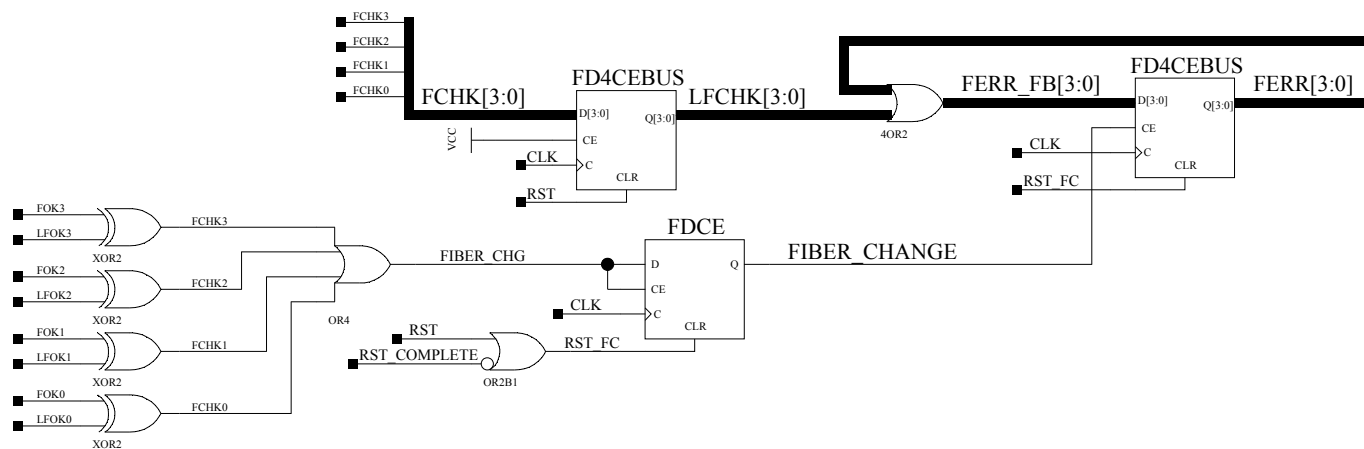
Calibration START timeout 7.2usec:  $288=0x0120$ .



SPS BXN cycle from 0 to 923: CLR after 923=0x39B.

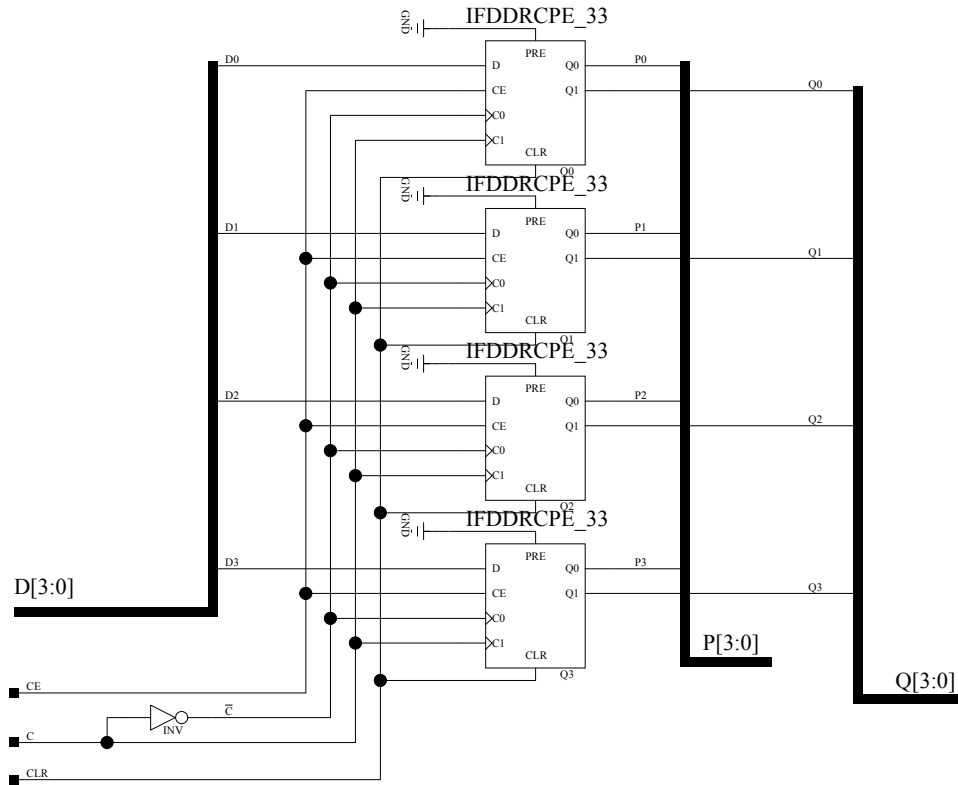
\*\*\* L1A\_MT probably should OR with DO\_RST, not AND^^^







drawn by KS  
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Title: VIRTEX Family IFDDR4CE Macro, LVCMOS33

Comments: 4-Bit Double-Data-Rate Input Register w/  
Clock Enable & Asynchronous Clr

Date: 10th December 2003

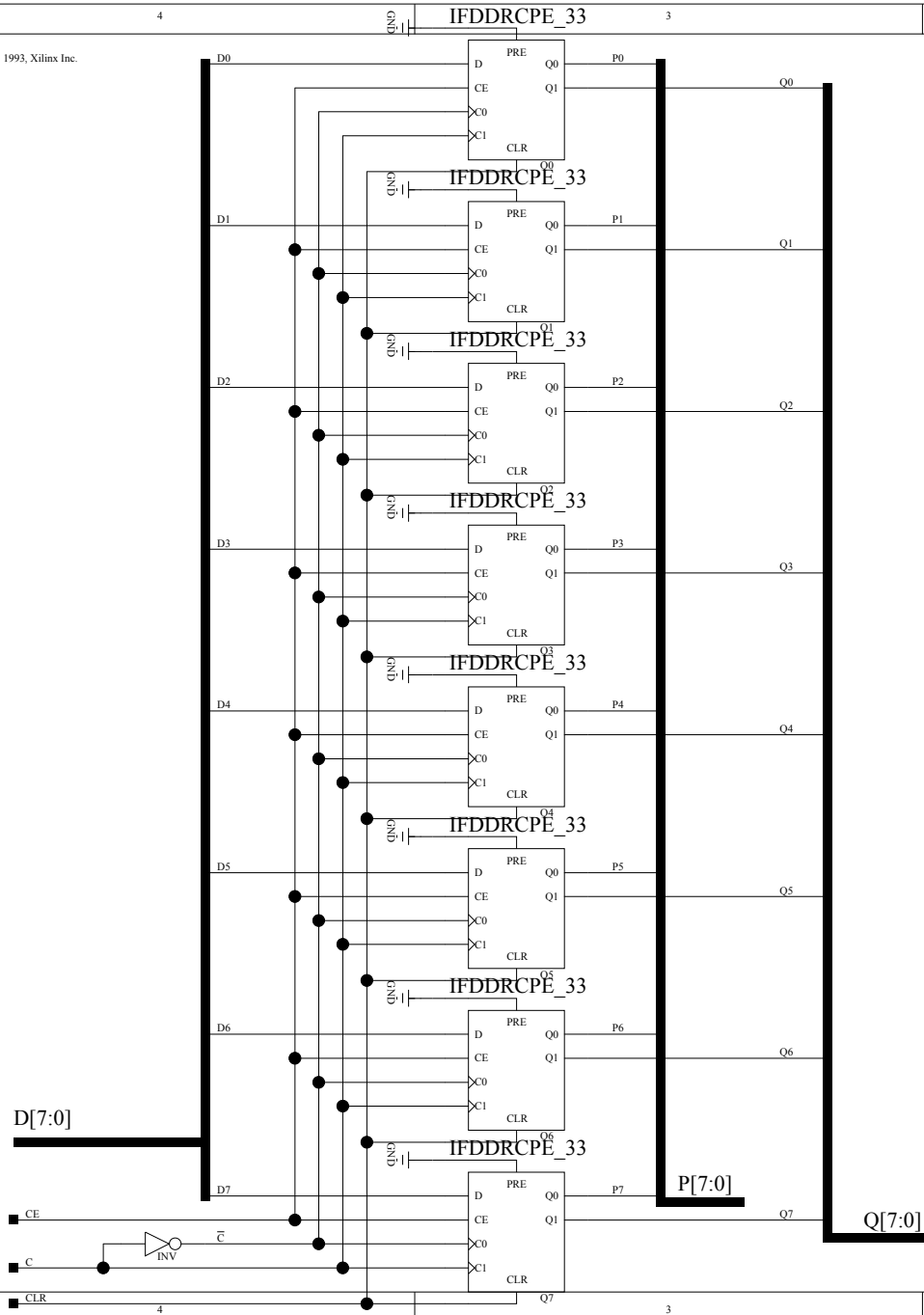
Sheet Size: B

Ver: 1

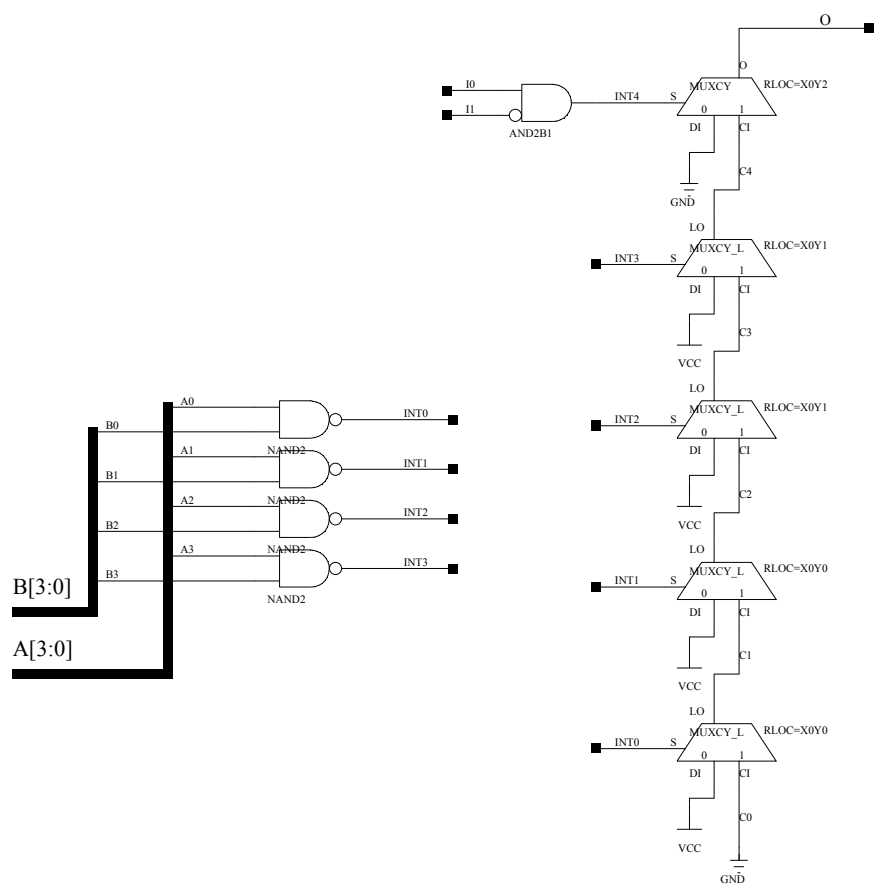
Rev: A

JRG

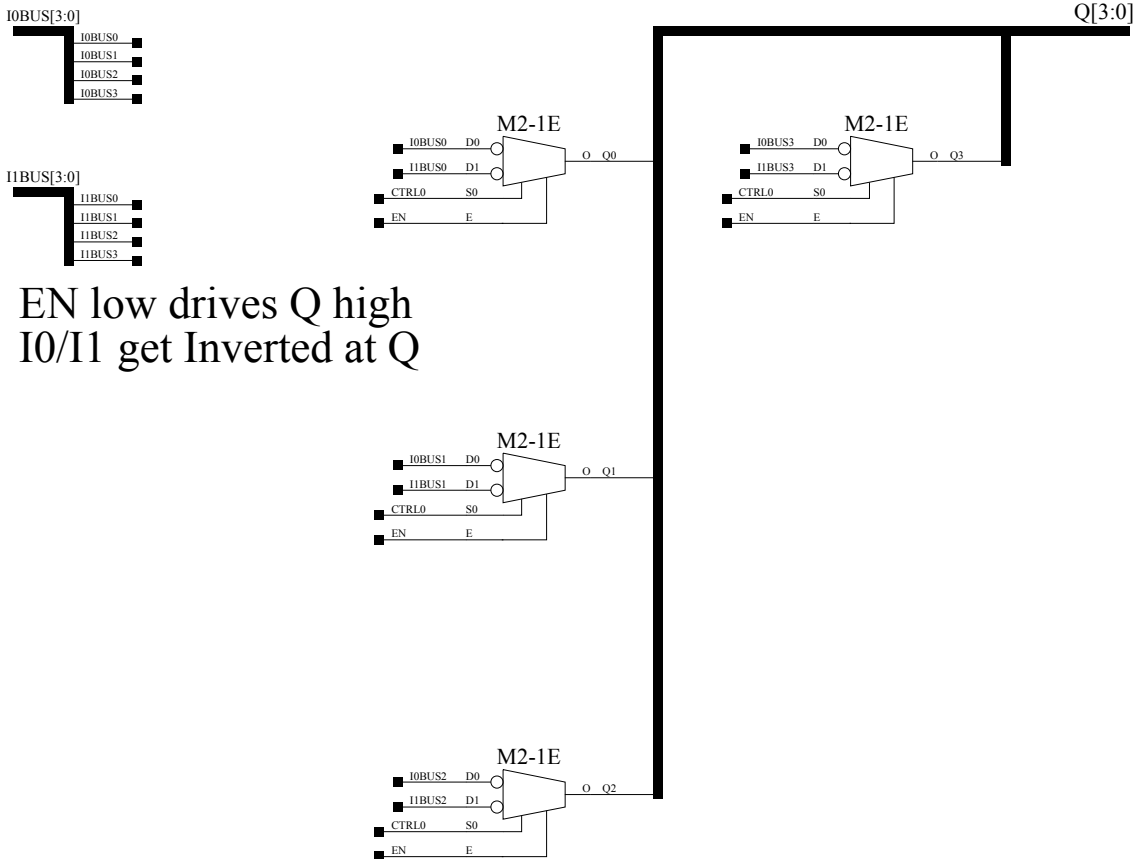
drawn by KS  
Copyright (c) 1993, Xilinx Inc.

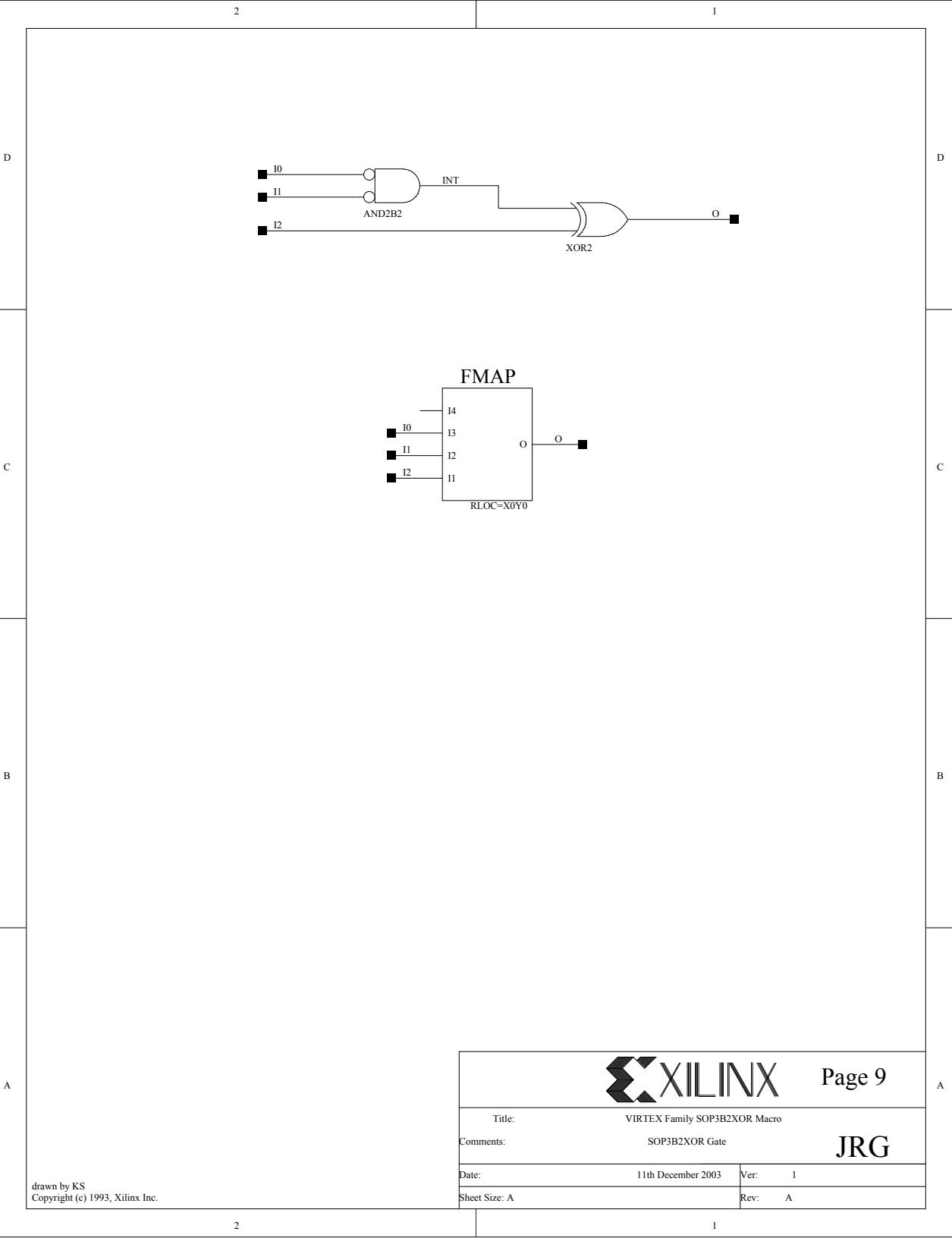


|                                                                                       |                    |                                                                             |   |
|---------------------------------------------------------------------------------------|--------------------|-----------------------------------------------------------------------------|---|
|  |                    |                                                                             |   |
| Title:                                                                                |                    | VIRTEX Family IFDDR8SCE Macro, LVCMOS33                                     |   |
| Comments:                                                                             |                    | 8-Bit Double-Data-Rate Input Register w/<br>Clock Enable & Asynchronous Clr |   |
| Date:                                                                                 | 10th December 2003 | Ver:                                                                        | 1 |
| Sheet Size:                                                                           | B                  | Rev:                                                                        | A |



|                                                                                       |                   |                                                                                                 |   |
|---------------------------------------------------------------------------------------|-------------------|-------------------------------------------------------------------------------------------------|---|
|  |                   | JRG                                                                                             |   |
| Title:                                                                                |                   | FAST10B1                                                                                        |   |
| Comments:                                                                             |                   | Custom Fast, Complex Logic for DDU, use 4 MUXCY as OR, 1 as AND similar to: OR of 4 AND2 AND2B1 |   |
| Date:                                                                                 | 15th October 2003 | Ver:                                                                                            | 1 |
| Sheet Size:                                                                           | B                 | Rev:                                                                                            | A |

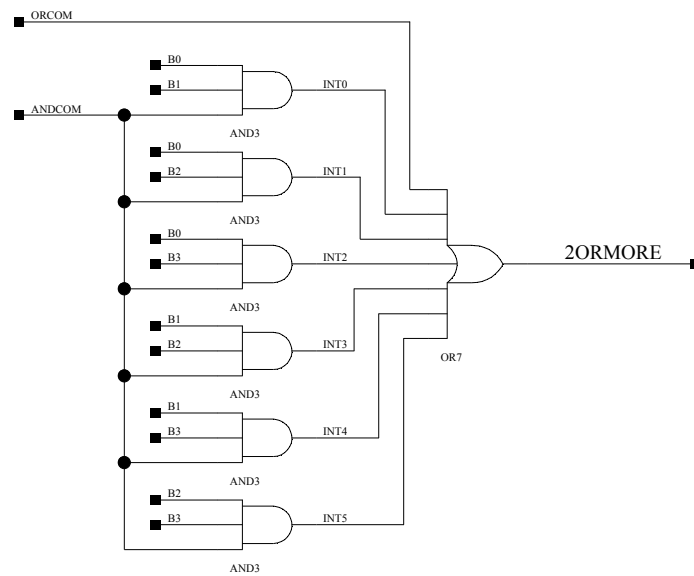


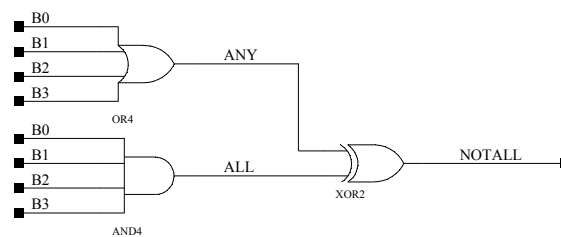


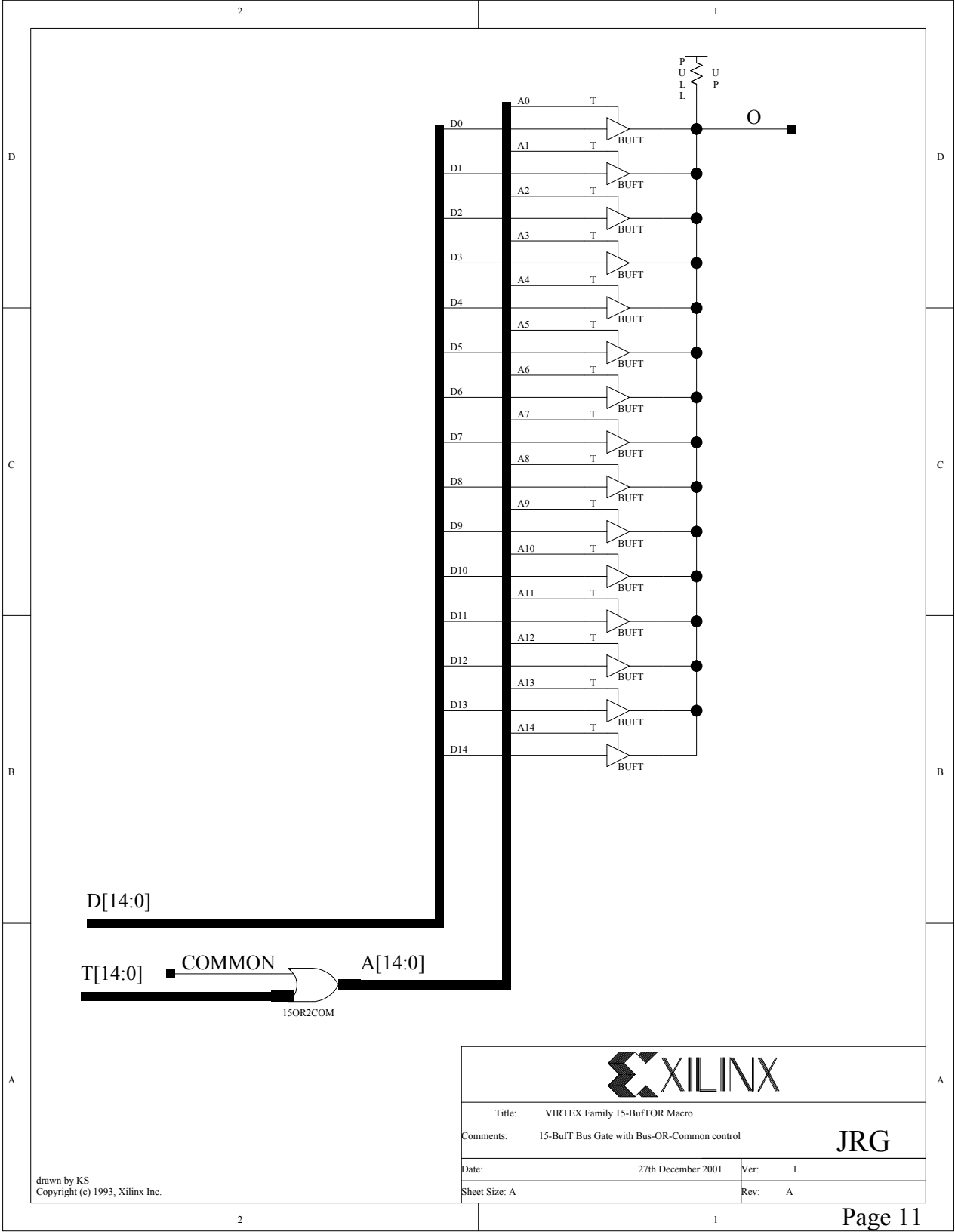
Page 9

|               |                               |        |
|---------------|-------------------------------|--------|
| Title:        | VIRTEX Family SOP3B2XOR Macro |        |
| Comments:     | SOP3B2XOR Gate                |        |
| Date:         | 11th December 2003            | Ver: 1 |
| Sheet Size: A | Rev: A                        |        |

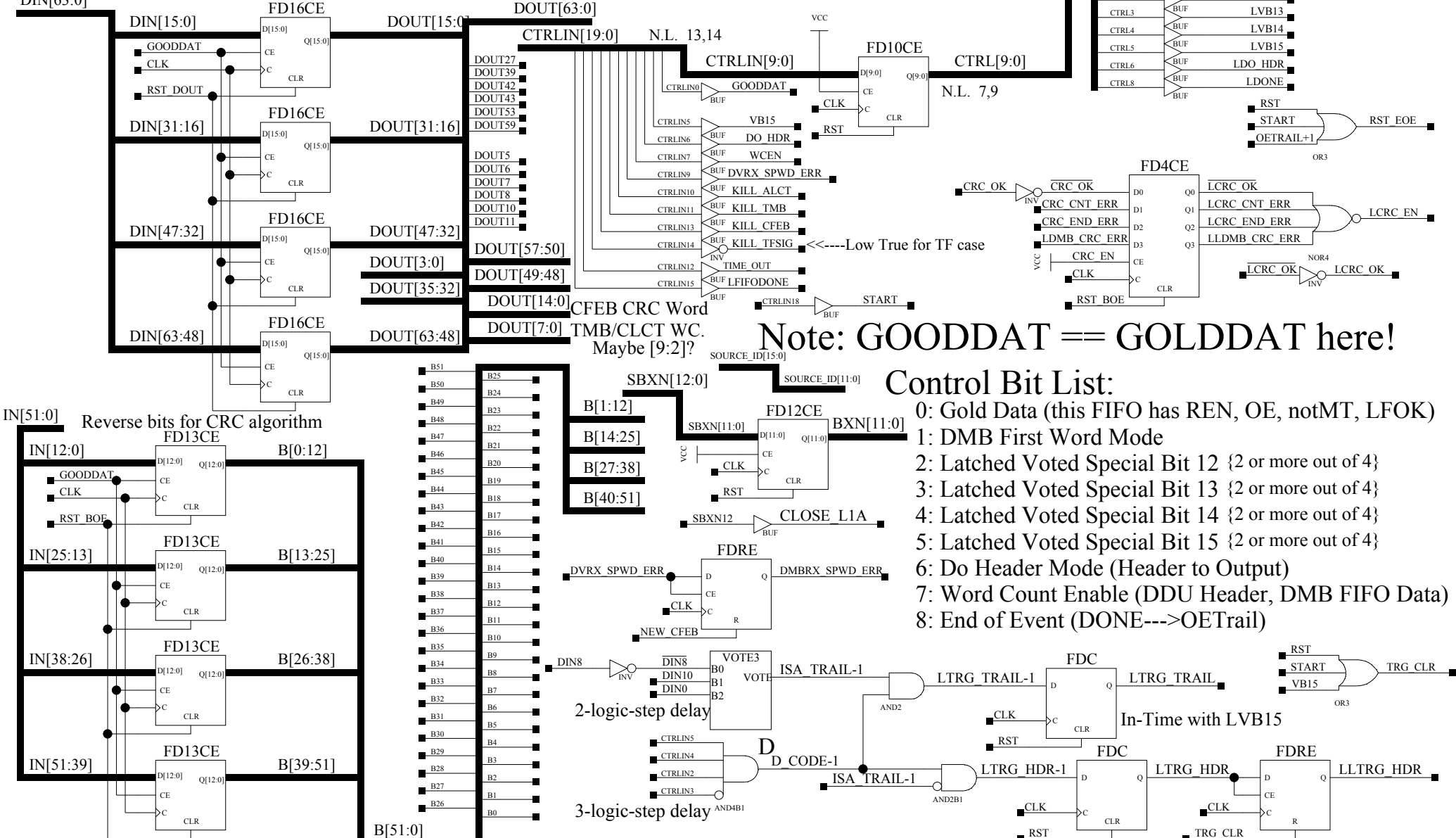
JRG







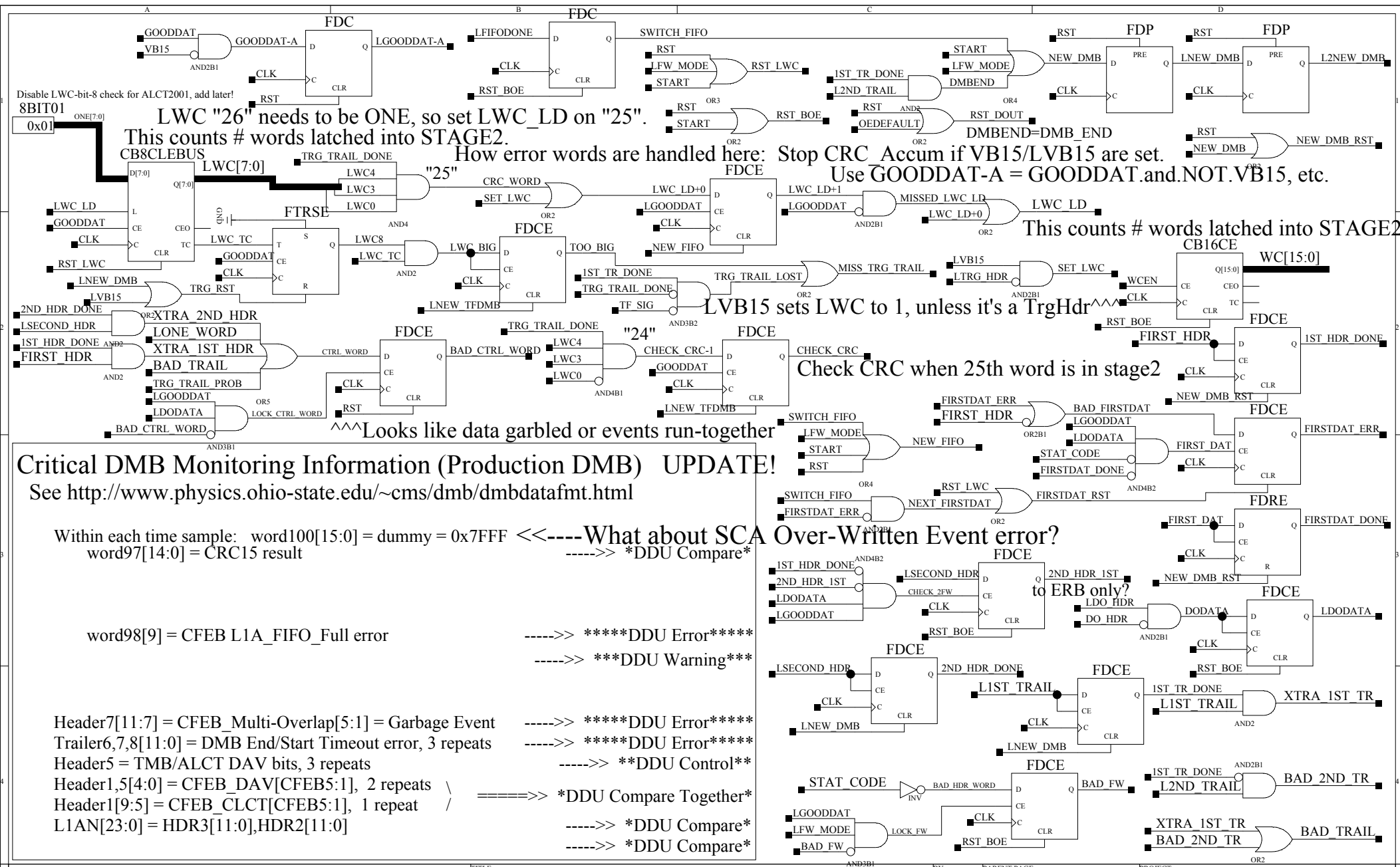
The lowest 13-bits of every 16 go into the CFEB CRC (but reverse them!): 52-bits of data --->15-bit CRC  
 Only the lowest 12-bits of every 16 go into the Special Word Decode (un-reverse these!)

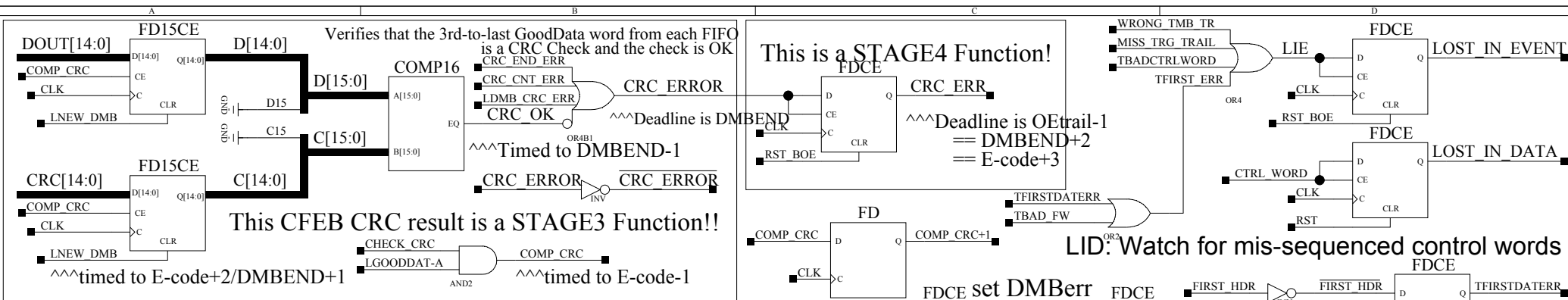


Note: GOODDAT == GOLDDAT here!

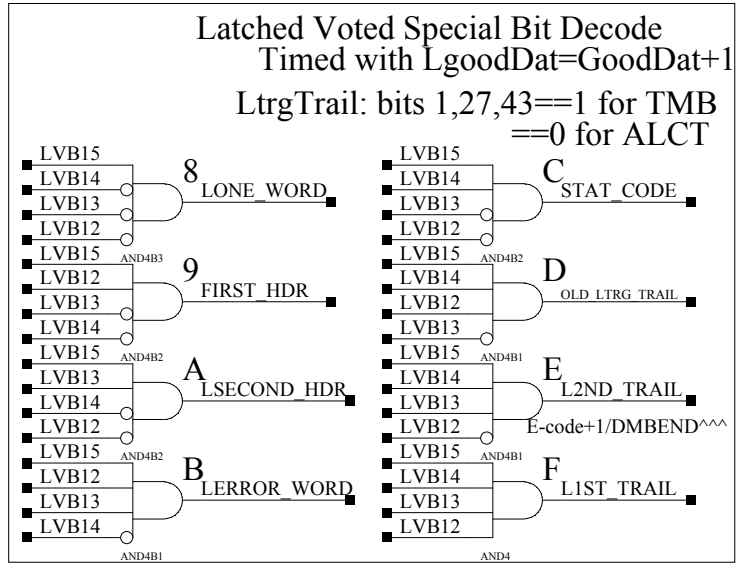
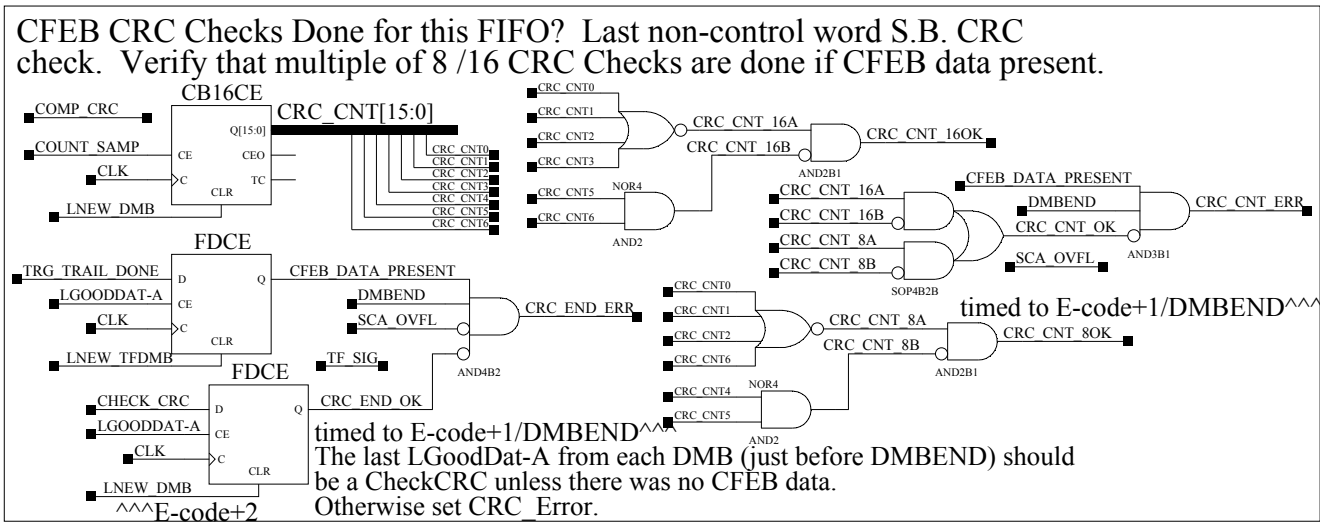
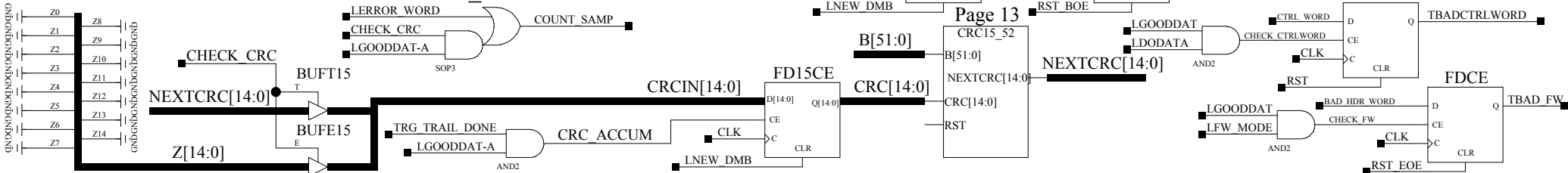
### Control Bit List:

- 0: Gold Data (this FIFO has REN, OE, notMT, LFOK)
- 1: DMB First Word Mode
- 2: Latched Voted Special Bit 12 {2 or more out of 4}
- 3: Latched Voted Special Bit 13 {2 or more out of 4}
- 4: Latched Voted Special Bit 14 {2 or more out of 4}
- 5: Latched Voted Special Bit 15 {2 or more out of 4}
- 6: Do Header Mode (Header to Output)
- 7: Word Count Enable (DDU Header, DMB FIFO Data)
- 8: End of Event (DONE--->OETrail)

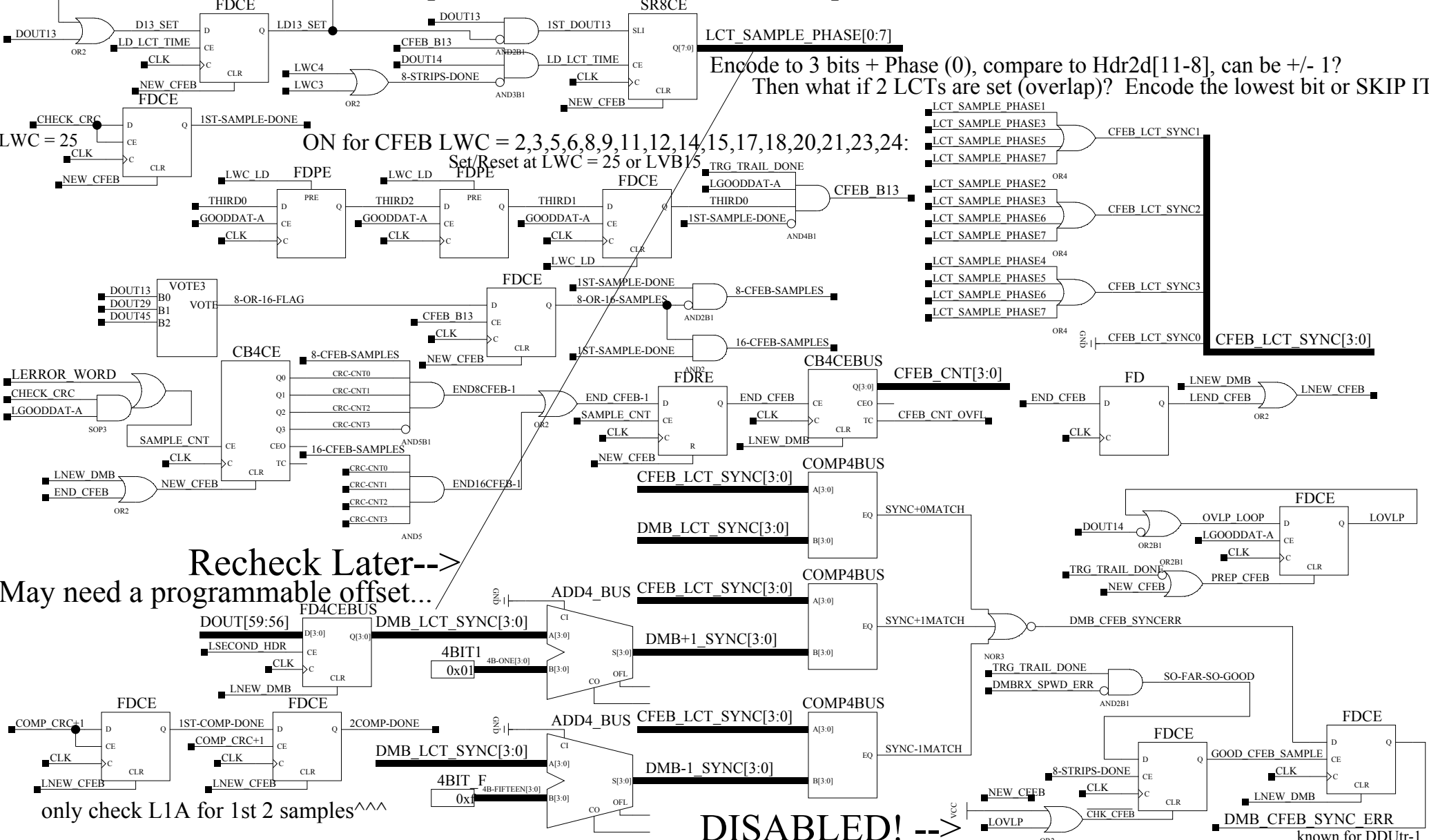




# CFEB/DMB Comparisons and Error Checks

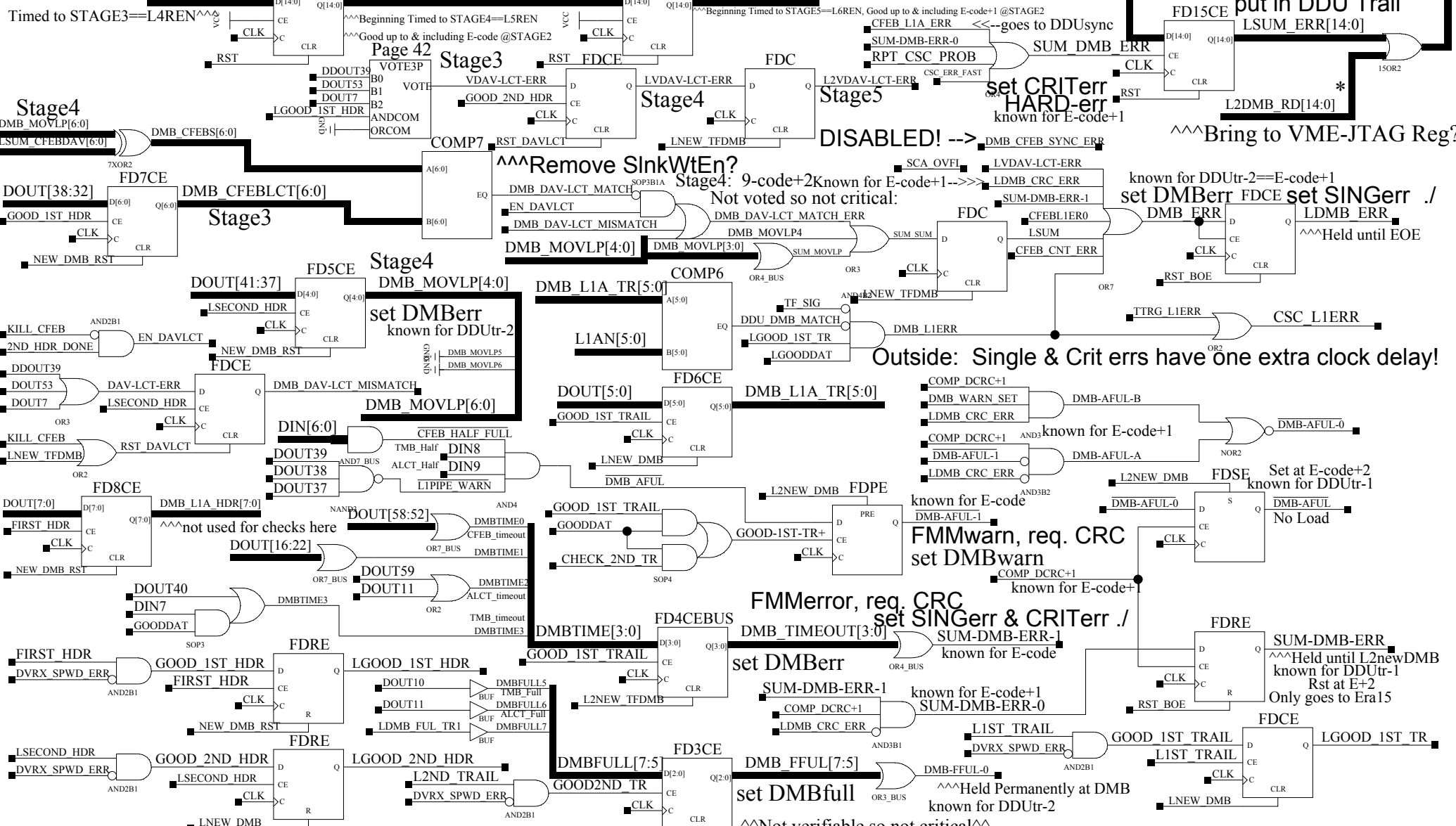


Need to deserialize b13 in 1st sample for \*EACH CFEB\* and compare to Hdr2d!

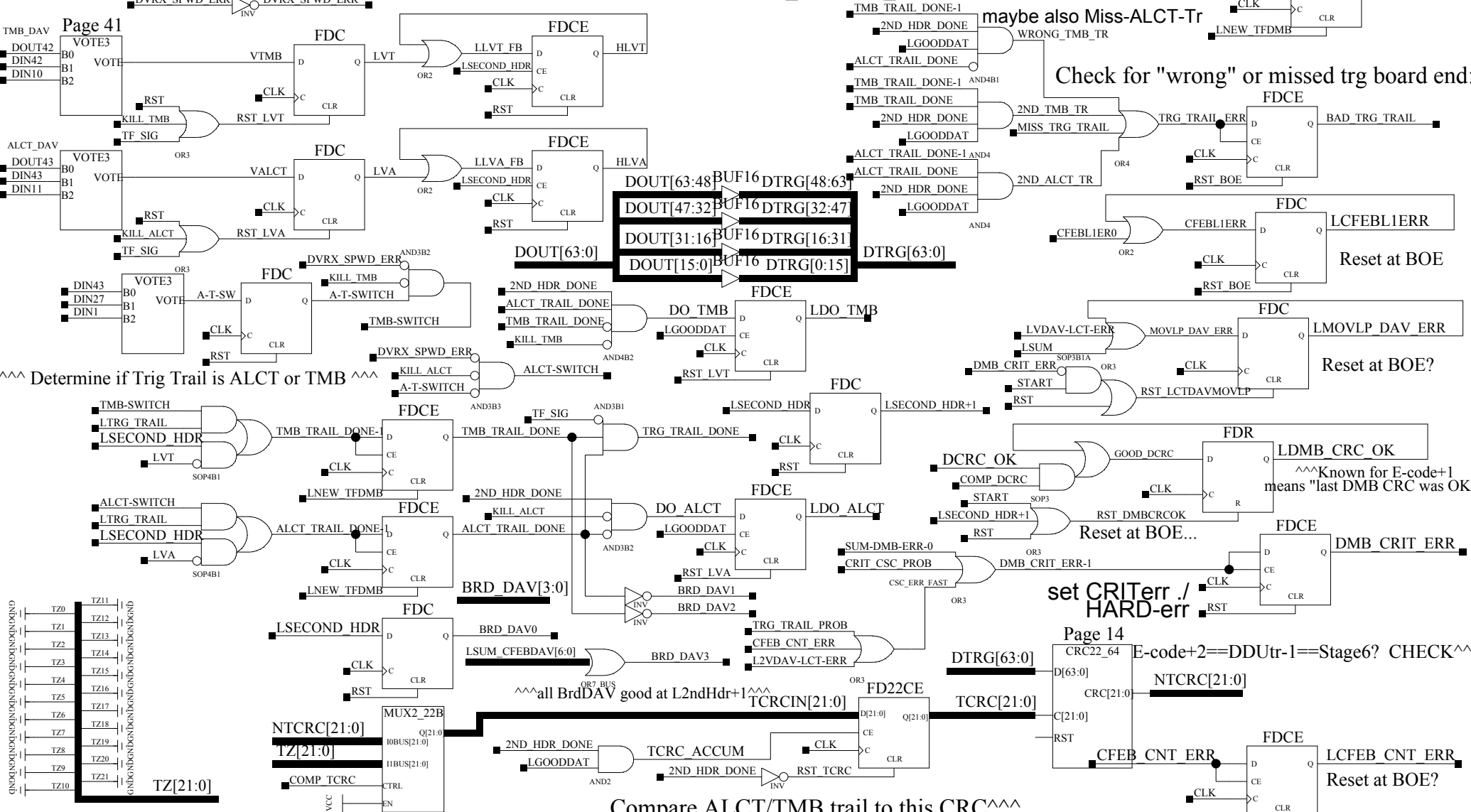




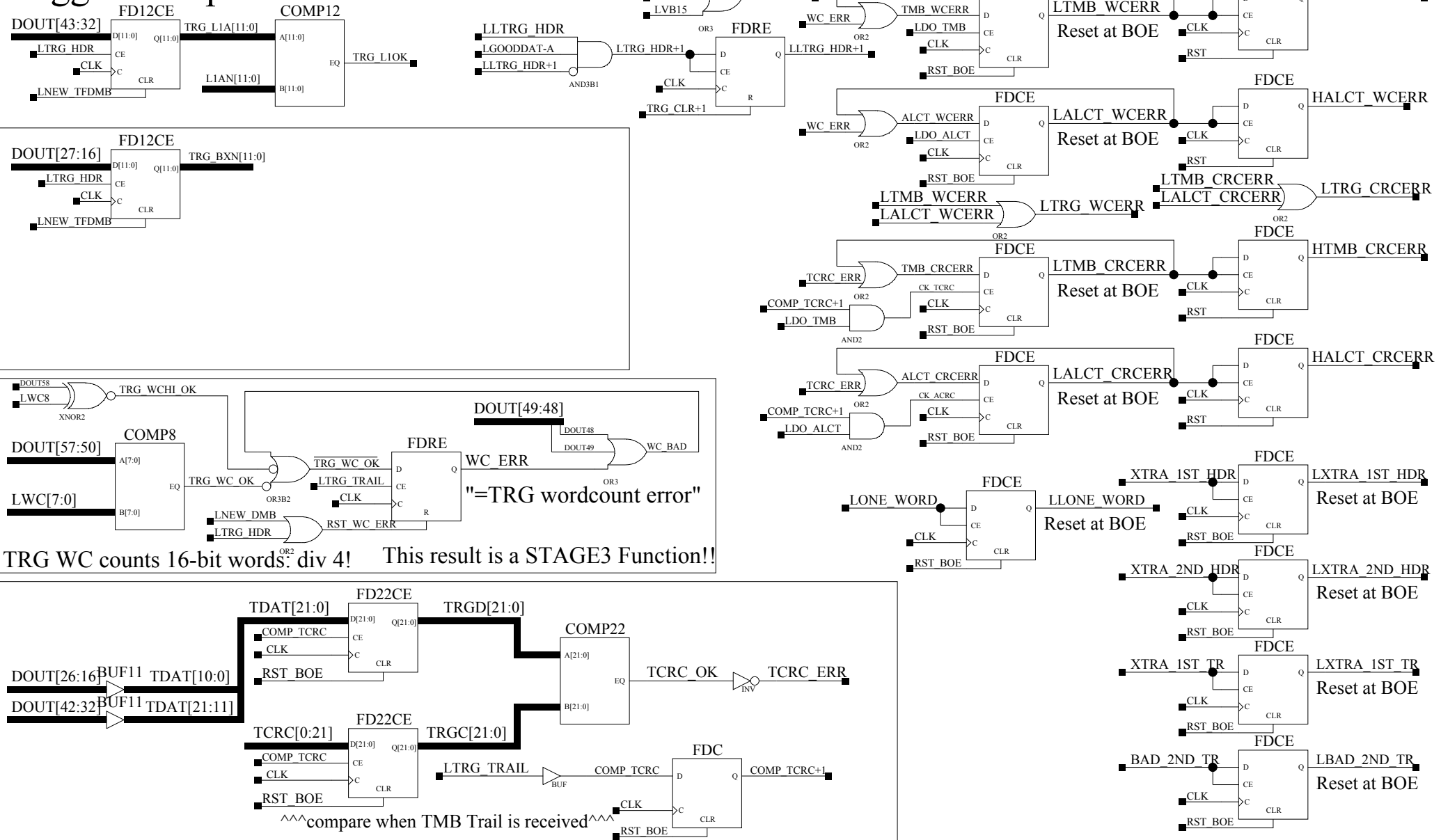
## CSC "Reset Needed" register



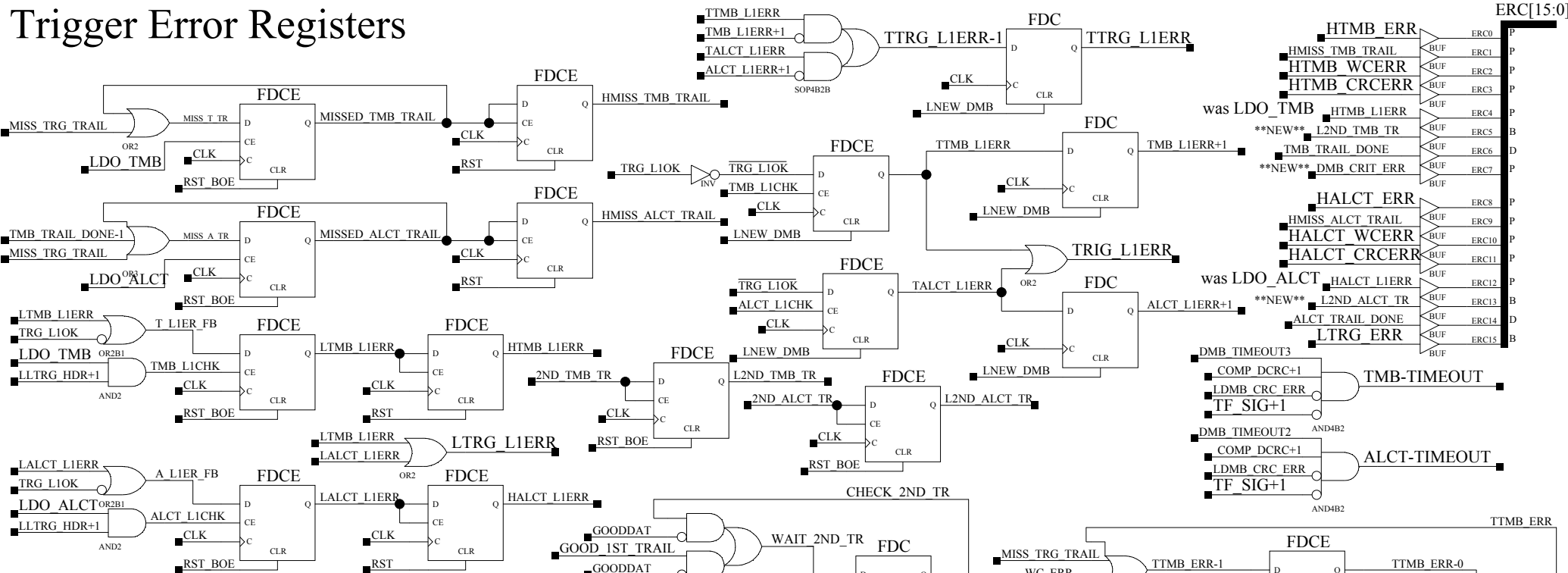
Trigger CRC Check Control: assume that TMB comes after ALCT!  
 ^^^affects L1A check: DoTMB, 1st\_TMB/1st\_ALCT



# Trigger Comparisons and Error Checks

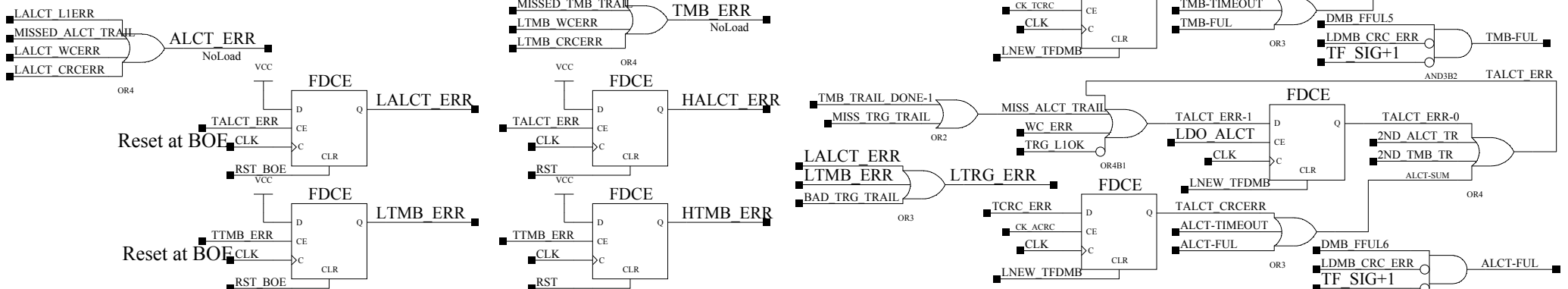


## Trigger Error Registers

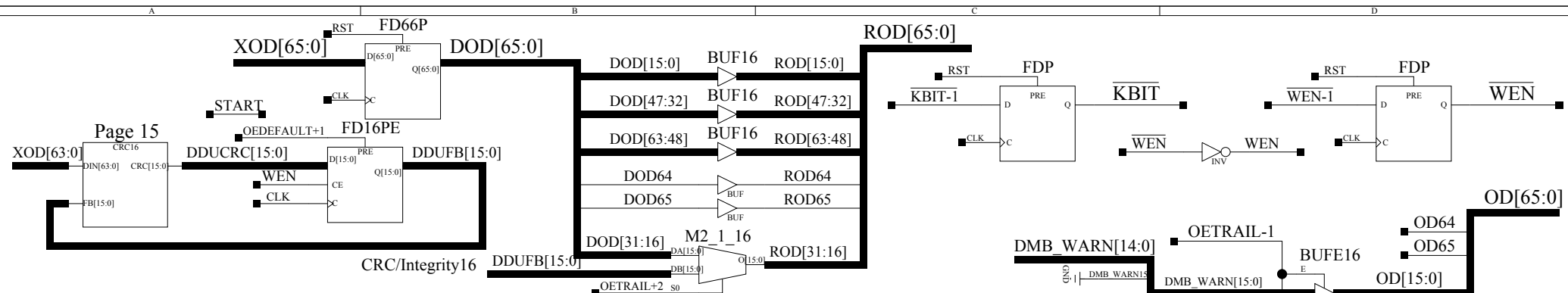


## TMB/ALCT need Err Reg's for CSC/EVT

CRC: Evt      WC: Evt      L1err: Evt  
TMBerr: CSC&Evt      ALCTerr: CSC&Evt







Add Xtra pipeline reg. after OD tbufs, fixes CRCs?

## DDU Timing Info

DDUctrl to InFIFO signals: 2" - 4", .3ns - .6ns

IRCLK has 4 loads, may slow signal by 0.1-0.5ns?

CKFBout has normal drive, IRCLK has ~1.1ns Faster drive

## FPGA I/O Delays (lvcmos33, ns)

IBUF: 0.92

IFD set/hold: 0.92/-0.12 Clk to Q: 0.65

OBUF: 2.33

OFD set/hold: 0.26/0.14 Clk to Q: 2.41

\*modifiers for drive/slew settings:

6mA: add 2.60 for Slow, 1.28 for Fast

8mA: add 1.69 for Slow, 0.46 for Fast

12mA: add 1.18 for Slow, 0.26 for Fast

16mA: add 0.52 for Slow, 0.02 for Fast

24mA: +0.44 for Slow, -0.08 for Fast

## FPGA CLB Delays (ns)

4-FG: 0.32 5-FG: 0.65

FD set/hold: 0/0.14 Clk to Q: 0.38

Sync. set-rst setup: 0.60

Async. pre-clr to Q: 1.25

SR16 Clk to Q: 3.12

SR32 Clk to Q: 3.49

SI set/hold: 0.34/0.01 Q11 (low state) 3.22-3.34 3.23

## TI FIFO I/O Delays (ns)

RCLK to Empty (low state) Vcc: 3.38V 3.04V

Max: 3.6, Min: 2.5 3.02-3.18 3.20-3.29

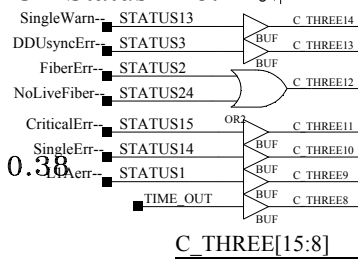
to Not Empty (high state) 3.22-3.34 3.23-3.31

RCLK to Q11 False (low state)

Max: 4.3, Min: 2.5 3.32-3.62 3.40-3.64

to Q11 True (high state) 3.31-3.87 3.51-4.06

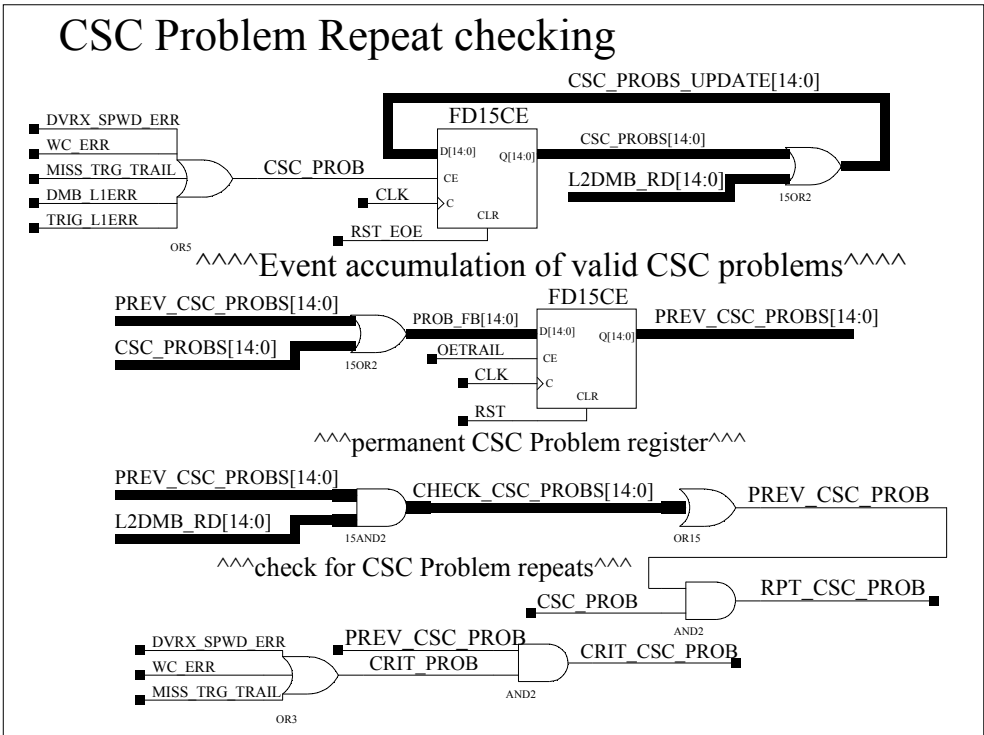
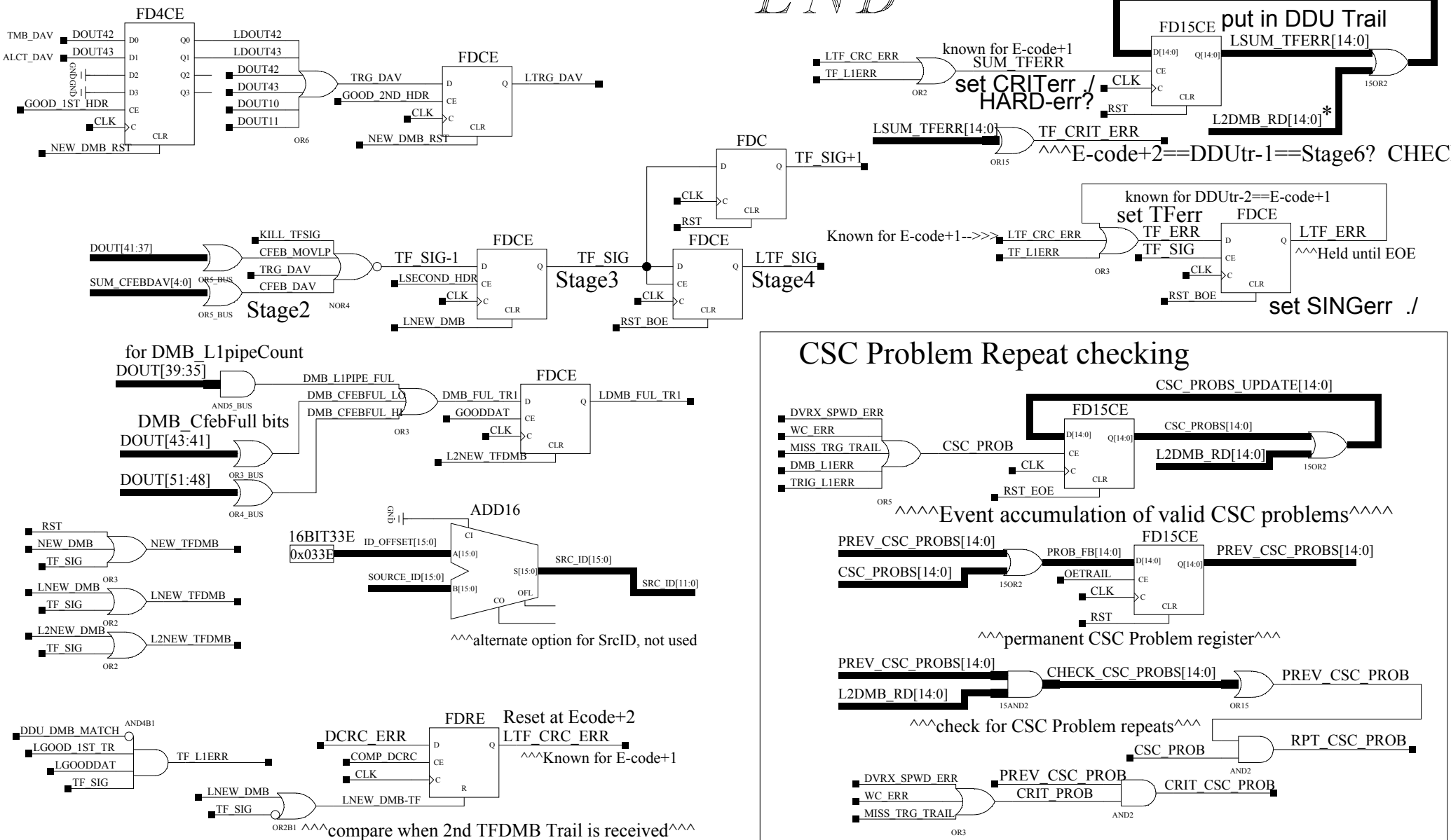
## BOE Status info:

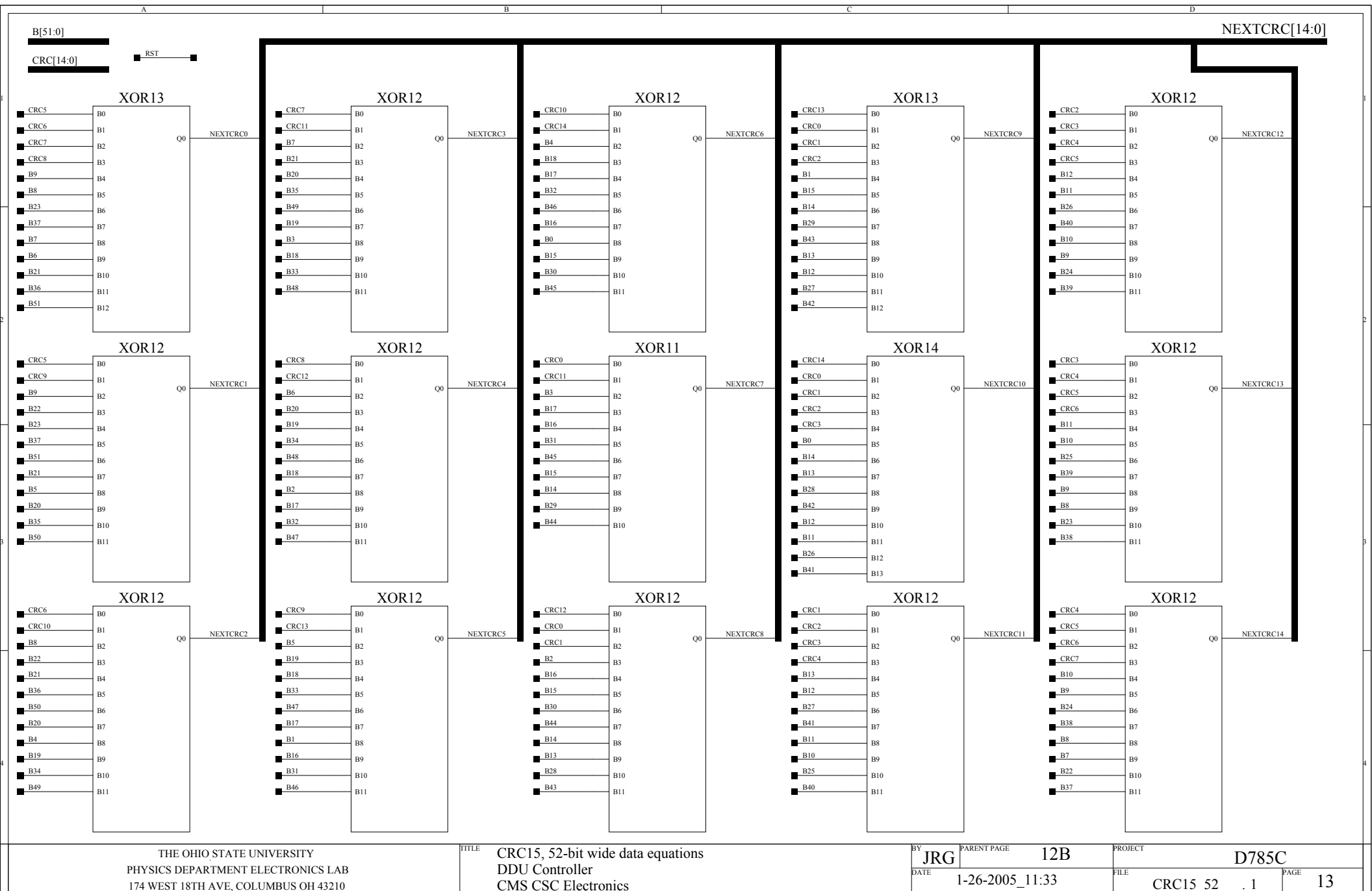


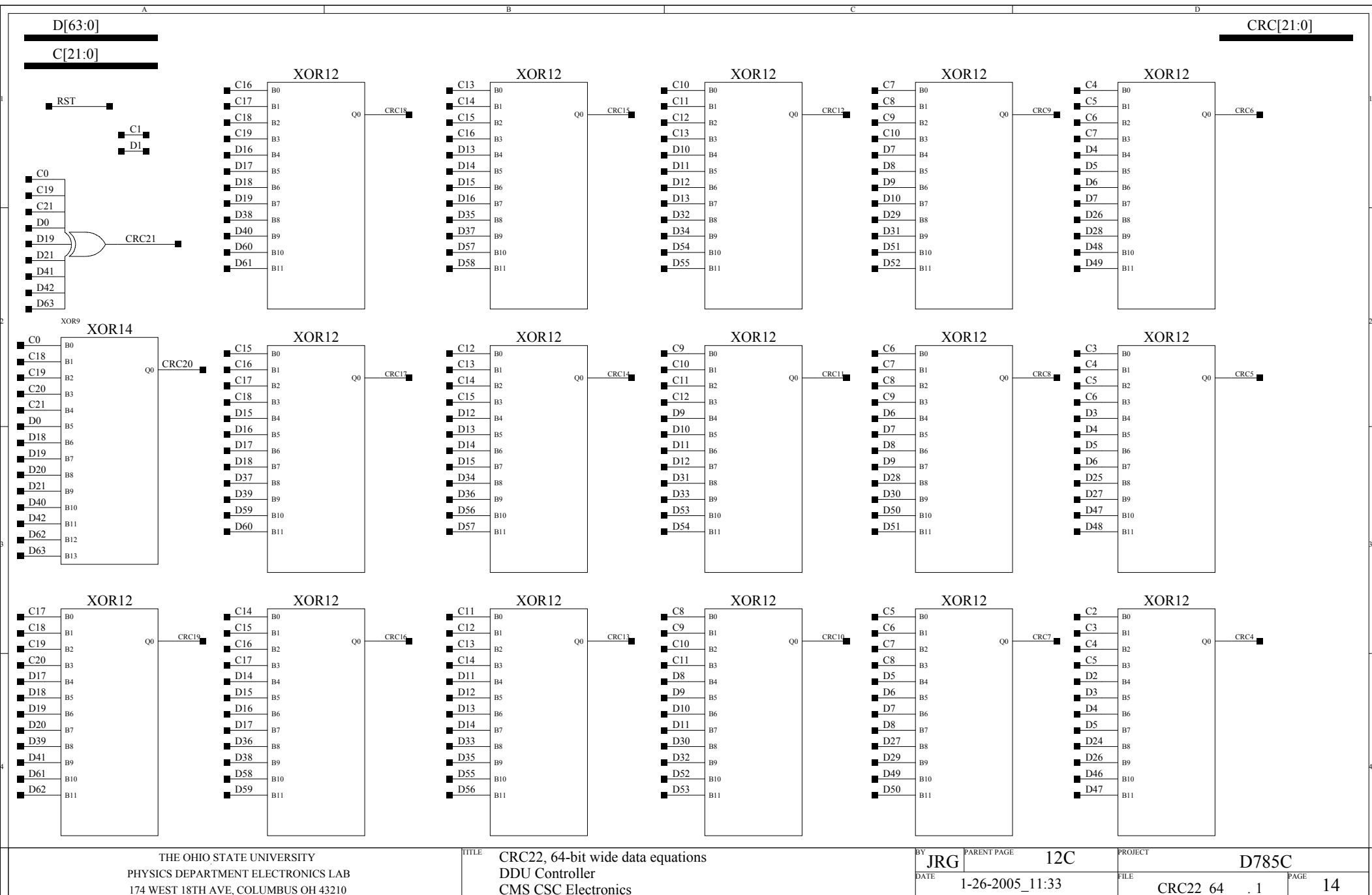
C\_THREE[15:8]

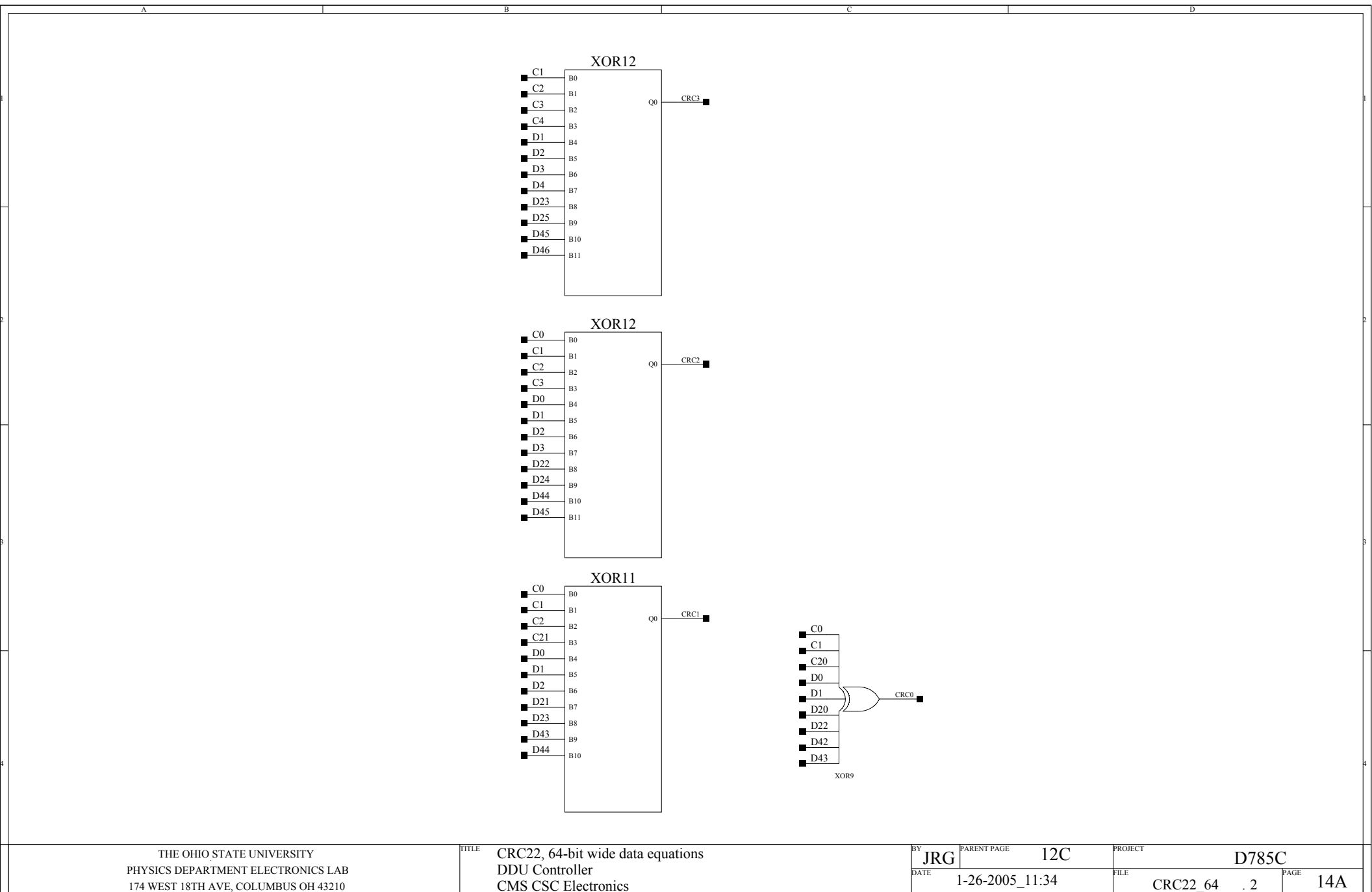
Check for Track Finder signal, record TF errors

END

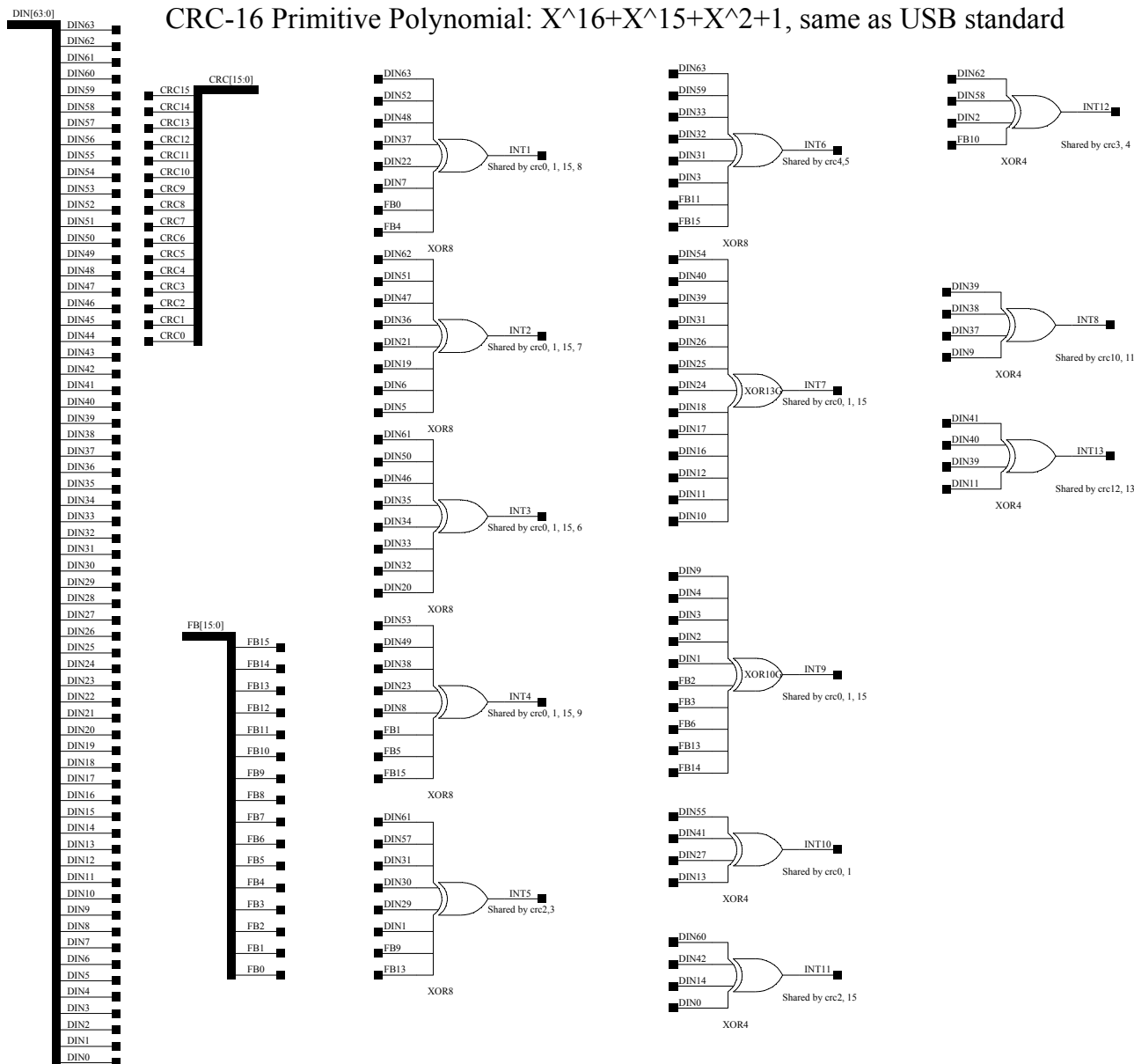


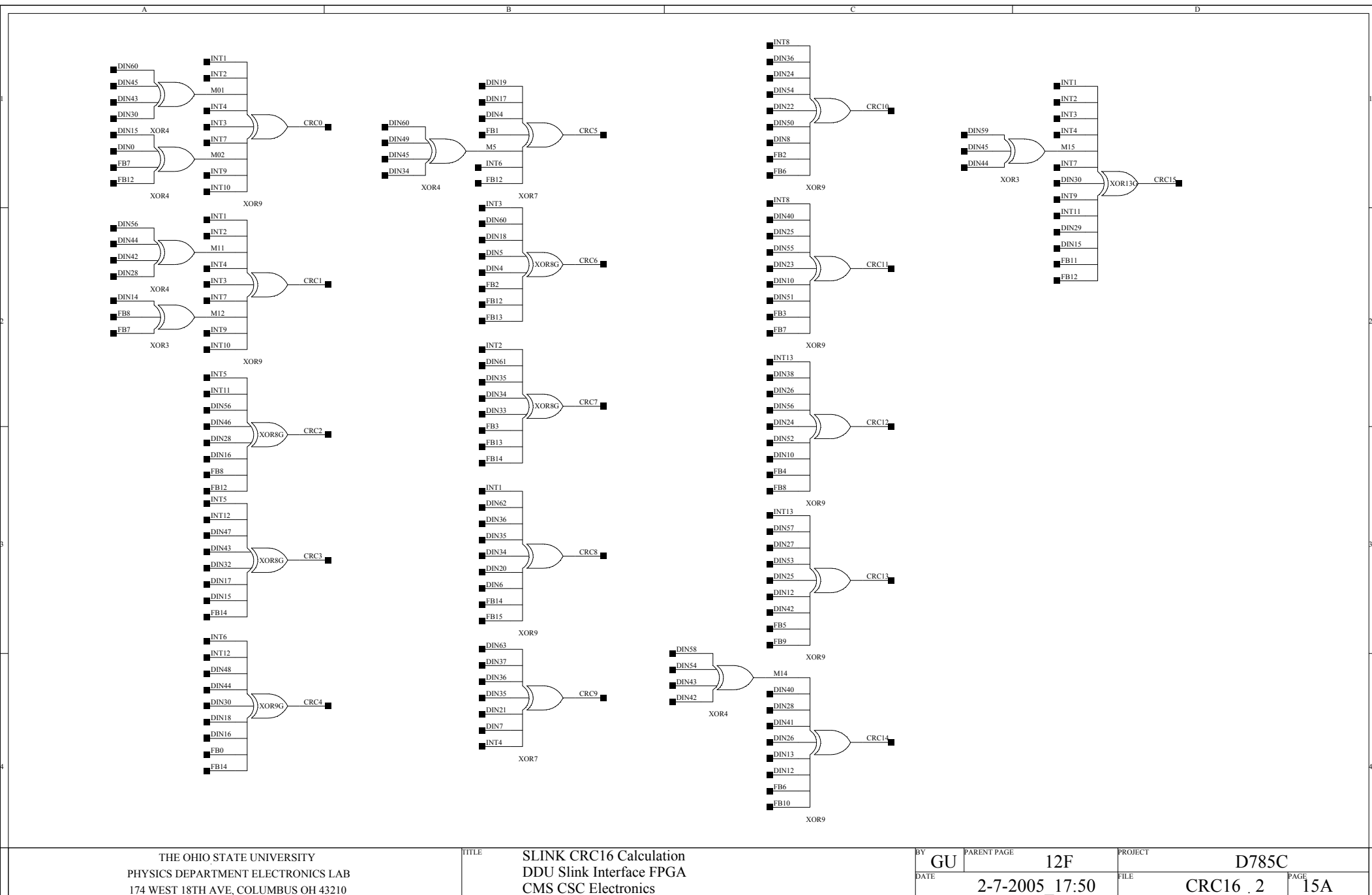




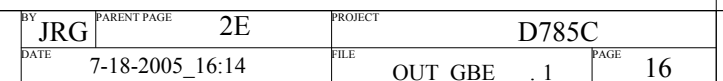
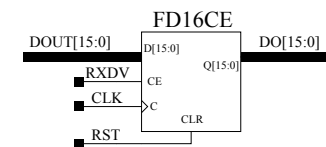


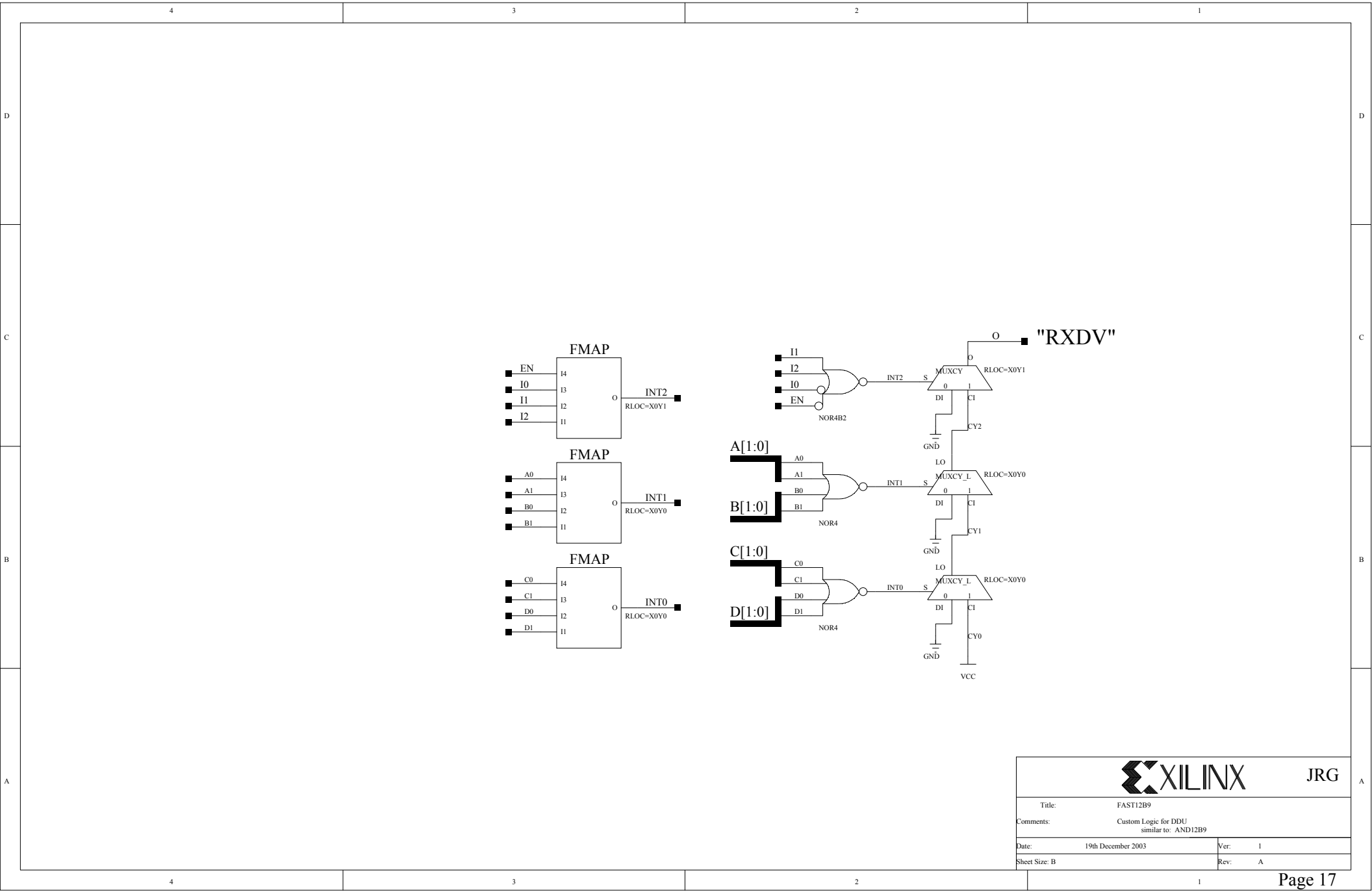
# CRC-16 Primitive Polynomial: $X^{16}+X^{15}+X^2+1$ , same as USB standard





---> Not done yet! Consider a counter to skip 1st ~12 bytes after K word. Skip 4 CRC bytes too.

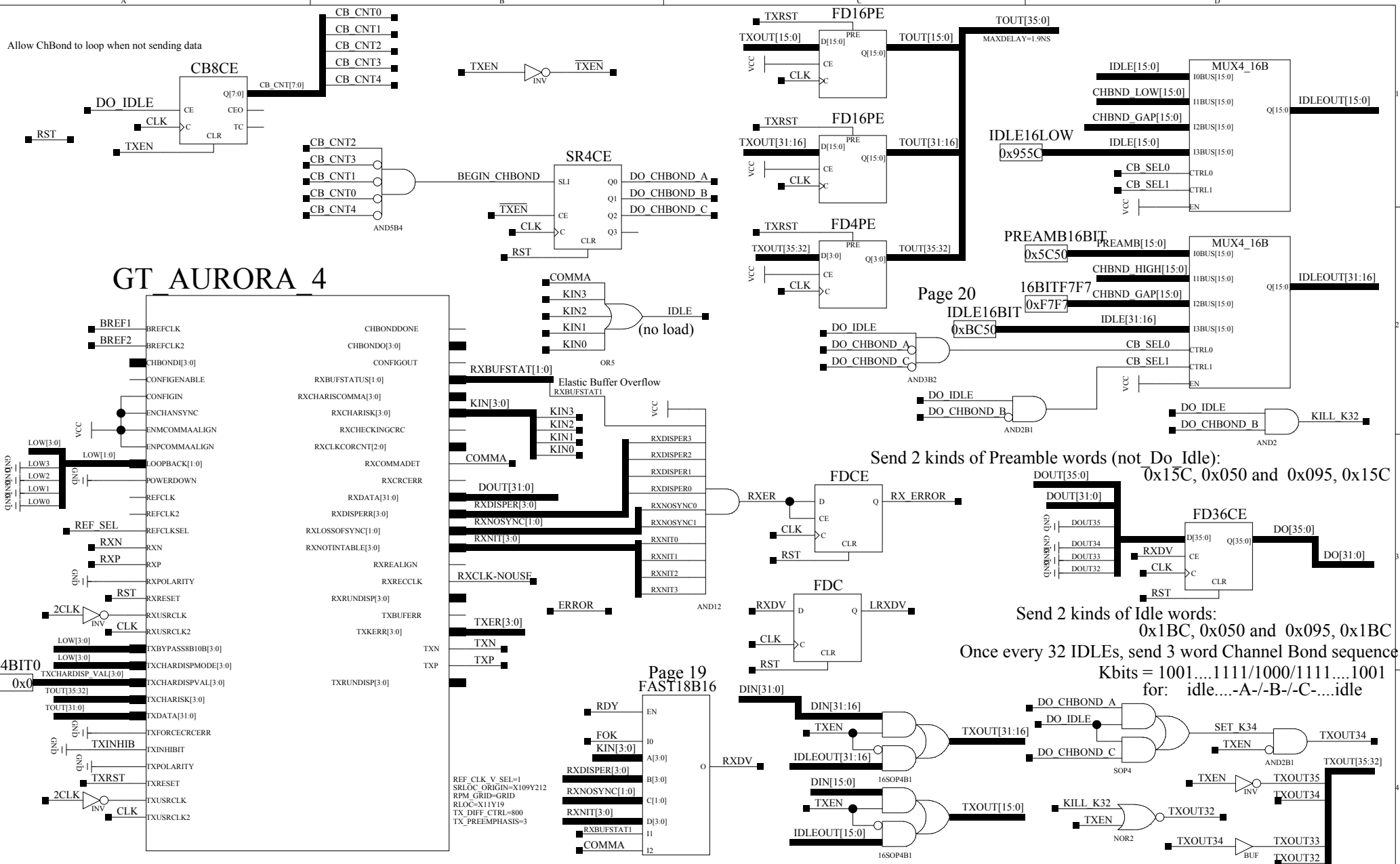


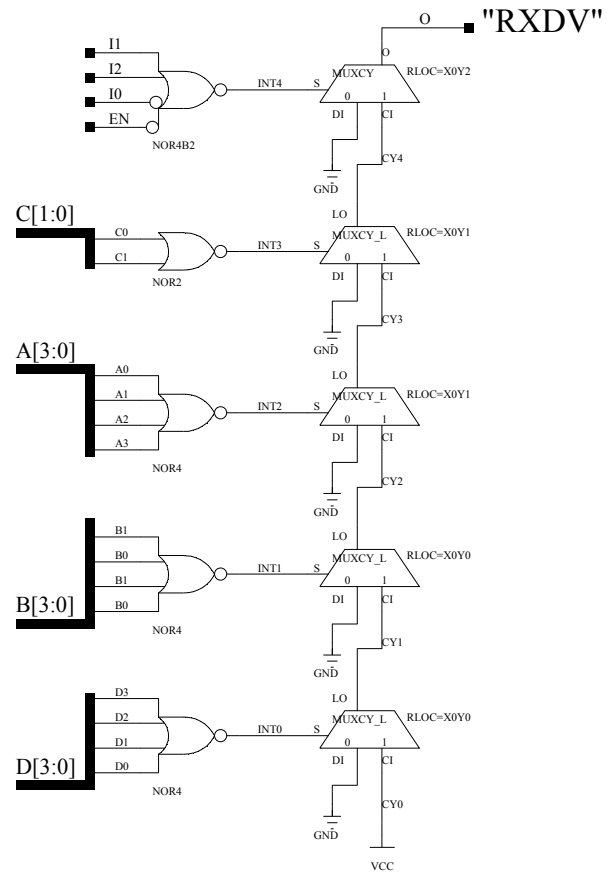
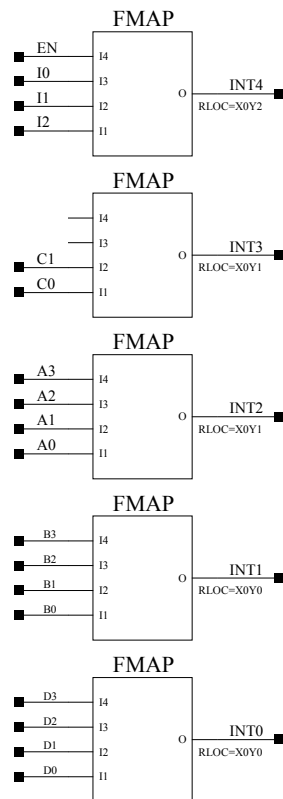


JRG

|               |                                             |
|---------------|---------------------------------------------|
| Title:        | FAST12B9                                    |
| Comments:     | Custom Logic for DDU<br>similar to: AND12B9 |
| Date:         | 19th December 2003                          |
| Sheet Size: B | Ver: 1<br>Rev: A                            |

Allow ChBond to loop when not sending data



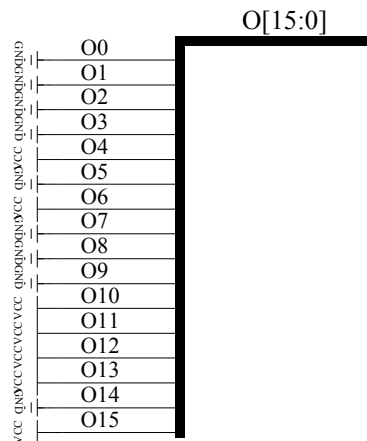


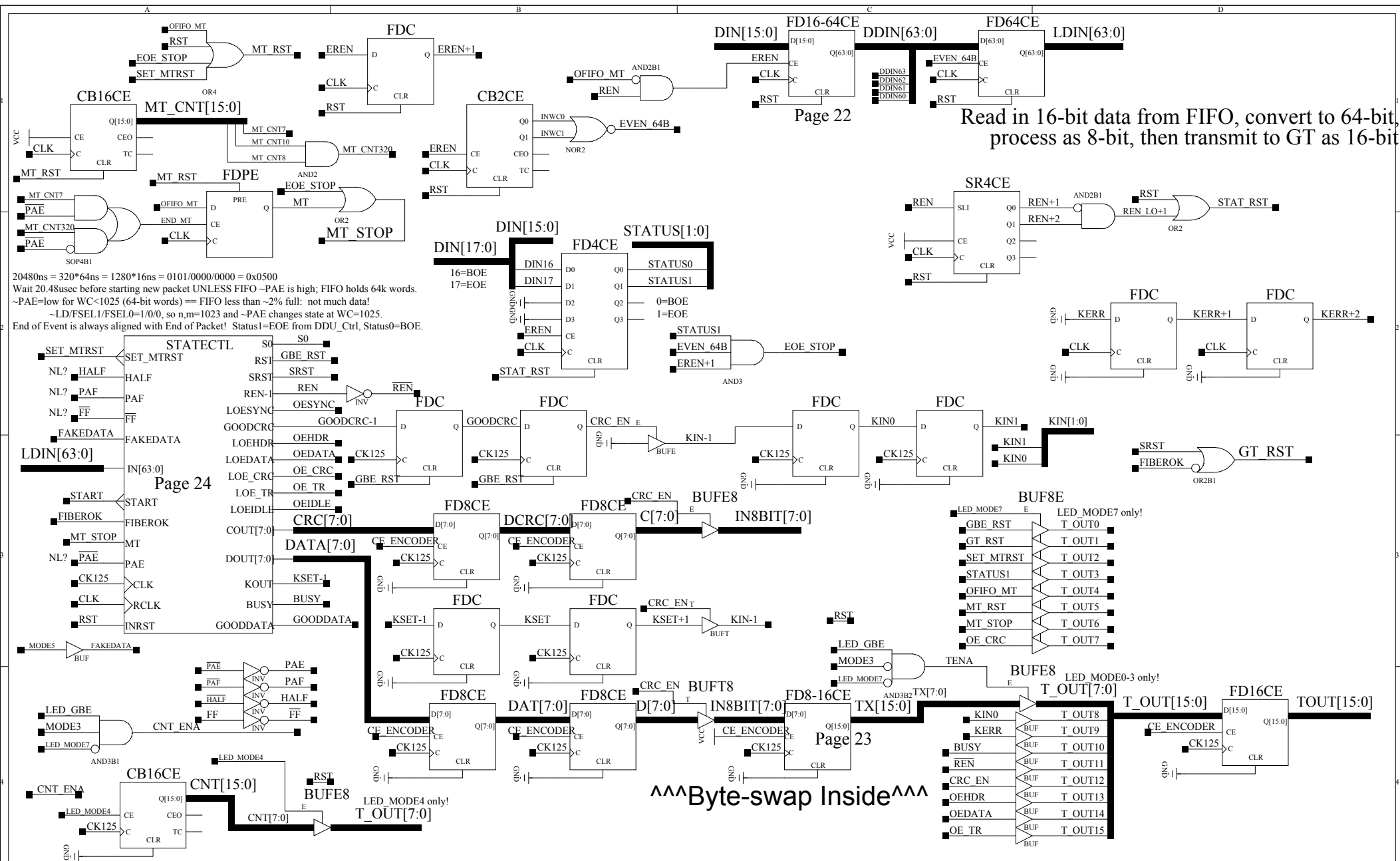
JRG

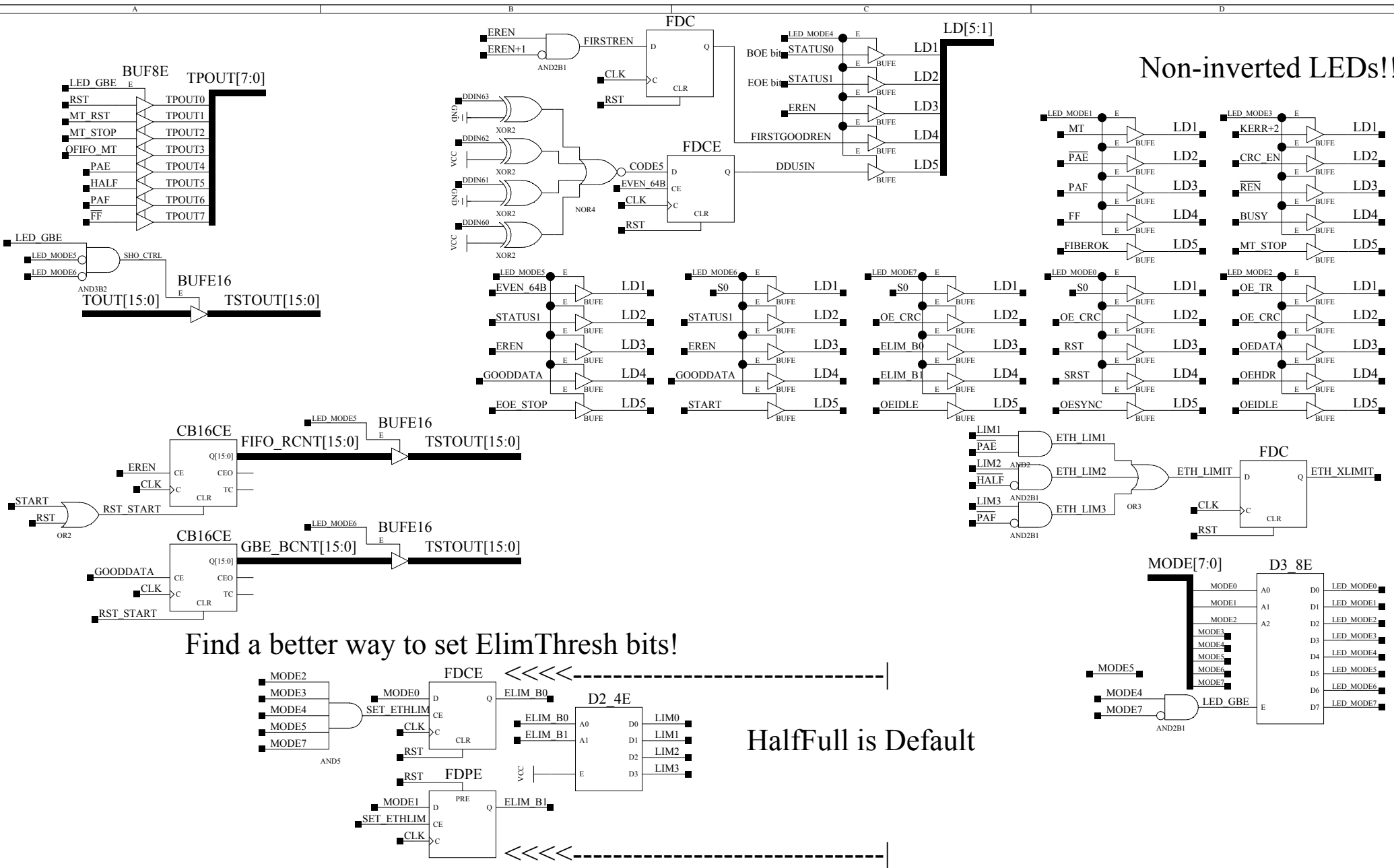
|             |                                                                               |      |   |
|-------------|-------------------------------------------------------------------------------|------|---|
| Title:      | FAST13B10                                                                     |      |   |
| Comments:   | Custom Logic for DDU similar to: AND12B10 with an OR2 (allows ON to override) |      |   |
| Date:       | 19th December 2003                                                            | Ver: | 1 |
| Sheet Size: | B                                                                             | Rev: | A |

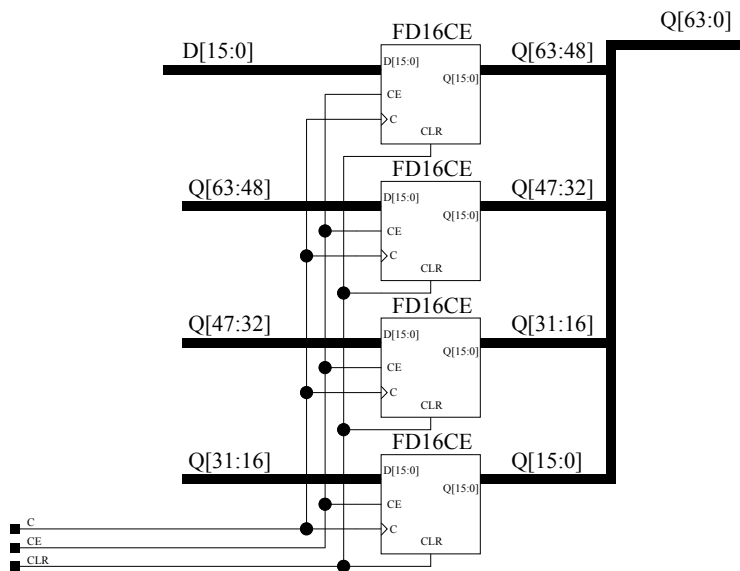
Send 2 Idle bytes:

K28.5(10111100)+D16.2(01010000)  
= 0x1BC + 0x050 (time-ordered)  
= 0xBC50 (in parallel)









JRG

Title: VIRTEX Family FD16-64CE Macro  
Comment: 64-Bit Bus Matching Register with Asynchronous Clear and Chip Enable

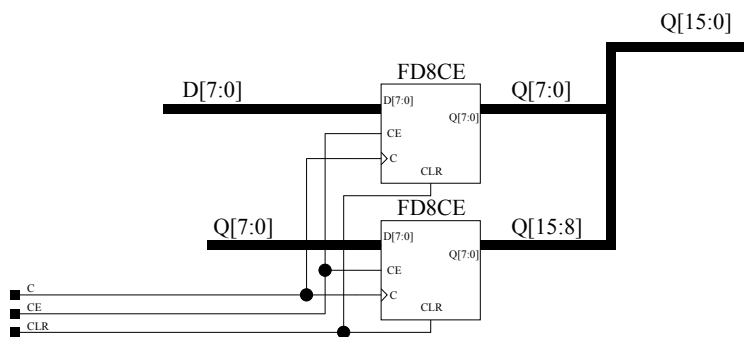
|             |                   |      |   |
|-------------|-------------------|------|---|
| Date:       | 2nd February 2004 | Ver: | 1 |
| Sheet Size: | B                 | Rev: | A |

4

3

2

1



JRG

|               |                                                                        |      |   |
|---------------|------------------------------------------------------------------------|------|---|
| Title:        | VIRTEX Family FD8-16CE Macro                                           |      |   |
| Comments:     | 8-16-Bit Bus Matching Register with Asynchronous Clear and Chip Enable |      |   |
| Date:         | 4th February 2004                                                      | Ver: | 1 |
| Sheet Size: B |                                                                        | Rev: | A |

4

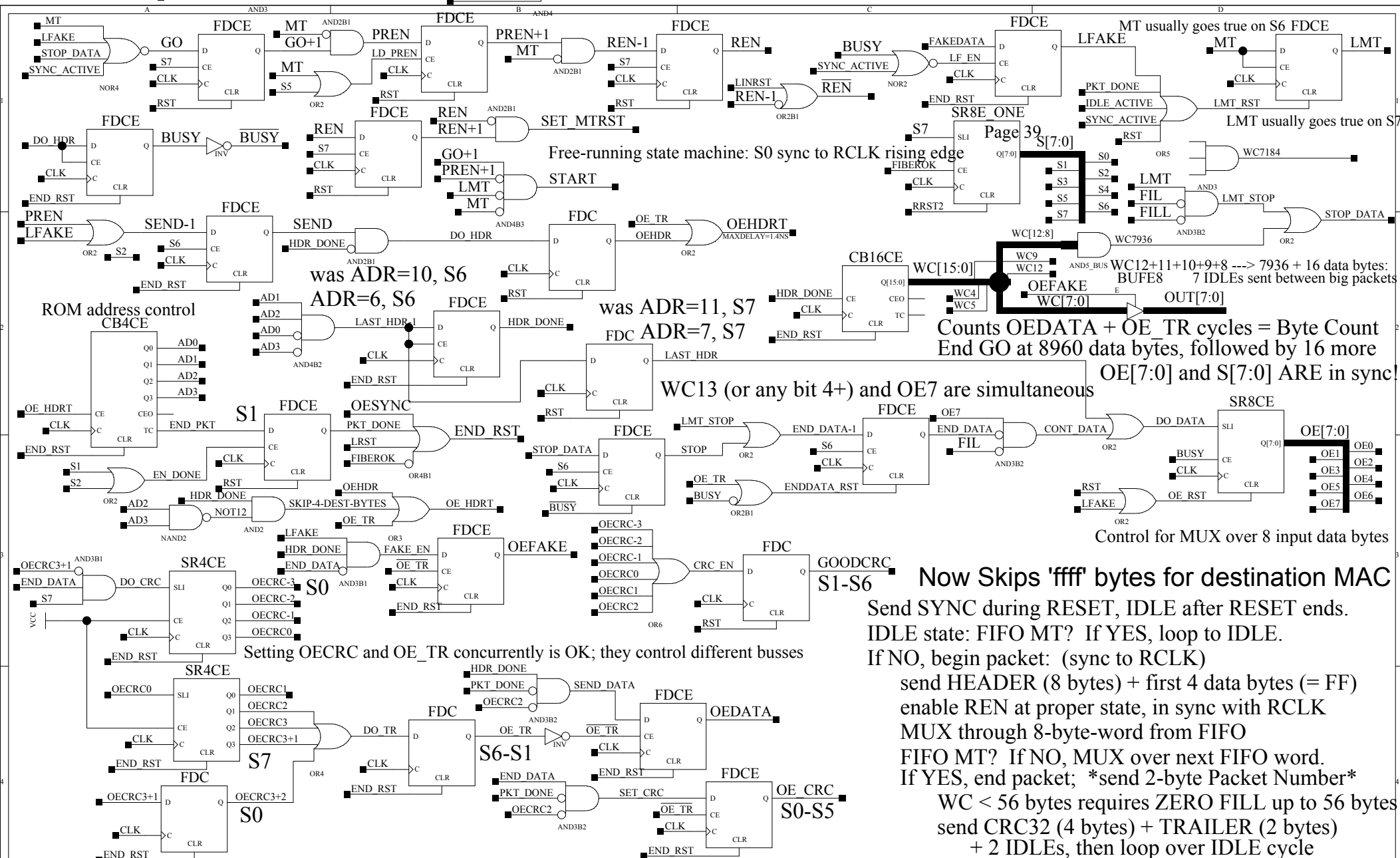
3

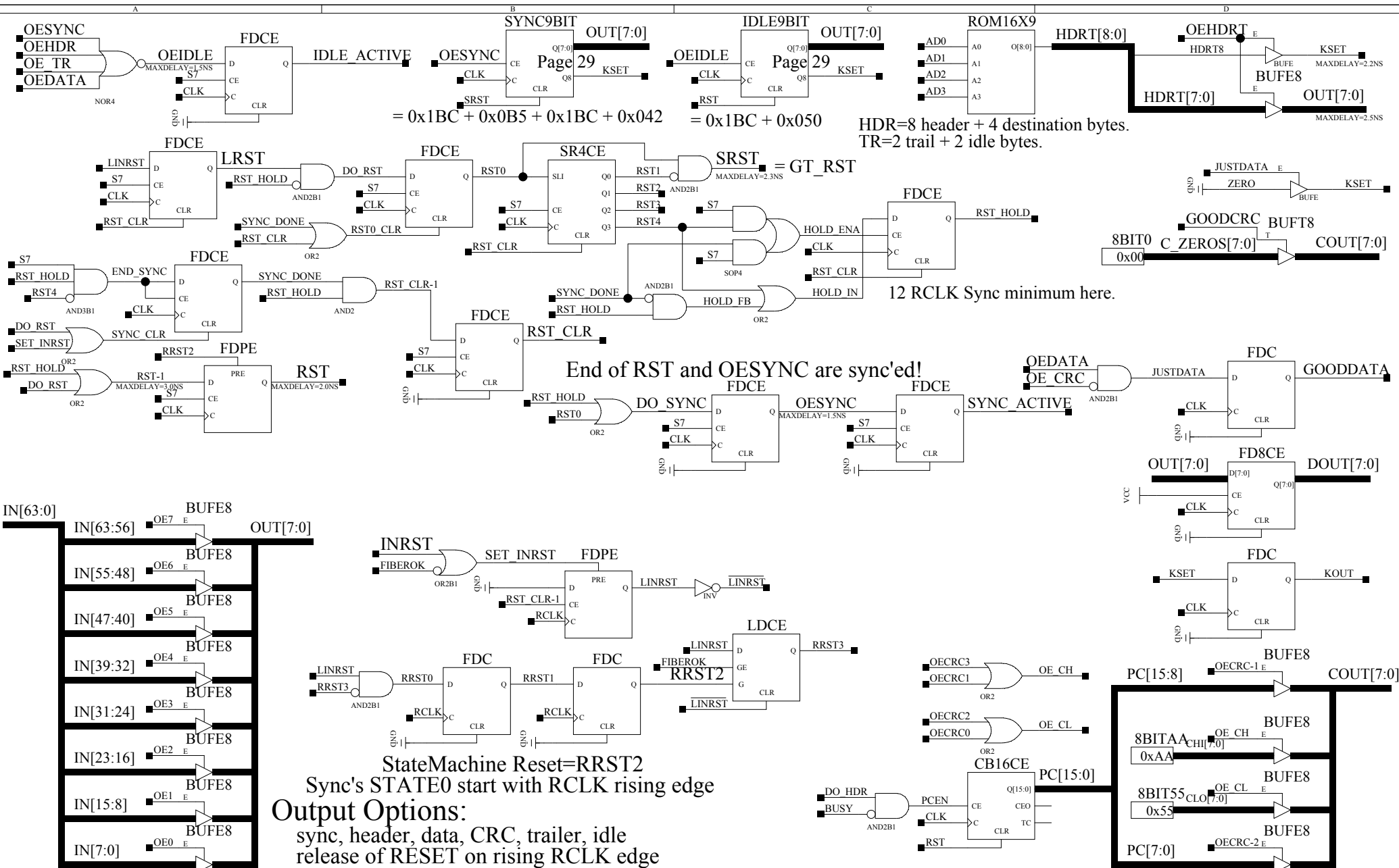
2

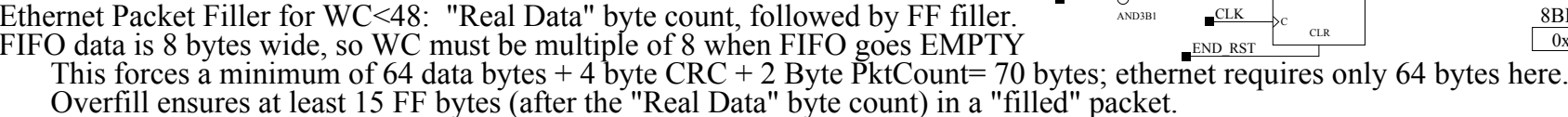
1

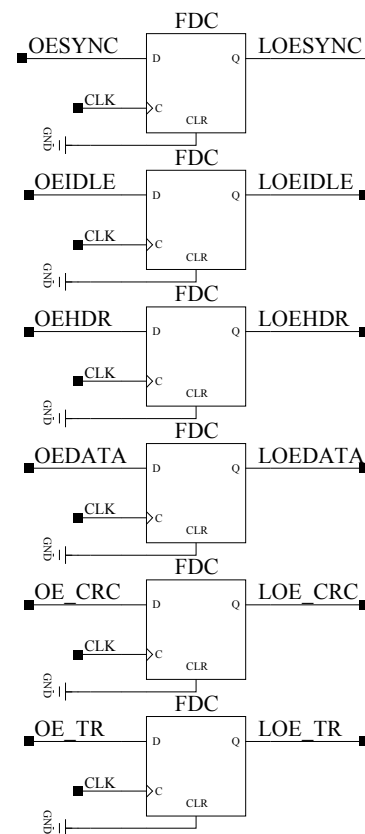
WC13+9+8 ---> 8960 + 16 data bytes:

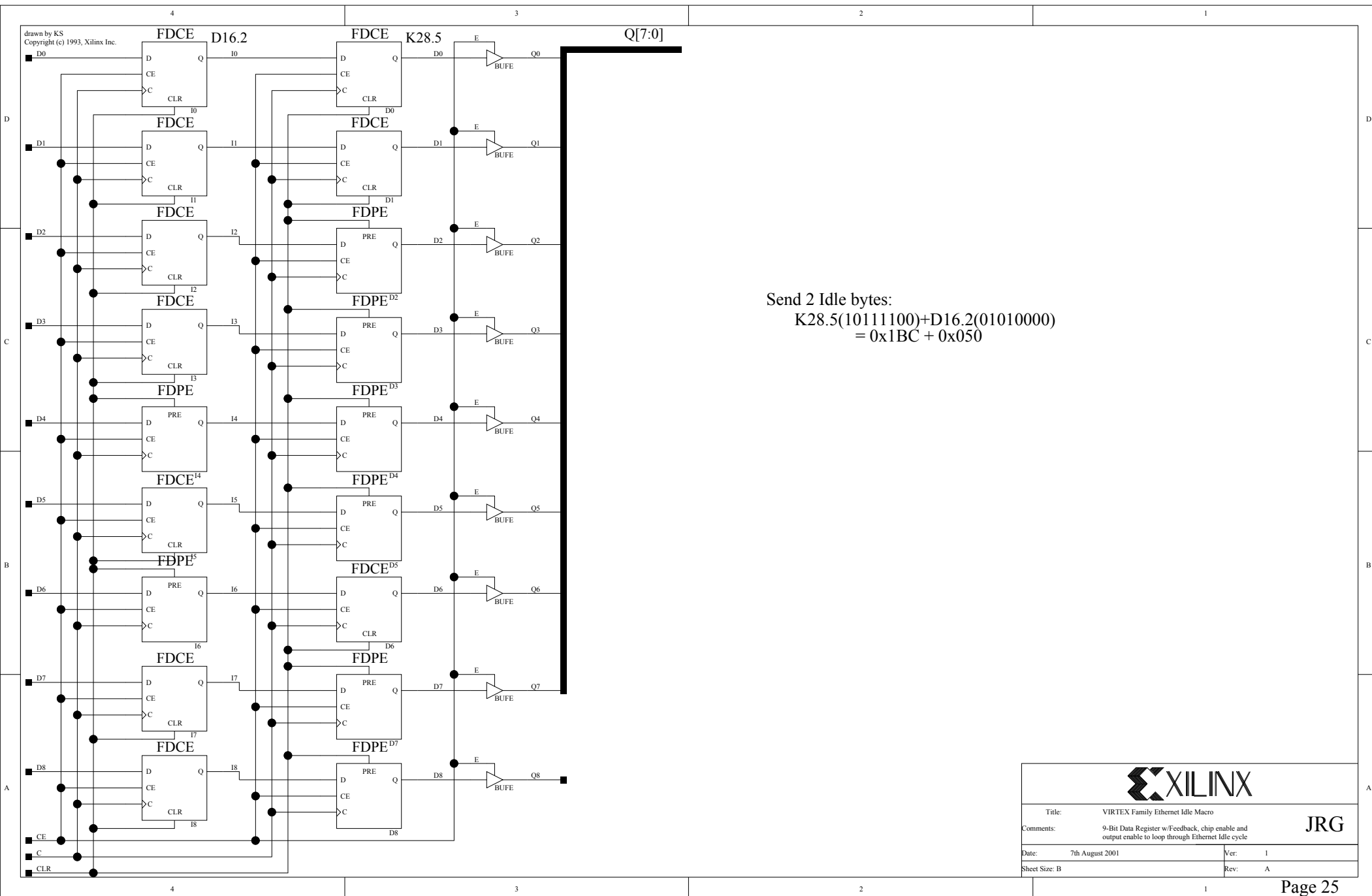
WC12+11+10+9 ----> 7680 + 16 data bytes:





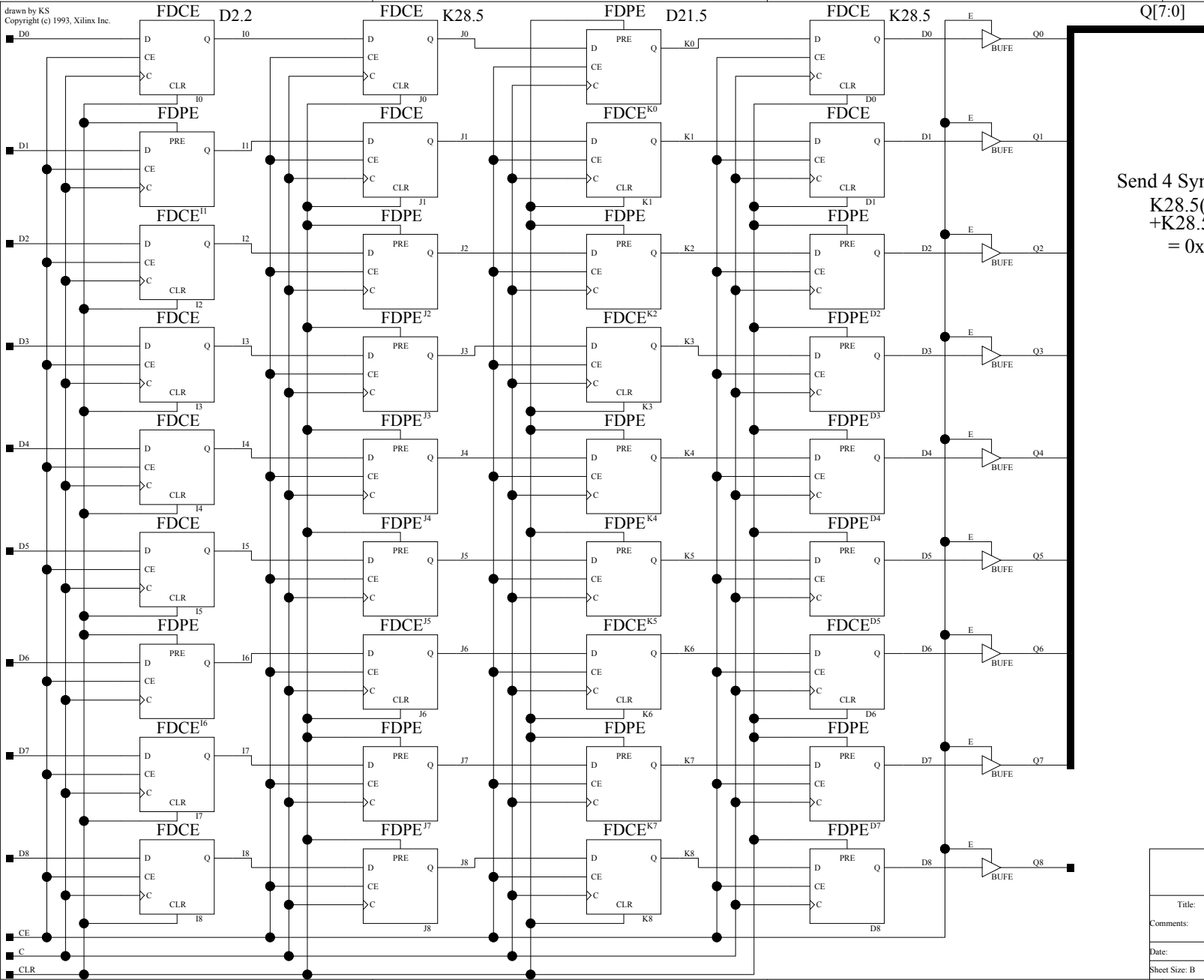






|               |                                                                                                    |        |
|---------------|----------------------------------------------------------------------------------------------------|--------|
| Title:        | VIRTEX Family Ethernet Idle Macro                                                                  | JRG    |
| Comments:     | 9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Idle cycle. |        |
| Date:         | 7th August 2001                                                                                    | Ver: 1 |
| Sheet Size: B |                                                                                                    | Rev: A |

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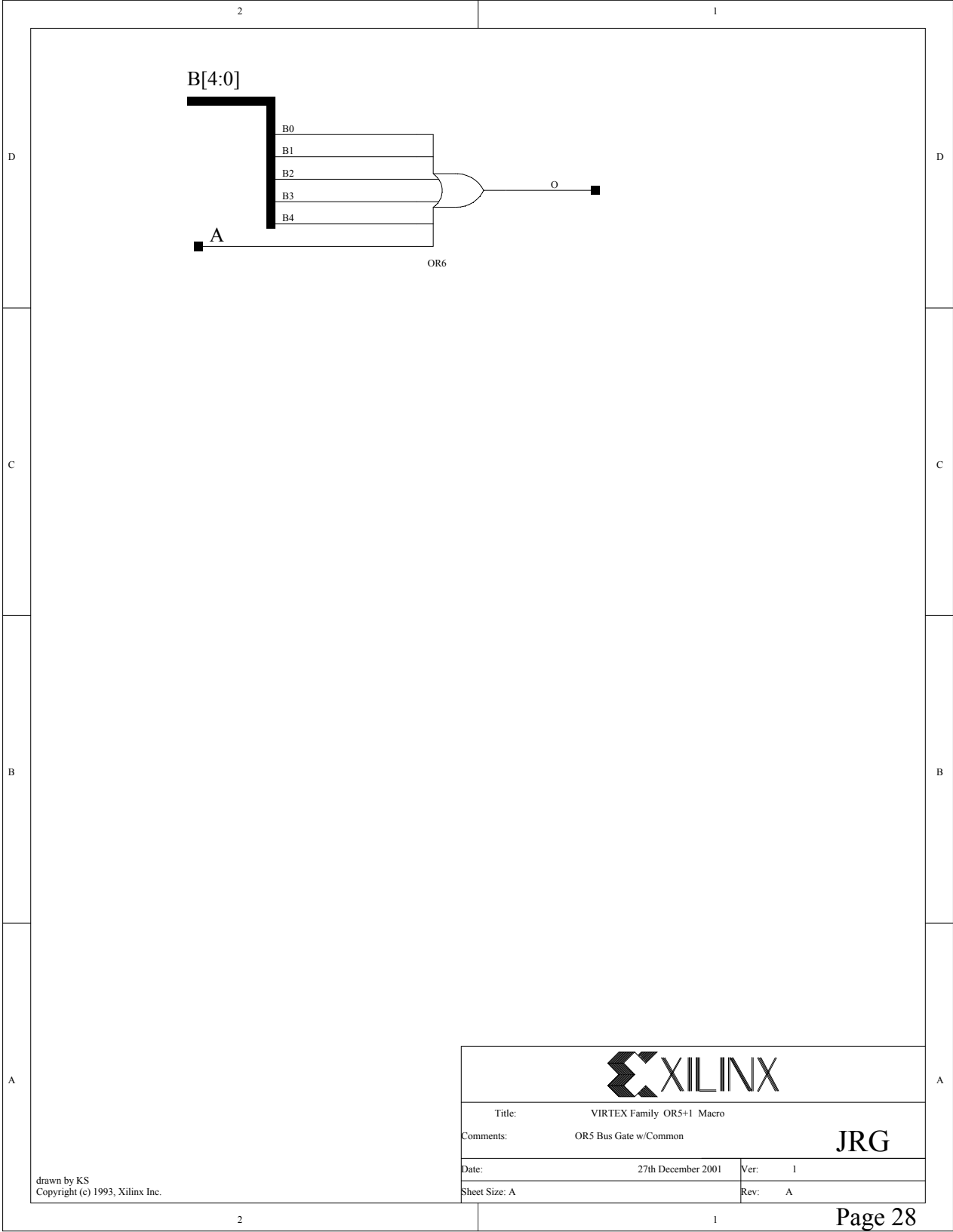


Send 4 Sync bytes:  
 $K28.5(10111100)+D21.5(01011010)$   
 $+K28.5(10111100)+D2.2(001000010)$   
 $= 0x1BC + 0x0B5 + 0x1BC + 0x042$



|               |                                                                                                   |      |     |
|---------------|---------------------------------------------------------------------------------------------------|------|-----|
| Title:        | VIRTEX Family Ethernet Syne Macro                                                                 |      | JRG |
| Comments:     | 9-Bit Data Register w/Feedback, chip enable and output enable to loop through Ethernet Syne cycle |      |     |
| Date:         | 7th August 2001                                                                                   | Ver: | 1   |
| Sheet Size: B |                                                                                                   | Rev: | A   |





|                                  |        |
|----------------------------------|--------|
| Title: VIRTEX Family OR5+1 Macro |        |
| Comments: OR5 Bus Gate w/Common  |        |
| Date: 27th December 2001         | Ver: 1 |
| Sheet Size: A                    | Rev: A |

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STAT[11:0]

STAT[11:8]

STAT[7:0]

STAT11  
STAT10  
STAT9  
STAT8  
STAT7  
STAT6  
STAT5  
STAT4  
STAT3  
STAT2  
STAT1  
STAT0

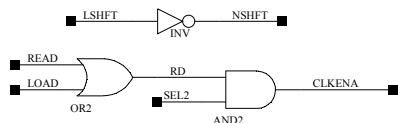
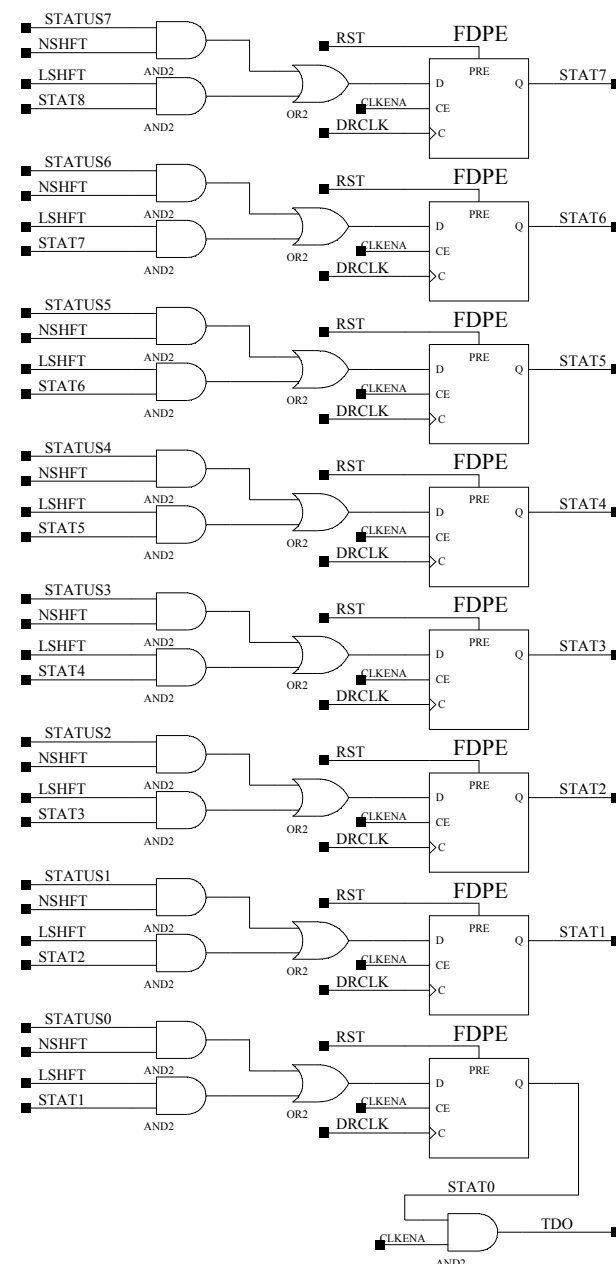
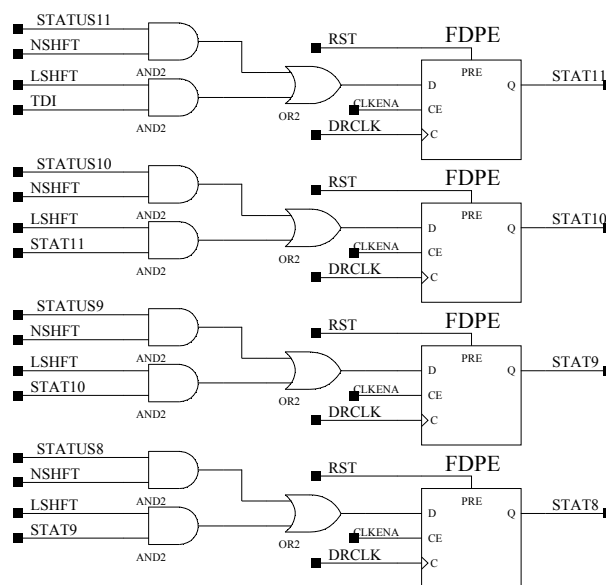
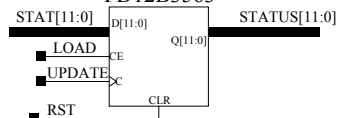
STATUS[11:0]

STATUS[11:8]

STATUS[7:0]

STATUS11  
STATUS10  
STATUS9  
STATUS8  
STATUS7  
STATUS6  
STATUS5  
STATUS4  
STATUS3  
STATUS2  
STATUS1  
STATUS0

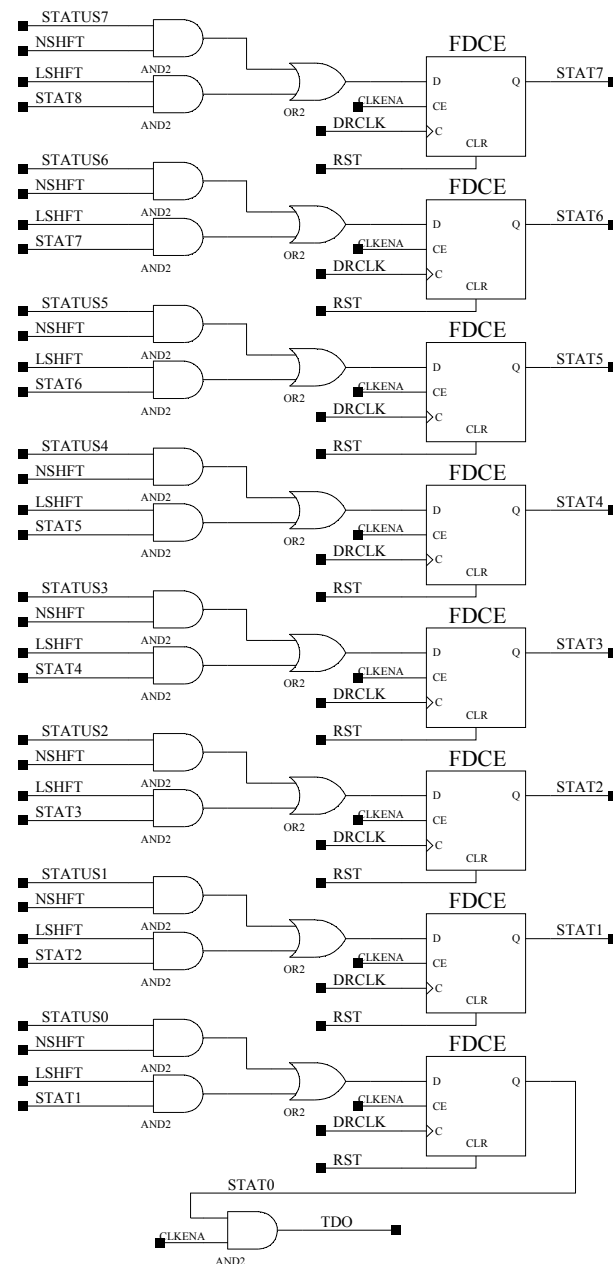
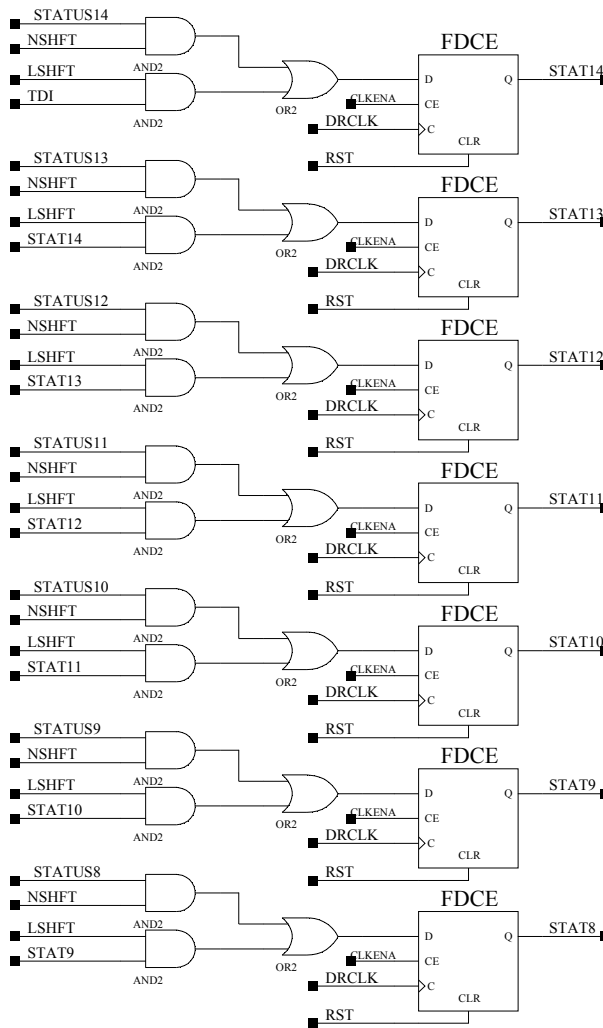
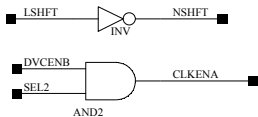
Default=924 BX per Orbit

Page 34  
FD12B3563

# 15-bit JTAG Register Read out (on DVCENB)

STATUS[14:0]

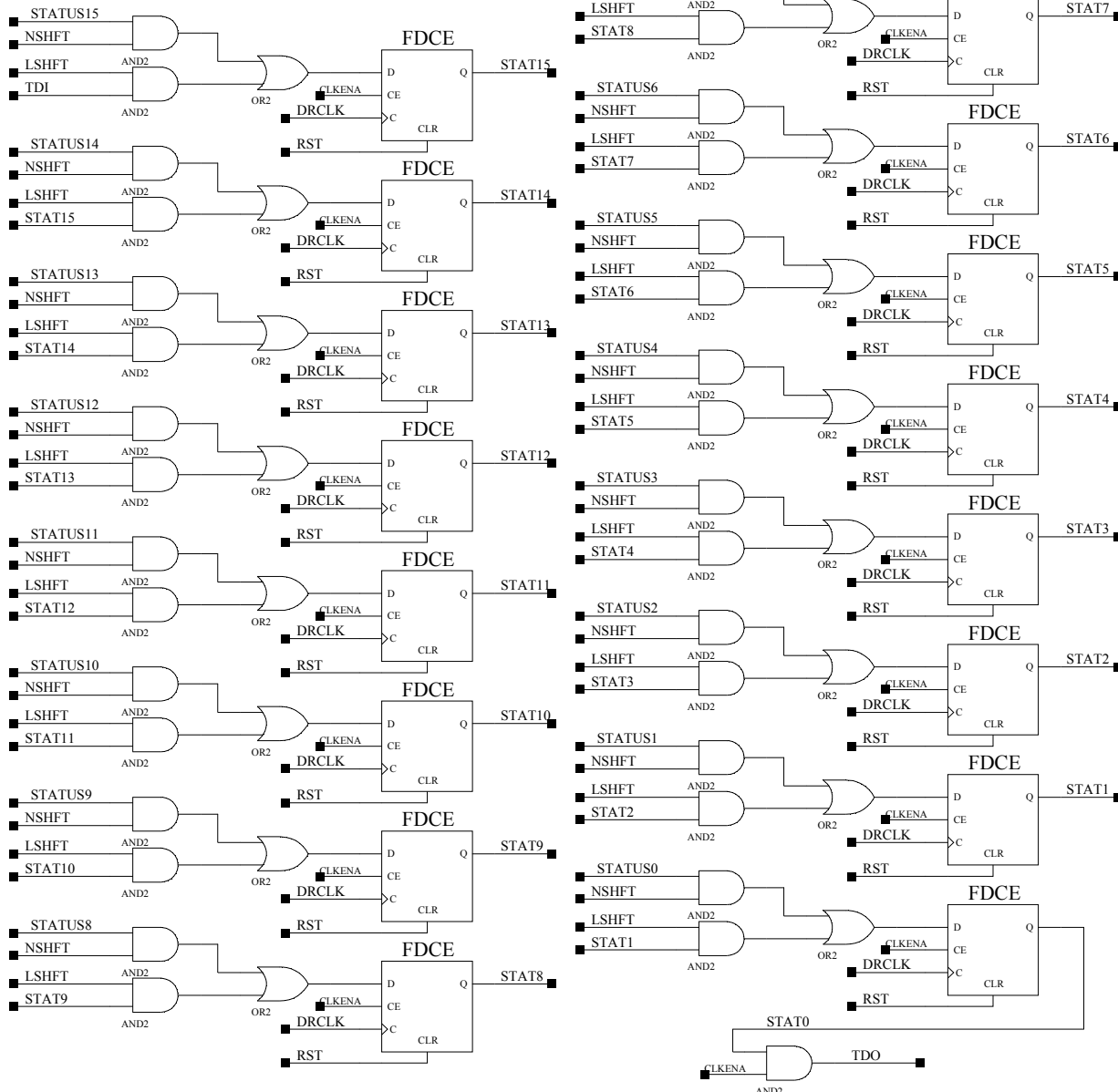
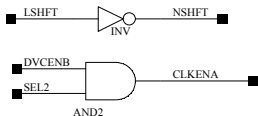
STATUS14  
STATUS13  
STATUS12  
STATUS11  
STATUS10  
STATUS9  
STATUS8  
STATUS7  
STATUS6  
STATUS5  
STATUS4  
STATUS3  
STATUS2  
STATUS1  
STATUS0



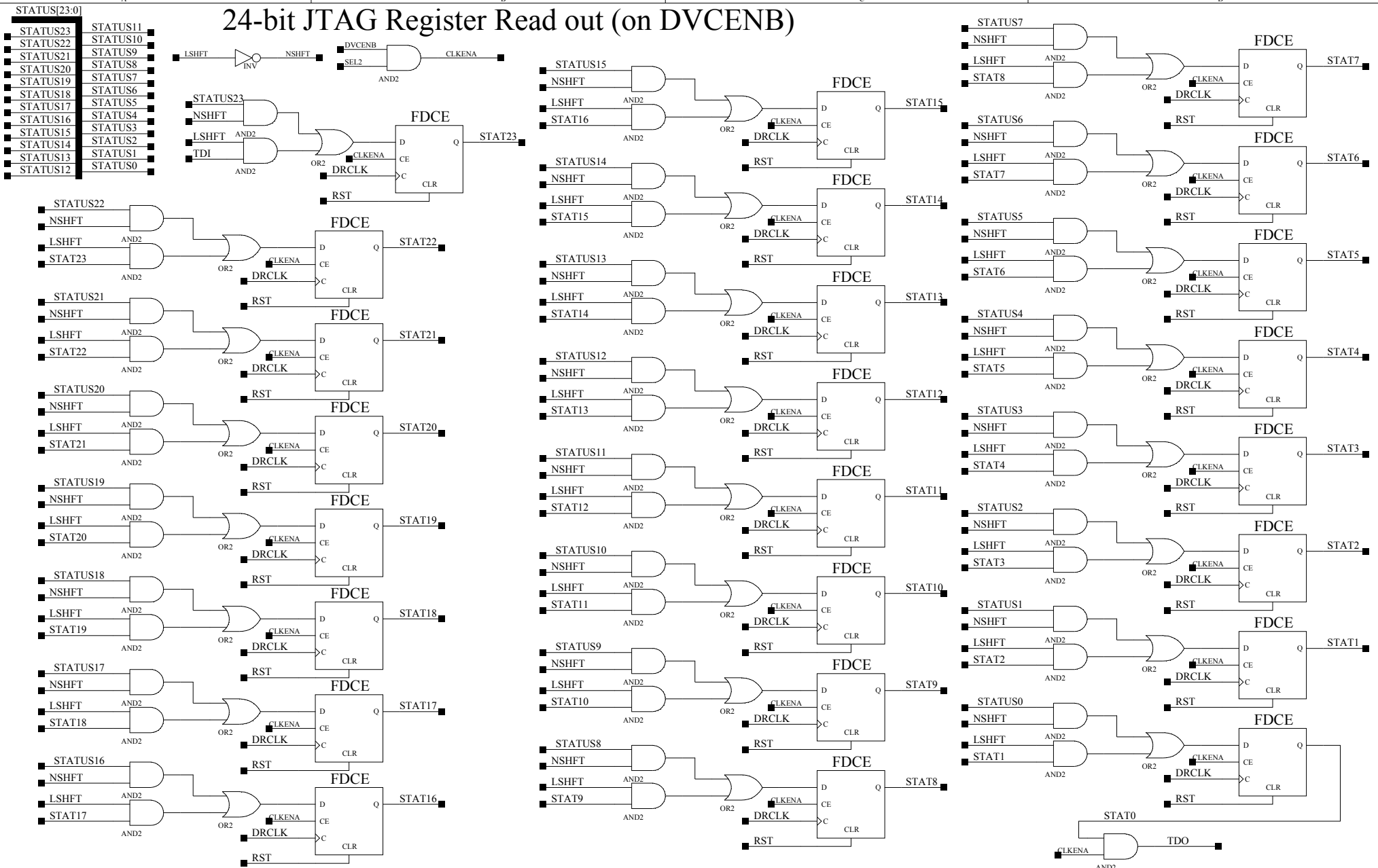
# 16-bit JTAG Register Read out (on DVCENB)

STATUS[15:0]

STATUS15  
STATUS14  
STATUS13  
STATUS12  
STATUS11  
STATUS10  
STATUS9  
STATUS8  
STATUS7  
STATUS6  
STATUS5  
STATUS4  
STATUS3  
STATUS2  
STATUS1  
STATUS0



# 24-bit JTAG Register Read out (on DVCENB)



Q[11:0]



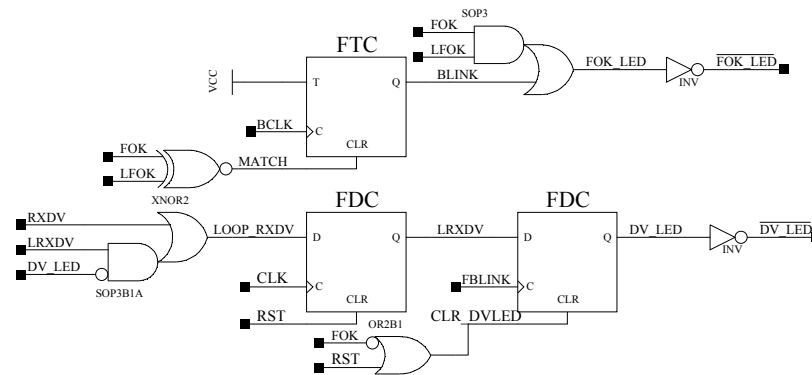
JRG

## FOK LED

- LIT == Link is alive and well
- BLINK == Link not ready
- OFF == Link not present

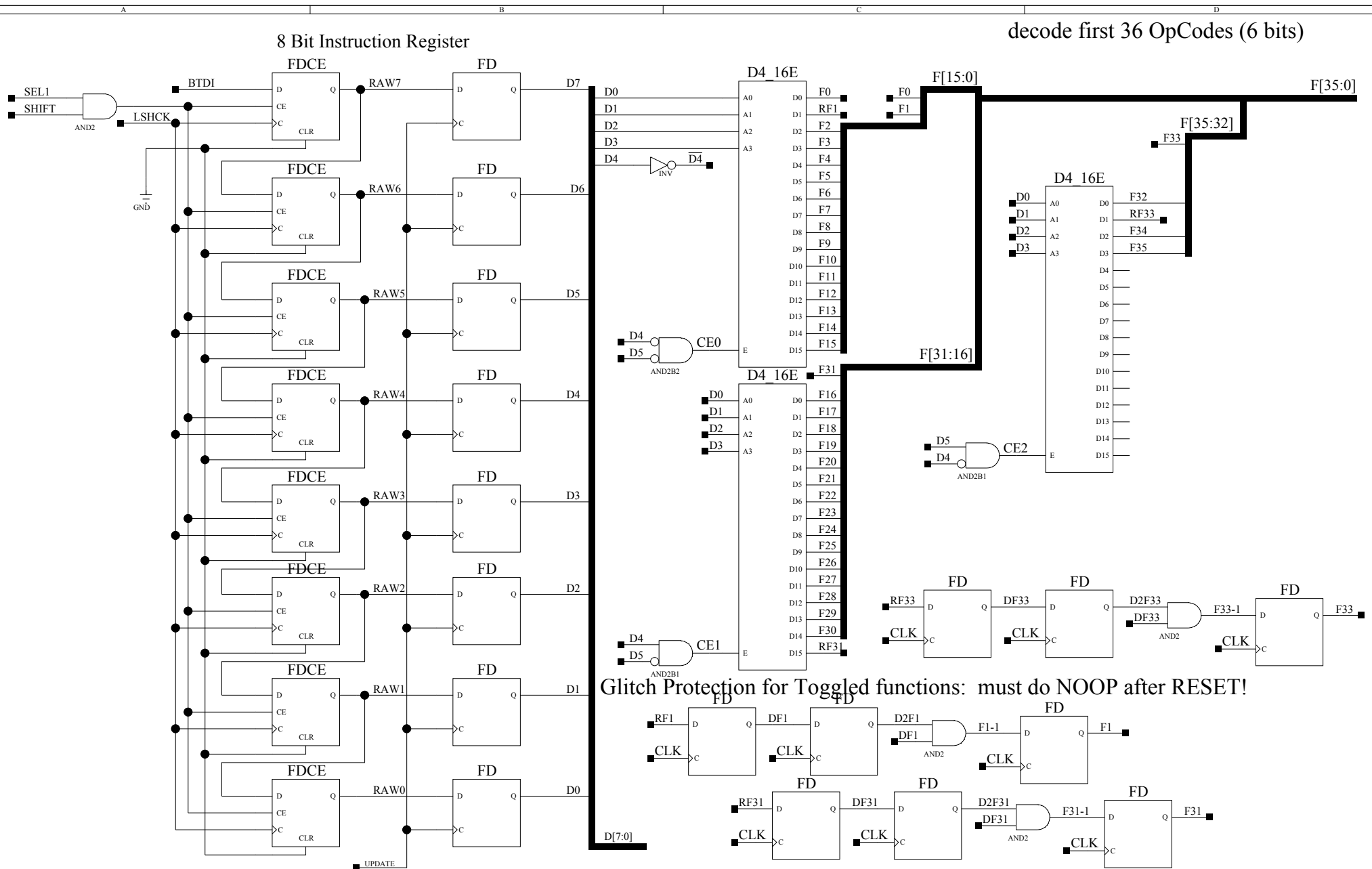
## DAV LED

- LIT == Active Data Xmit
- OFF == No data to Xmit

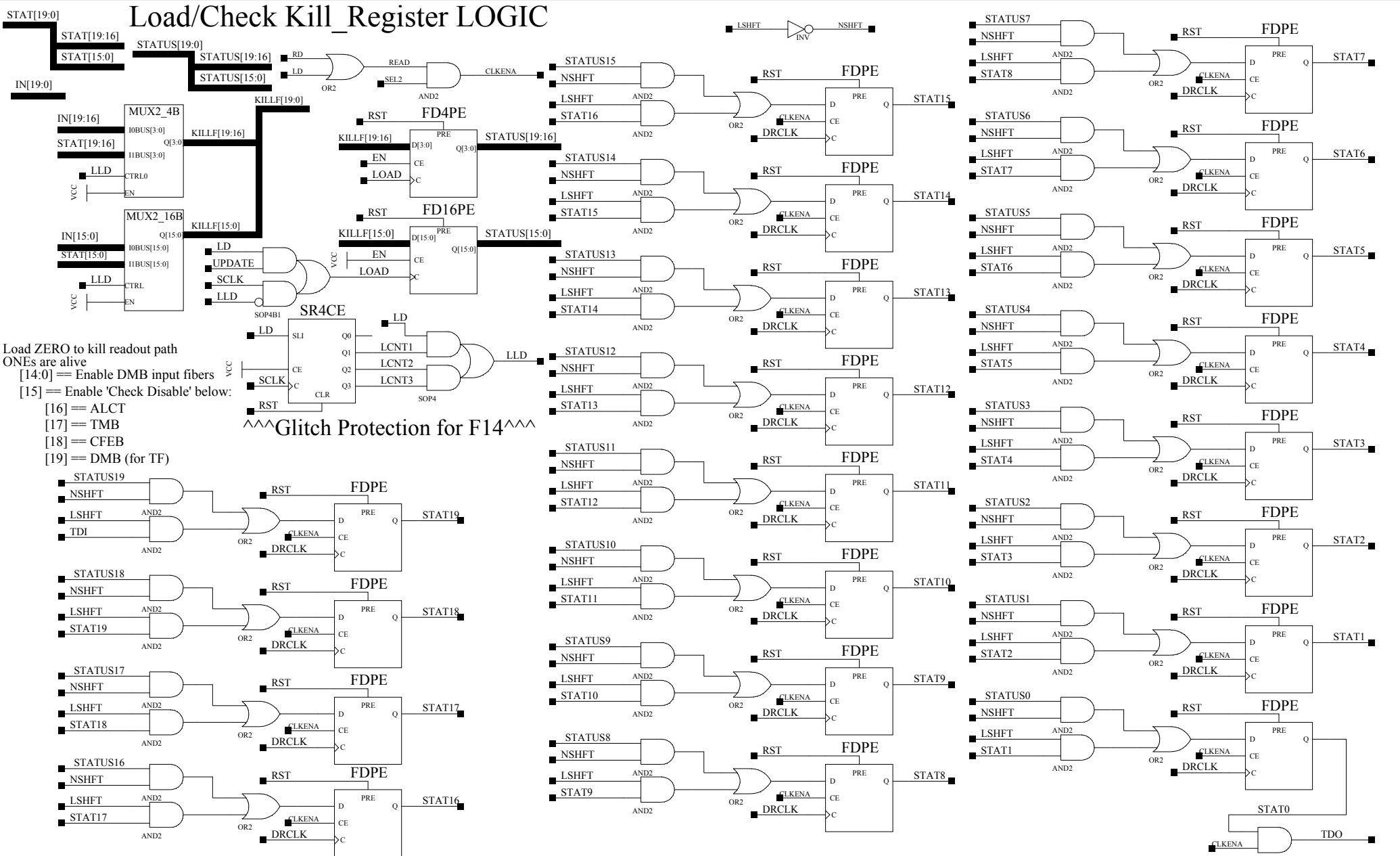


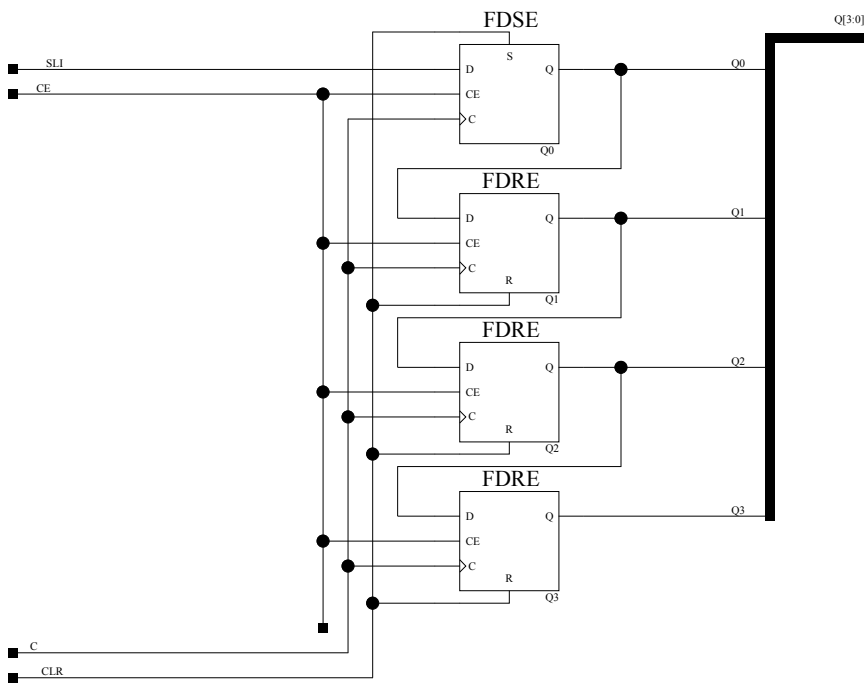
JRG

|               |                                                |
|---------------|------------------------------------------------|
| Title:        | FIBERLED                                       |
| Comments:     | Custom LED Slow-Blink Control for Fiber Inputs |
| Date:         | 27th January 2004                              |
| Ver:          | 1                                              |
| Sheet Size: B | Rev: A                                         |



# Load/Check Kill\_Register LOGIC

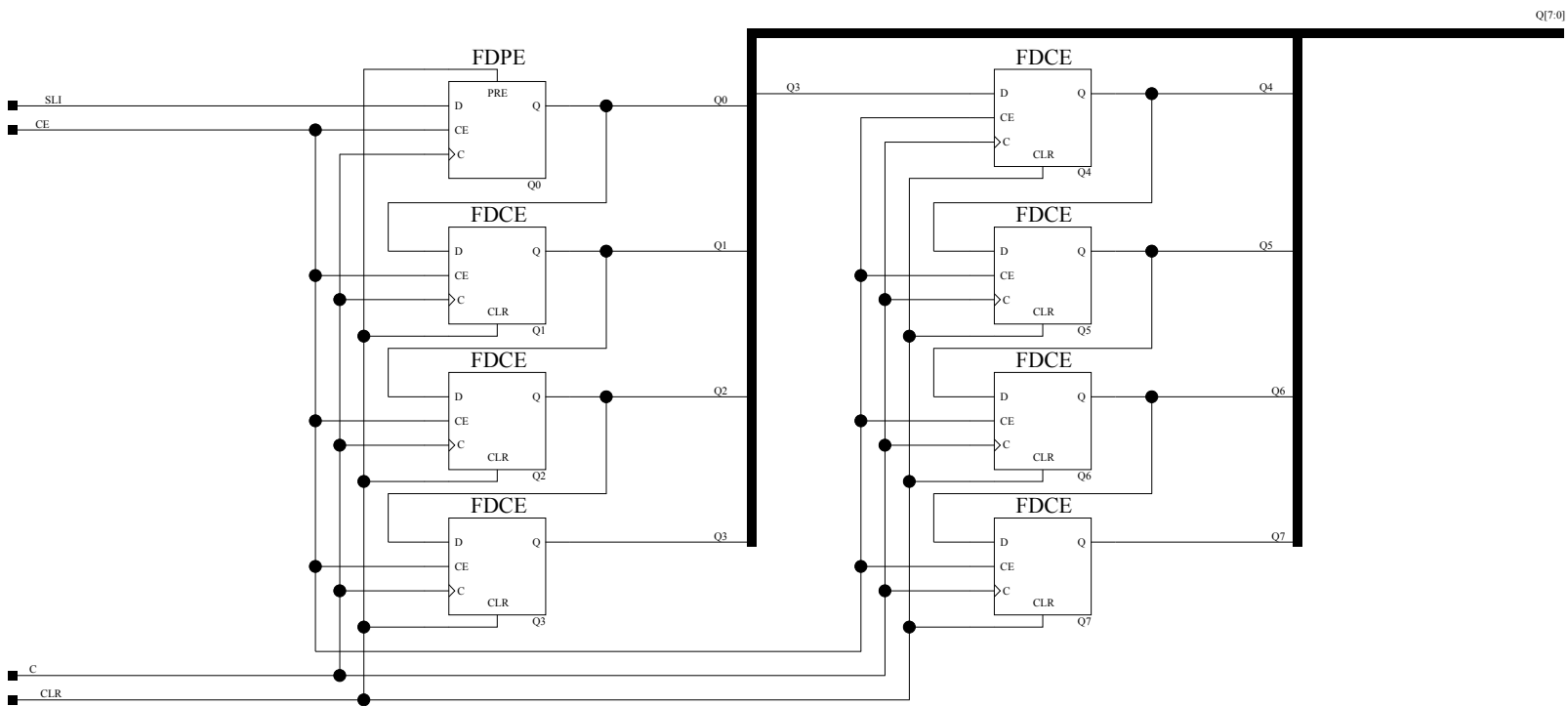


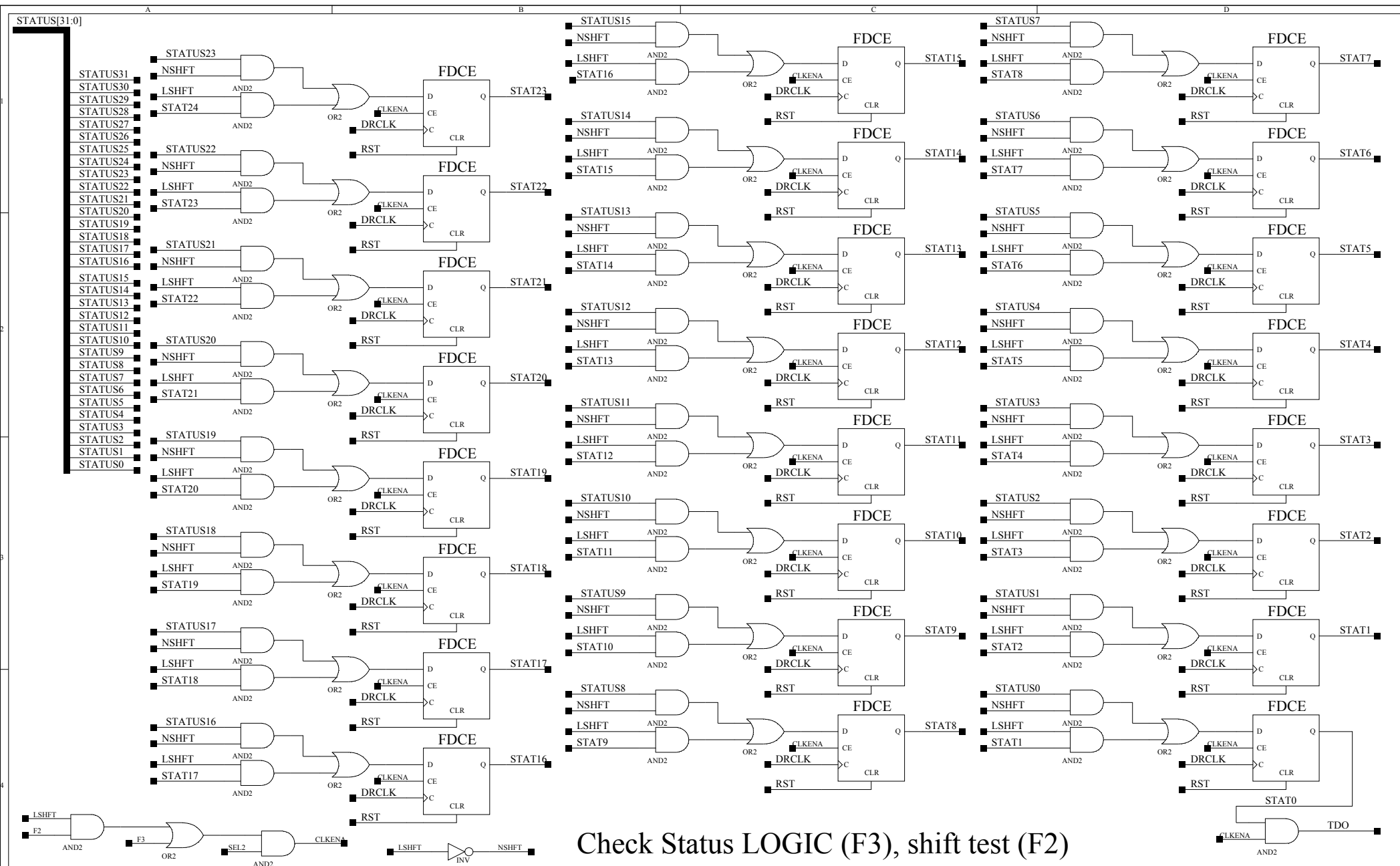


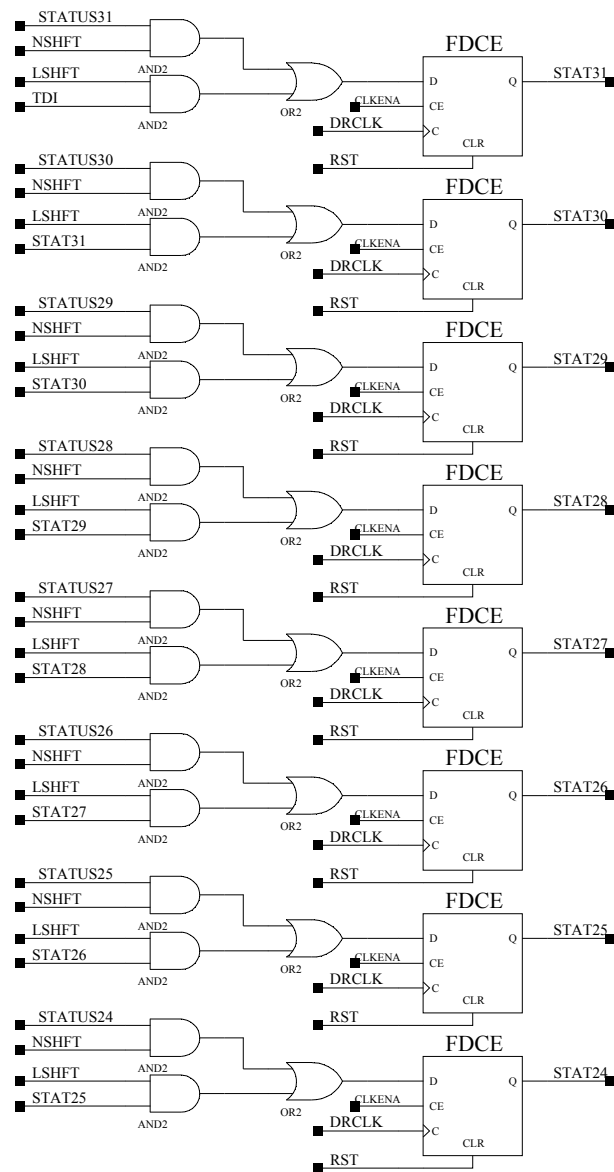
drawn by KS  
Copyright (c) 1993, Xilinx Inc.

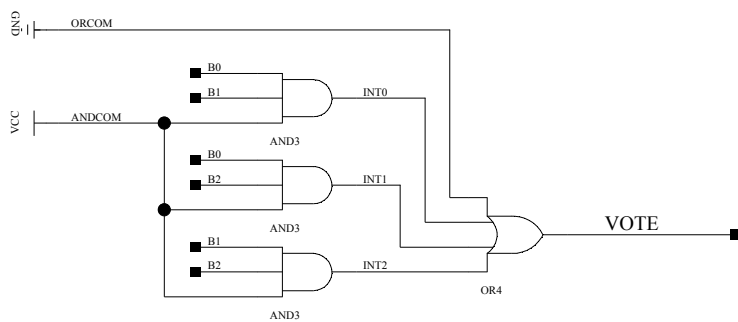


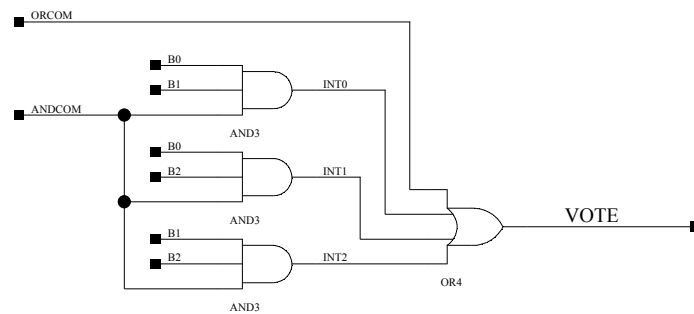
|               |                                                                                              |      |     |
|---------------|----------------------------------------------------------------------------------------------|------|-----|
| Title:        | VIRTEX Family SR4CE Macro                                                                    |      | JRG |
| Comments:     | 4-bit Serial-In Parallel-Out<br>Shift Register w/ Enable, loads a single "one" on Sync Reset |      |     |
| Date:         | 7th August 2001                                                                              | Ver: | 1   |
| Sheet Size: B |                                                                                              | Rev: | A   |











A[15:0]

B[15:0]

C[15:0]

VOTE[15:0]

