DAQMBC

CMS CSC DAQ Motherboard Control FPGA

Data Readout, Trigger Controller

MBCNTRL

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

2-14-2002_12:14

mojo

DAQMB Control FPGA Design

This FPGA coordinate the LCT, L1ACC signals, Control DATA transfer from CFEB, LCT/TMB to DDU. And CFEB calibration

Modification history:

Nov. 2, 2000: Redesign the FPGA logic, based on the new DAQMB PCB design, GU
Nov. 16, 2000: Finished first iteration design
Feb. 2, 2001: Move the design from m:\wv\d741mbc\ to m:\wv\cmsdaqmb\daqmbc\
Mar. 9, 2001: Major modifications, targeted device: XCV200E-FG456
Apr. 11, 2001: Loc pins according to PCB design
Aug. 1, 2001: Optimization of the design
Aug. 7, 2001: Modify the design to talk to Giga-bit Ethernet card
Aug. 30, 2001: Invert all the CCB related GTLP signals, because the CCB use inverted logic
Sept. 19, 2001: Add the CFEB data transfer error detection
Dec. 4, 2001: Add the Random Trigger, Trigger Rate Settable

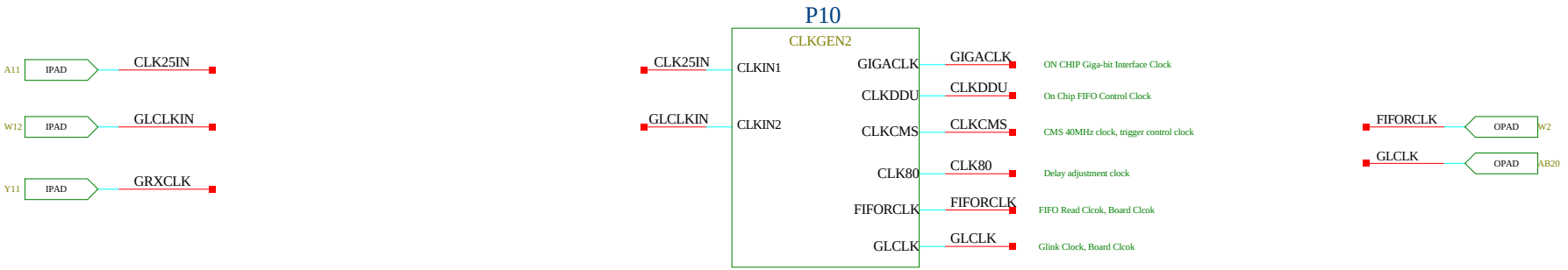
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Comment and Revision Information
DAQMB Controller
CMS CSC Electronics

BY: GU
PARENT PAGE:
PROJECT: DAQMBC
DATE: 3-18-2002_13:32
FILE: DAQMBC . 2
PAGE: 1A

For TLK2501, use 40MHz clock to generate 80MHz clock, CLKGEN1

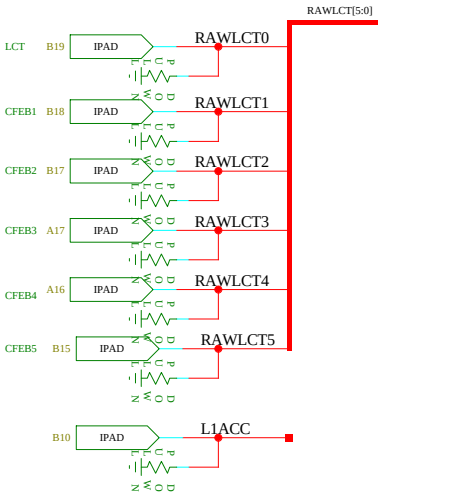
For TLK2201, use external clock as GLINK clock, CLKGEN2



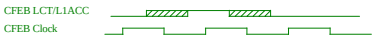
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Top Level DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 1	PROJECT: DAQMBC
		DATE: 3-18-2002_13:32	FILE: MBCNTRL . 1	PAGE: 2

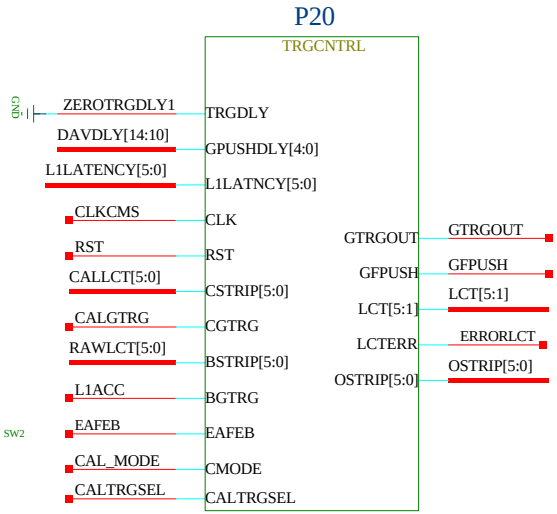
L1LATENCY[5:0]: Set by JTAG; Fixed for fixed pheripheral crate setup
For LCTdelay 500ns, L1Acc delay 3.2us, set to 0F

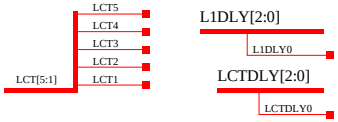
Minimize the LCT & L1ACC delay on DAQMB



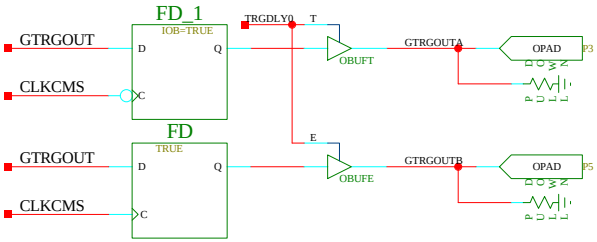
TRGDLY[1:0] is the fine delay
TRGDLY1: One clock cycle delay, TRGDLY0: half clock cycle delay
TRGDLY0 is used to adjust the LCT/L1ACC phase relative to CFEB clock.
TRGDLY1 is used to adjust the cable length 0 for 4-8m, 1 for 9m and longer

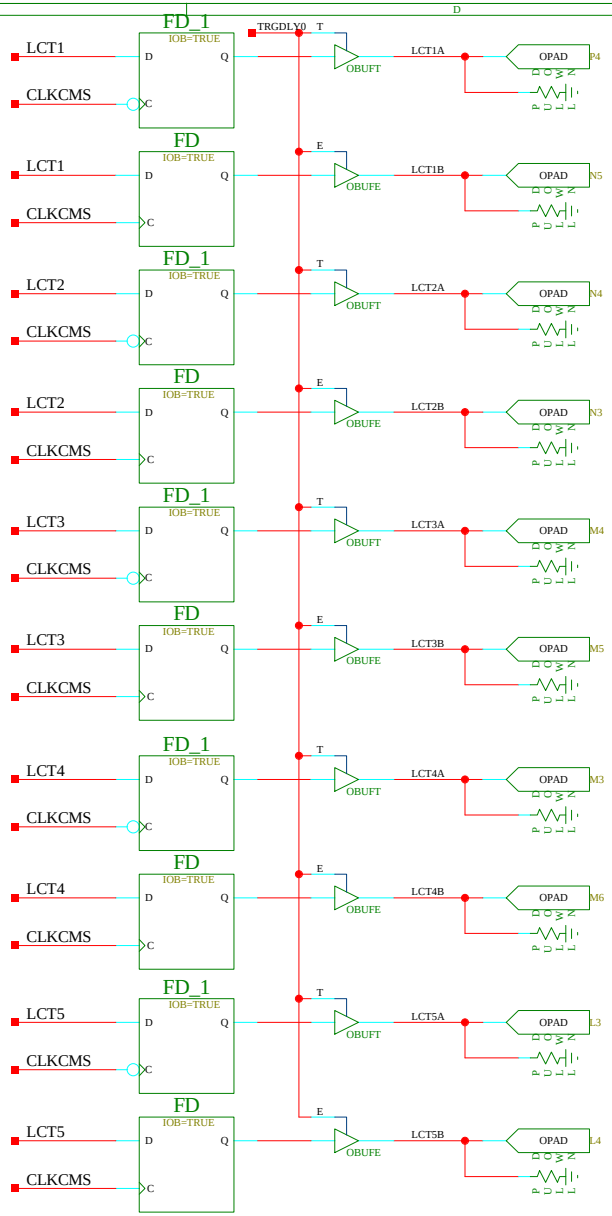






For other LEDs, refer to page 2D

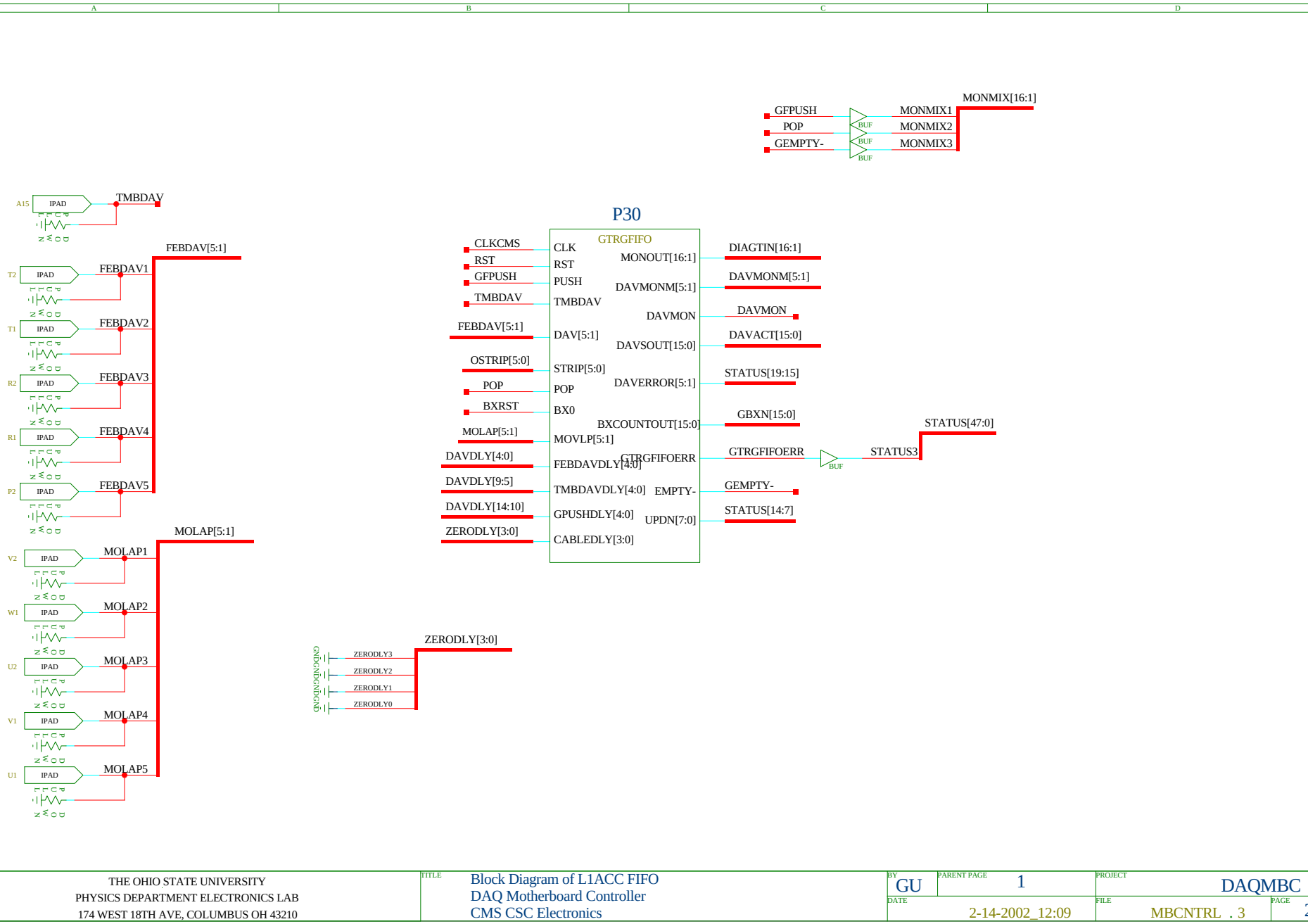




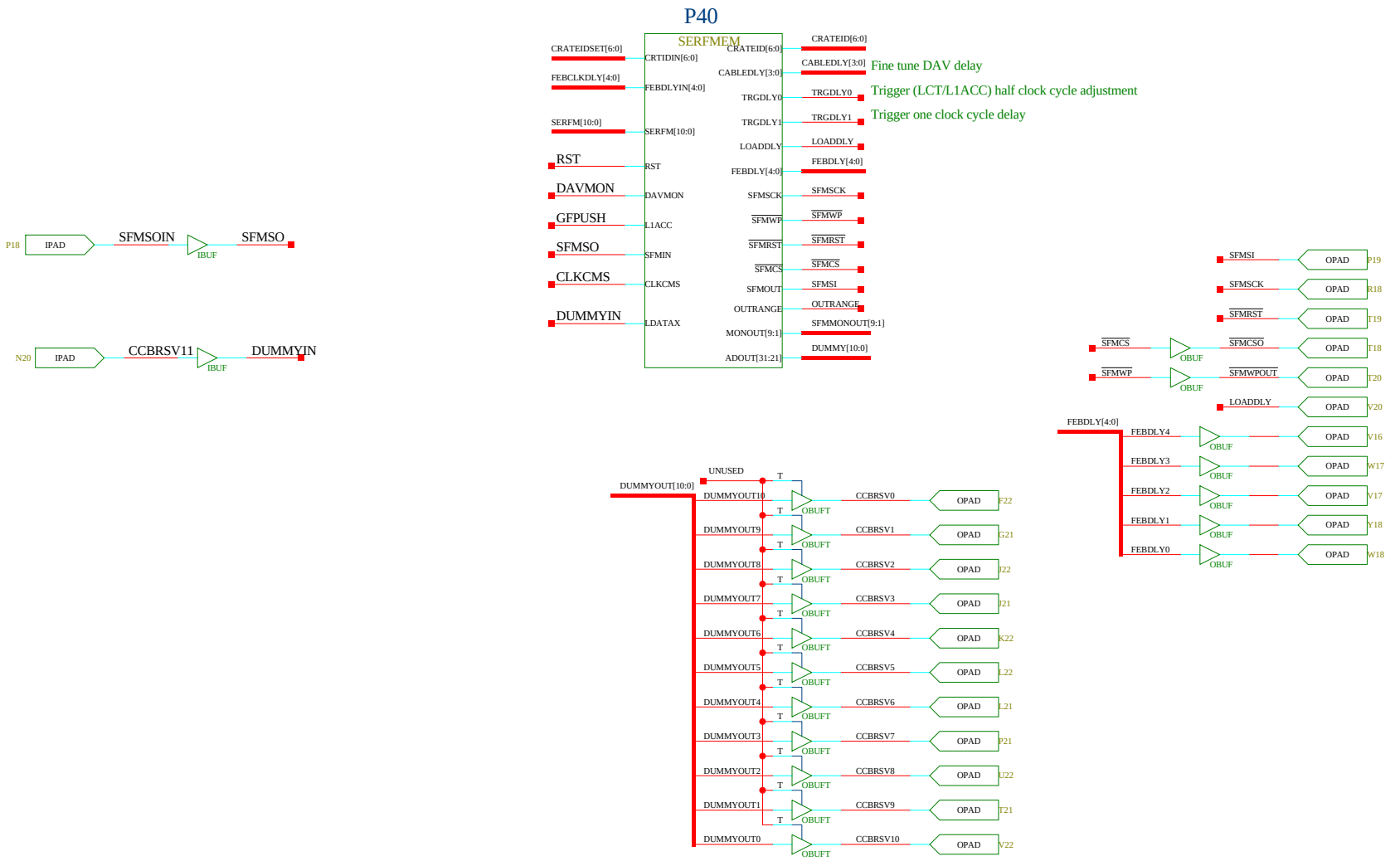
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Block Diagram of Trigger control
DAQ Motherboard Controller
CMS CSC Electronics

BY: GU
PARENT PAGE: 1
PROJECT: DAQMBC
DATE: 2-14-2002_12:09
FILE: MBCNTRL . 2
PAGE: 2A



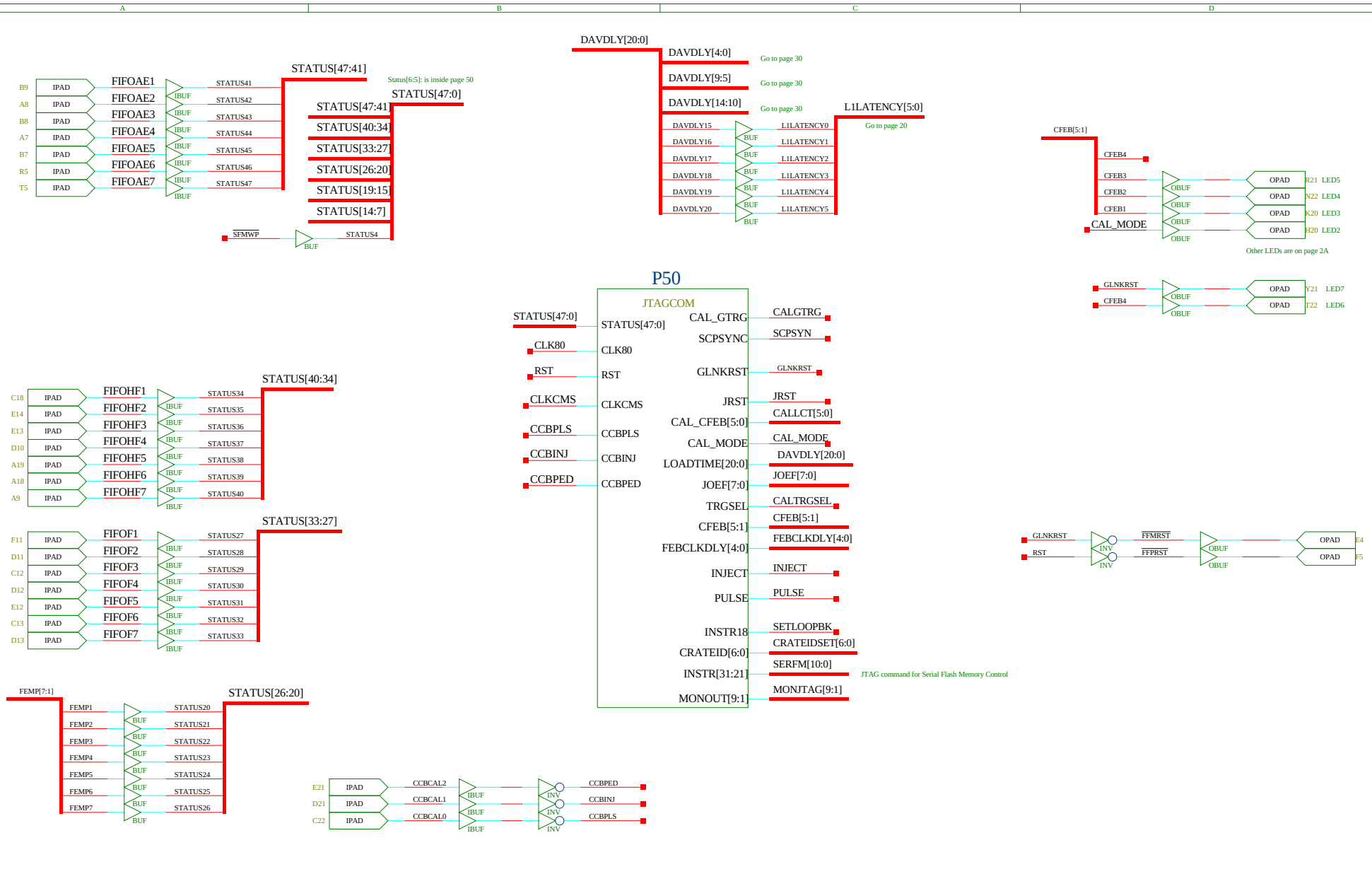
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Block Diagram of L1ACC FIFO DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 1	PROJECT: DAQMBC
		DATE: 2-14-2002_12:09	FILE: MBCNTRL . 3	PAGE: 2B



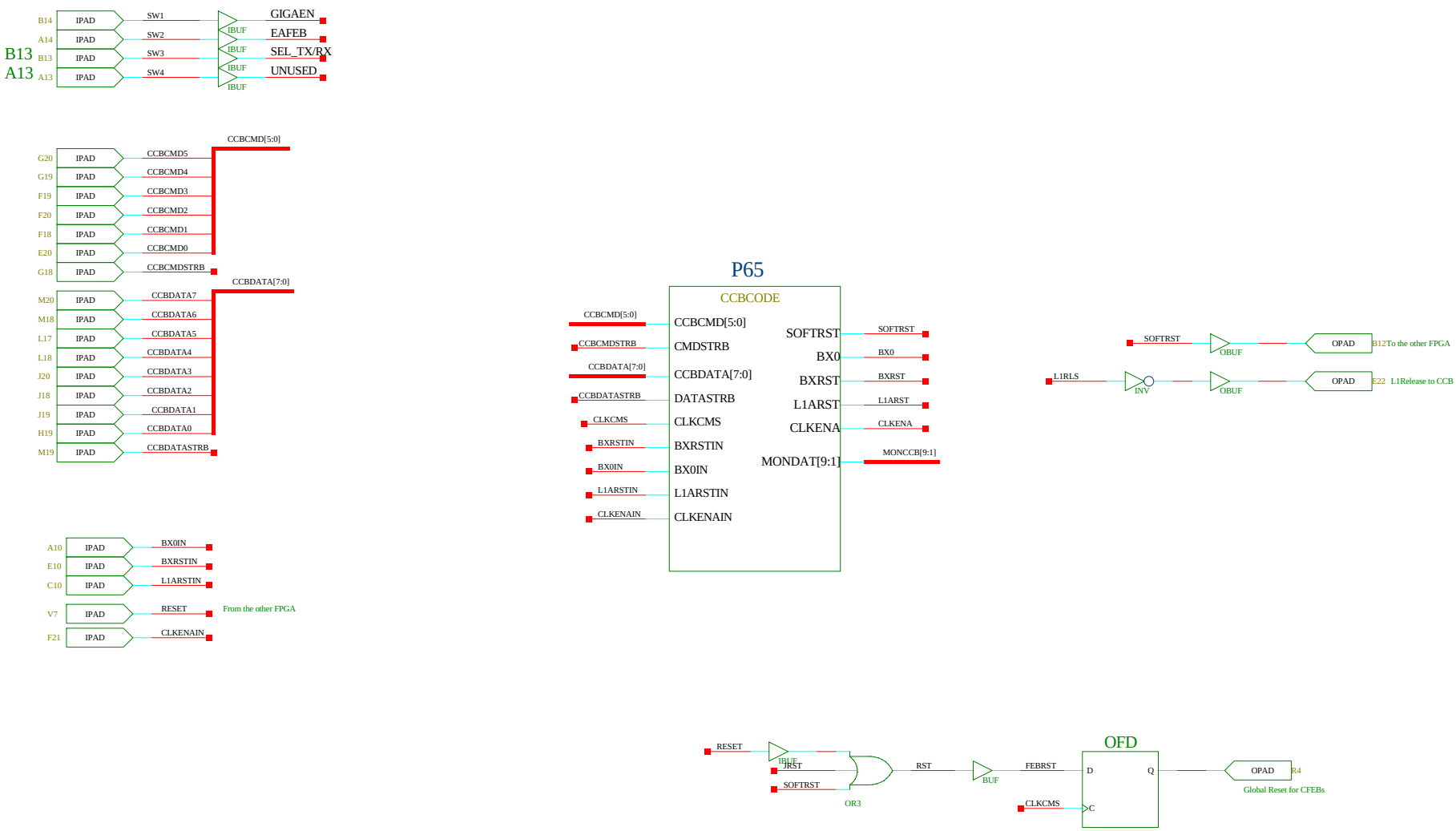
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Block Diagram of Serial Flash Memory Interface
DAQ Motherboard Controller
CMS CSC Electronics

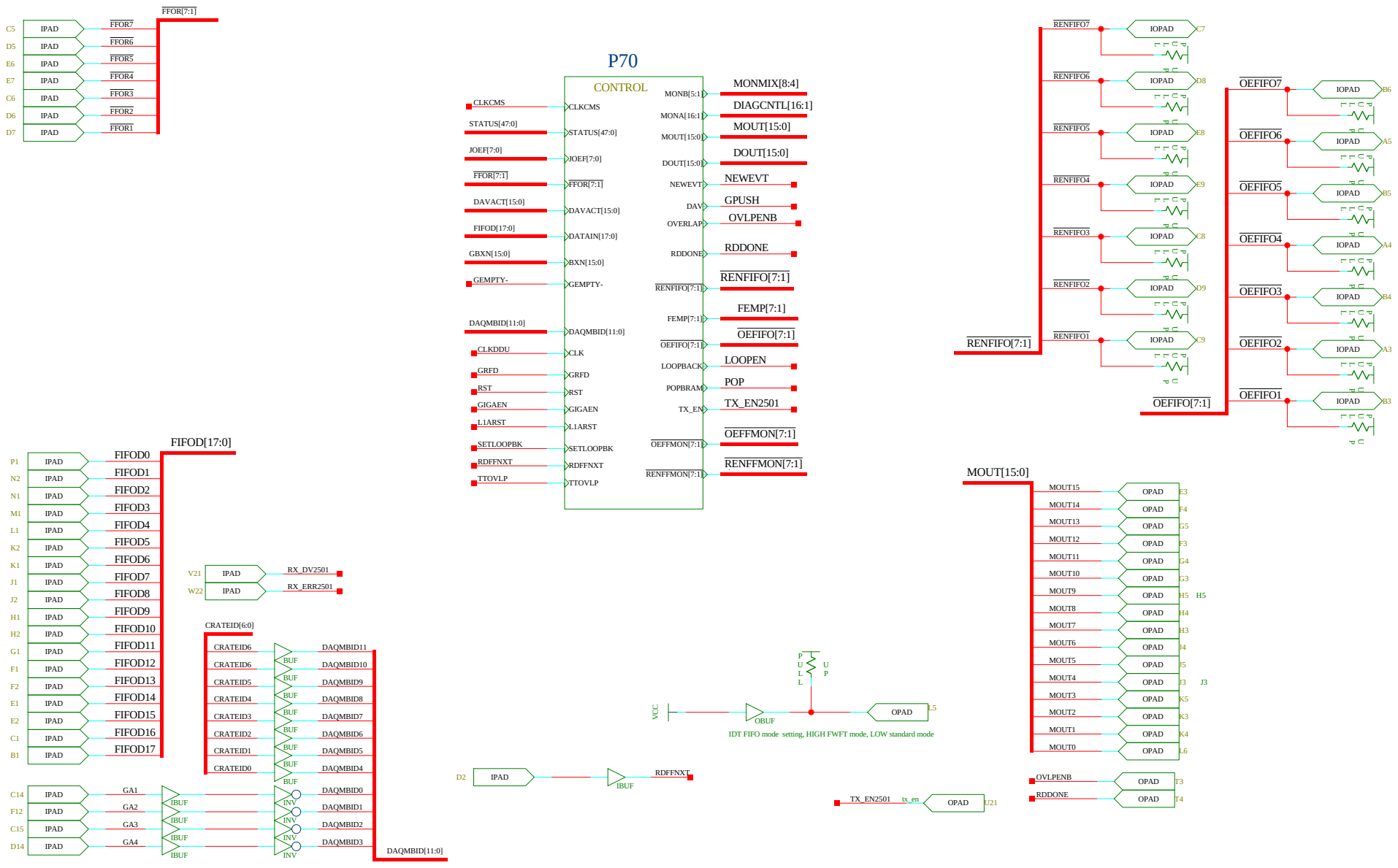
BY	PARENT PAGE	PROJECT
GU	1	DAQMBC
DATE		FILE / PAGE
1-14-2002_16:36		MBCNTRL . 4 / 2C



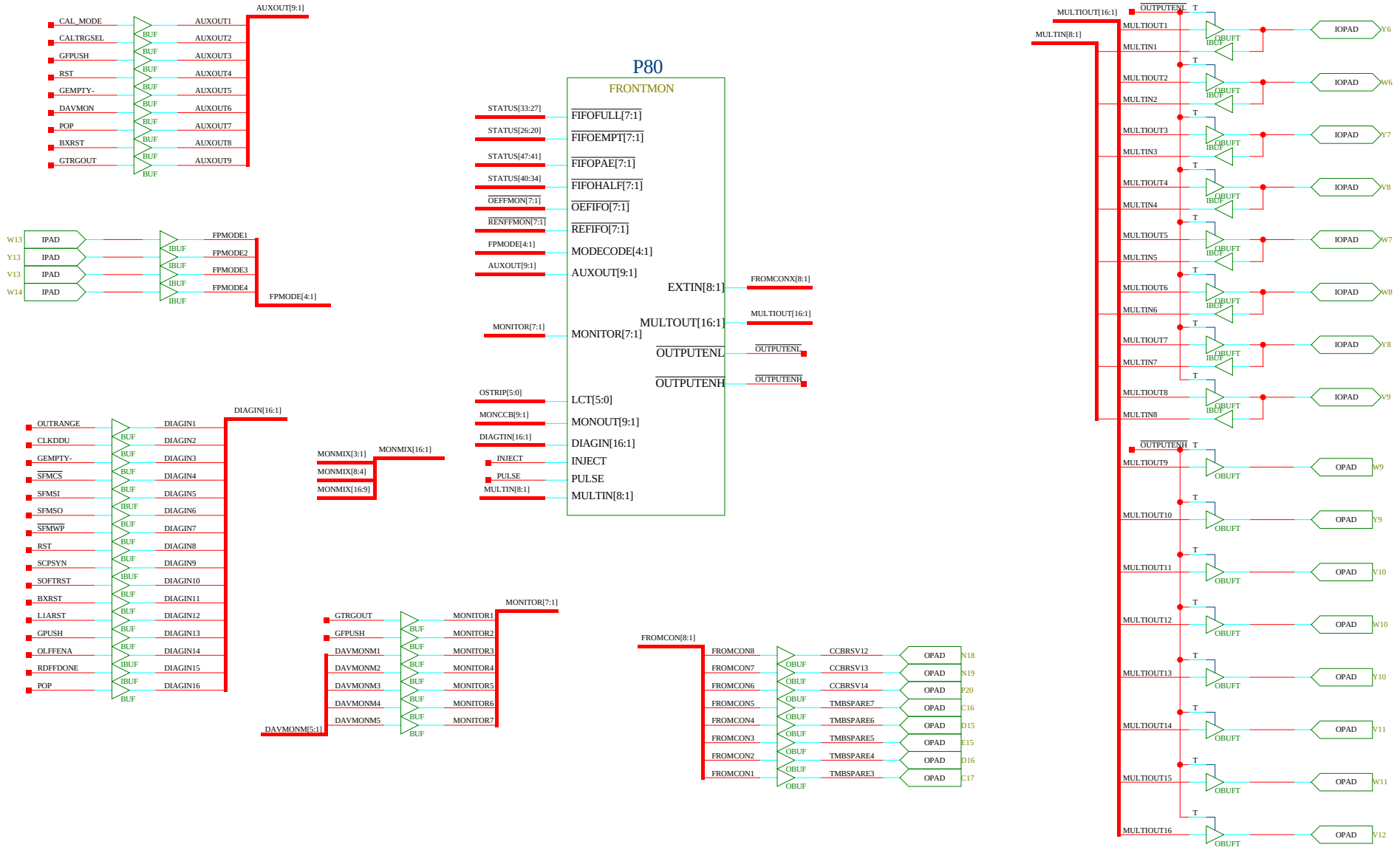
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Block Diagram DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2	PROJECT: DAQMBC
		DATE: 3-18-2002_13:32	FILE: MBCNTRL . 5	PAGE: 2D



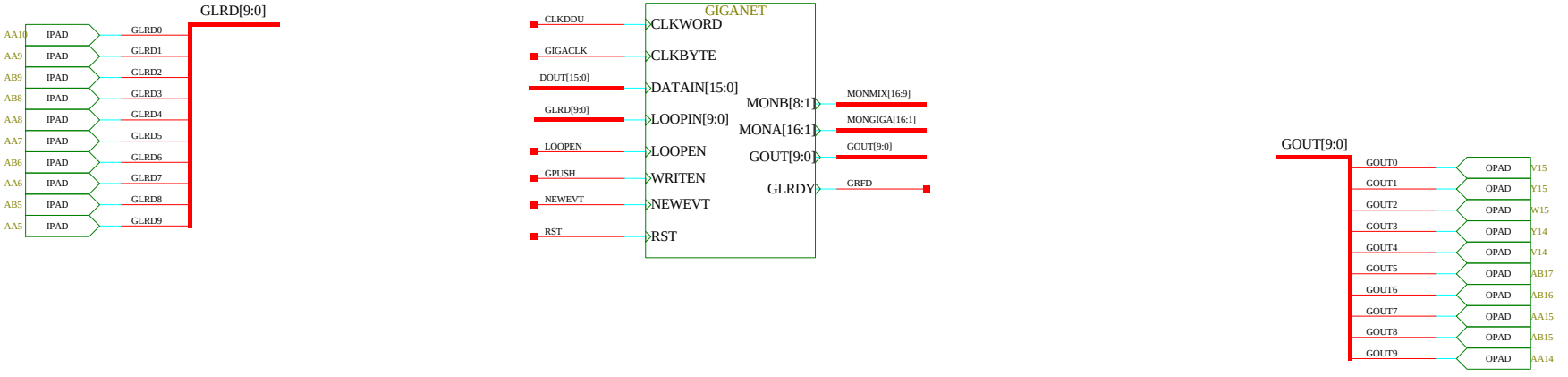
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Block Diagram of CCB fast control DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 1	PROJECT: DAQMBC
		DATE: 1-2-2002_14:01	FILE: MBCNTRL . 6	PAGE: 2E



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Block Diagram of FIFO Readout Controller DAQ Motherboard Controller CMS CSC Electronics	BY: GU PARENT PAGE: 1 DATE: 1-2-2002_14:01	PROJECT: DAQMBC FILE: MBCNTRL . 7 PAGE: 2F



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Block Diagram of Front Pannal Connector Control DAQ Motherboard Controller CMS CSC Electronics	BY: GU PARENT PAGE: 1 DATE: 2-14-2002_12:12	PROJECT: DAQMBC FILE: MBCNTRL . 8 PAGE: 2G

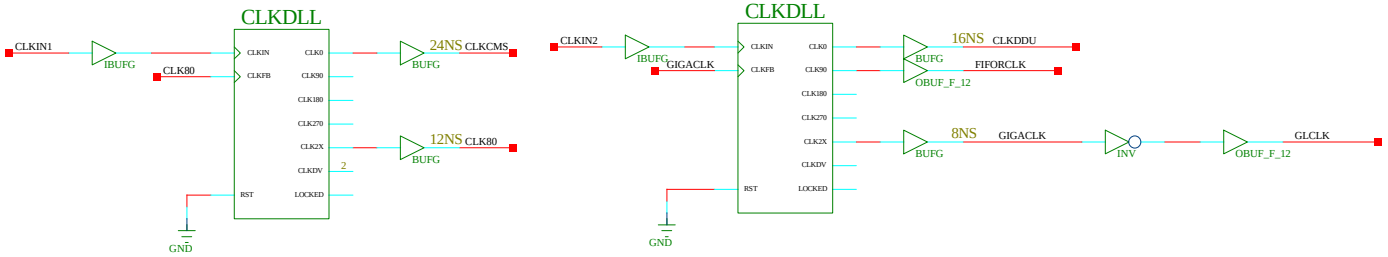


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Block Diagram of Giga Bit Ethernet readout Control
DAQ Motherboard Controller
CMS CSC Electronics

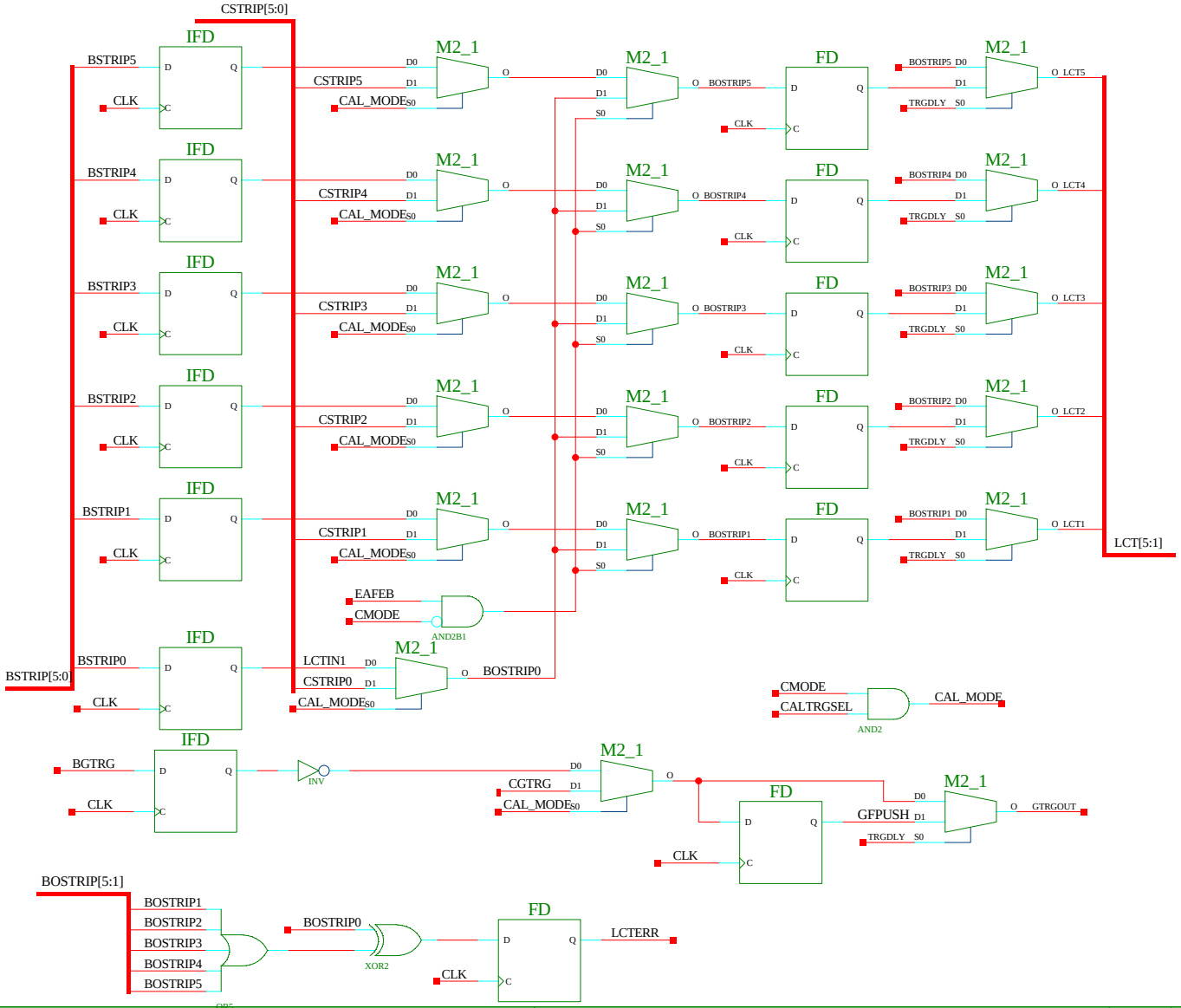
BY: GU
PARENT PAGE: 1
PROJECT: DAQMBC
DATE: 12-5-2001_16:44
FILE: MBCNTRL . 9
PAGE: 2H

For TLK2201, use external 62.5MHz clock as Glink clock



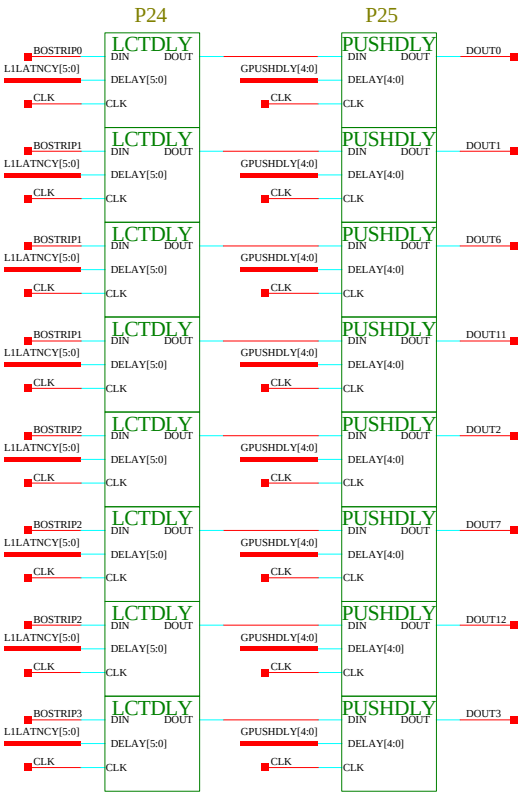
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	CLOCK generator, CMS clock and GLINK clock DAQ Motherboard Controller CMS CSC Electronics	BY GU DATE 9-26-2001_13:32	PARENT PAGE 2 FILE CLKGEN2 . 1
			PROJECT DAQMBC	PAGE 10

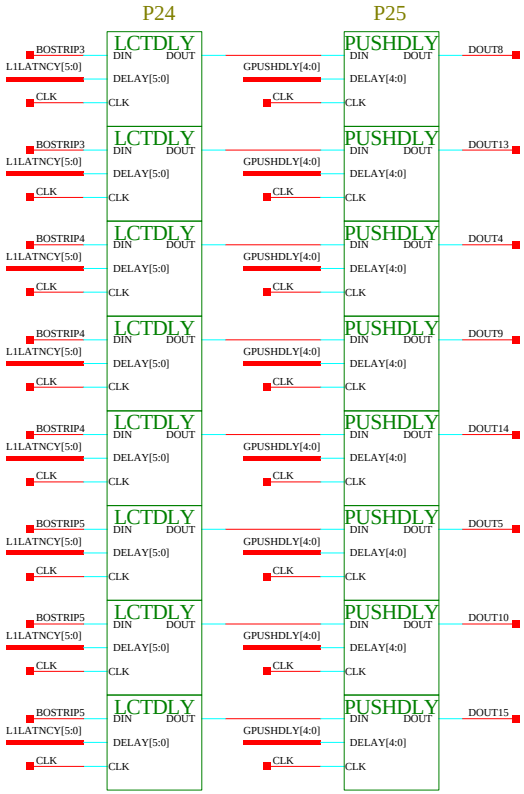
This IFD_1 is just used to sync with the Fake backplane, should do the change at Fake BP
Use IFD for real backplane to replace the IFD_1 and FD here

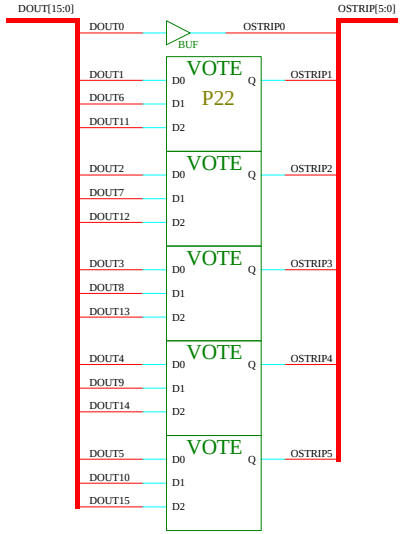


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: LCT/L1ACC Controller DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2A	PROJECT: DAQMBC	
		DATE: 1-2-2002_14:47		FILE: TRGCNTRL . 1	PAGE: 20

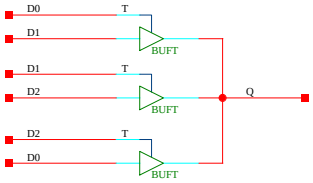
LCT delay for the length of L1 Latency, and take into account of one clock cycle uncertainty to match with L1ACC







THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: LCT Delay, +- one BX for LCT, and triple voting DAQ Motherboard Controller CMS CSC Electronics	BY: GU PARENT PAGE: 2A DATE: 1-2-2002_15:17	PROJECT: DAQMBC FILE: TRGCNTRL . 2 PAGE: 20A



Voting logic
DAQMB Controller
CMS CSC ELECTRONICS

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

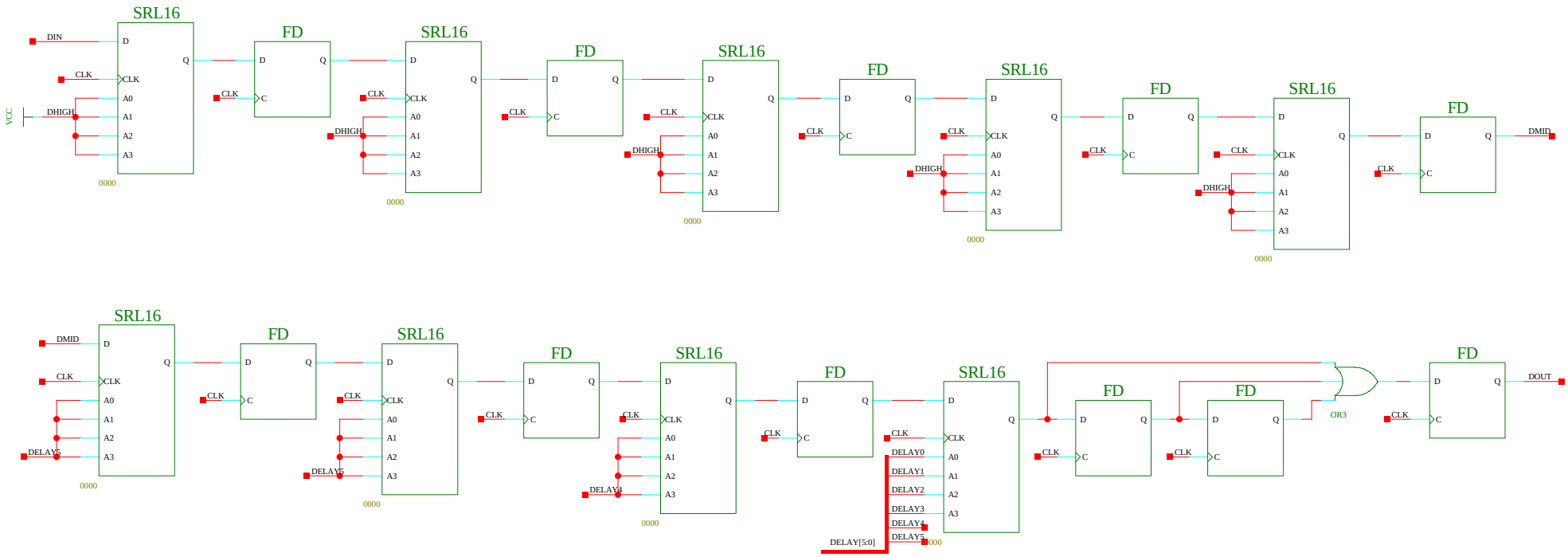
TITLE

PARENT PAGE		PROJECT	
GU	20A		DAQMBC

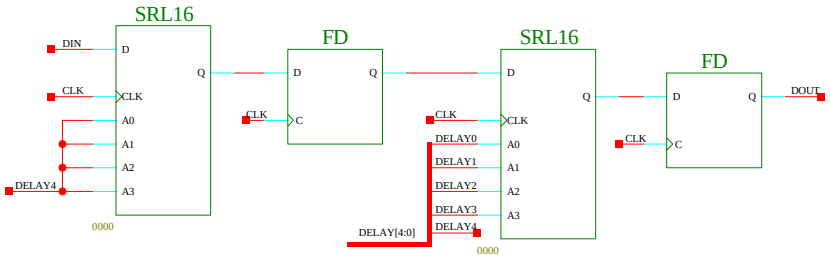
BY	DATE	FILE		PAGE
	3-18-2002_13:32	VOTE	1 .	22

Total delay: (2350 + 750*delay5 + 375*delay4 + 200*delay3 + 100*delay2 + 50*delay1 + 25*delay0)ns

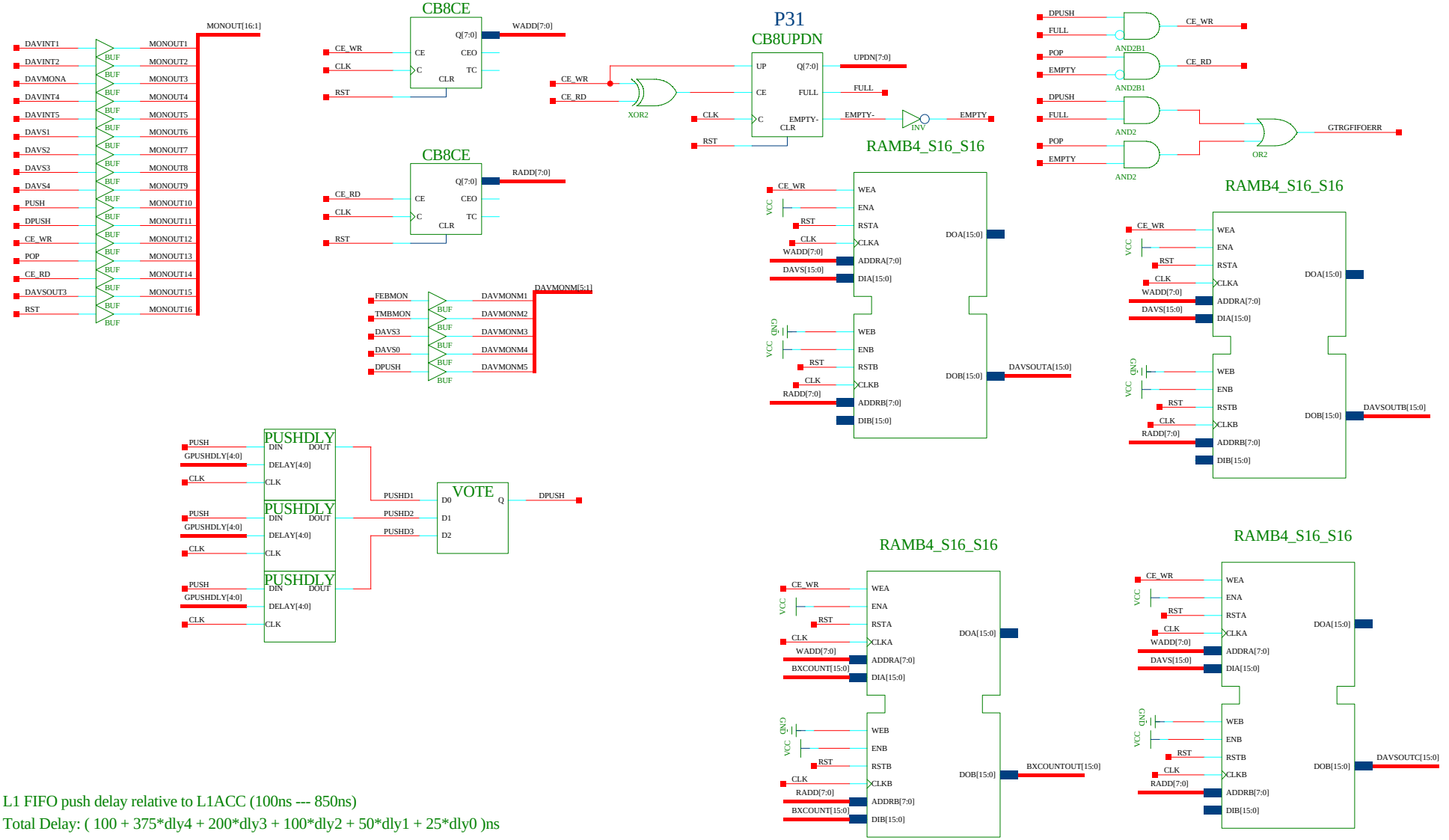
set the Delay as 011000, so the delay of mid-one is 29025ns, to match with current CFEB --Jan. 2, 2002



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Delay logic DAQMB Controller CMS CSC ELECTRONICS	BY: GU	PARENT PAGE: 20A	PROJECT: DAQMBC
		DATE: 1-2-2002_13:25	FILE: LCTDLY . 1	PAGE: 24



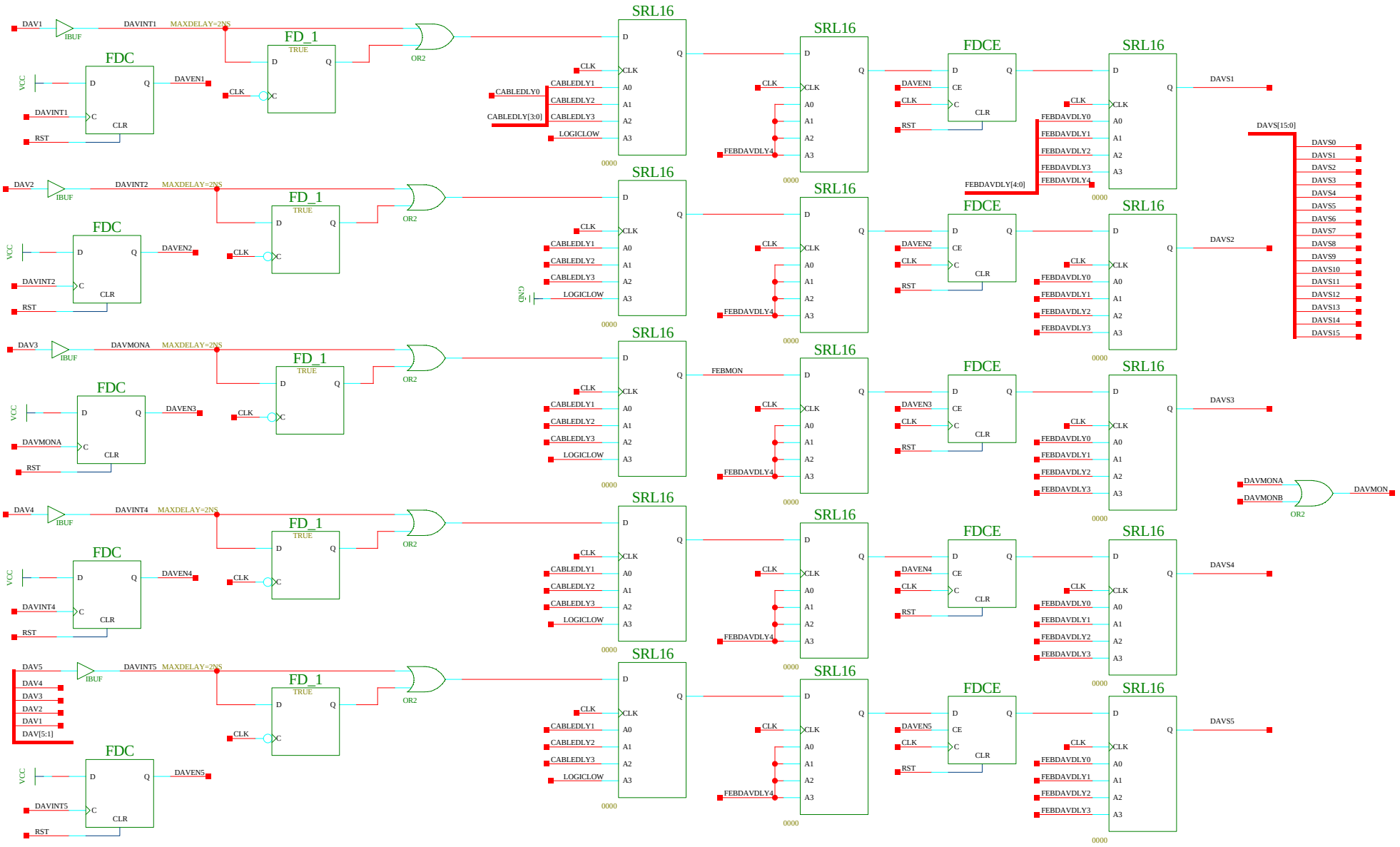
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Delay logic for PUSH waiting DAQMB Controller CMS CSC ELECTRONICS	BY: GU	PARENT PAGE: 20A	PROJECT: DAQMBC
		DATE: 1-2-2002_14:54	FILE: PUSHDLY . 1	PAGE: 25



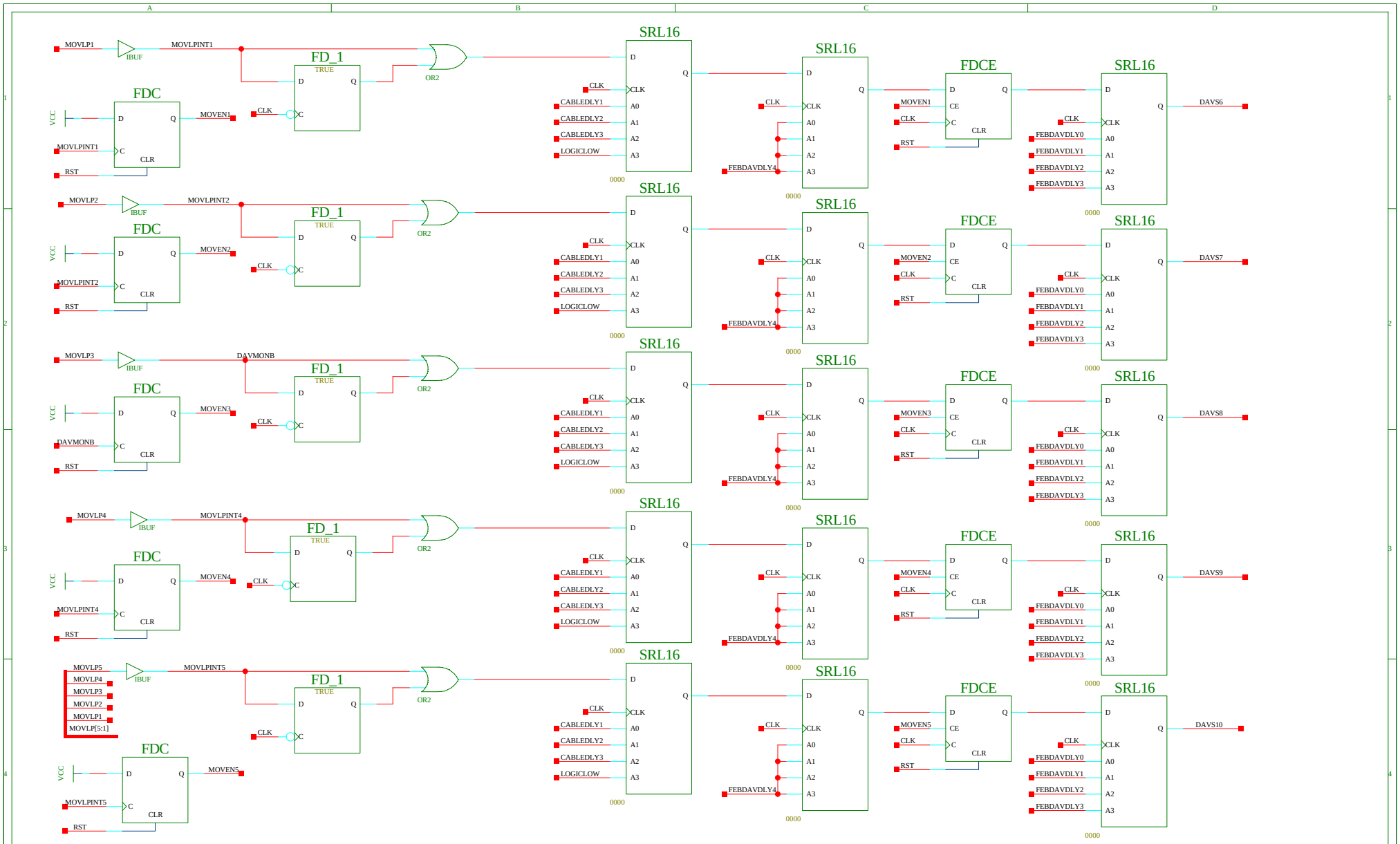
L1 FIFO push delay relative to L1ACC (100ns --- 850ns)

Total Delay: (100 + 375*dly4 + 200*dly3 + 100*dly2 + 50*dly1 + 25*dly0)ns

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: L1ACC FIFO Register DAQ Motherboard Controller CMS CSC Electronics	BY: GU DATE: 2-14-2002_12:08	PARENT PAGE: 2B FILE: GTRGFIFO. 1
		PROJECT: DAQMBC	PAGE: 30



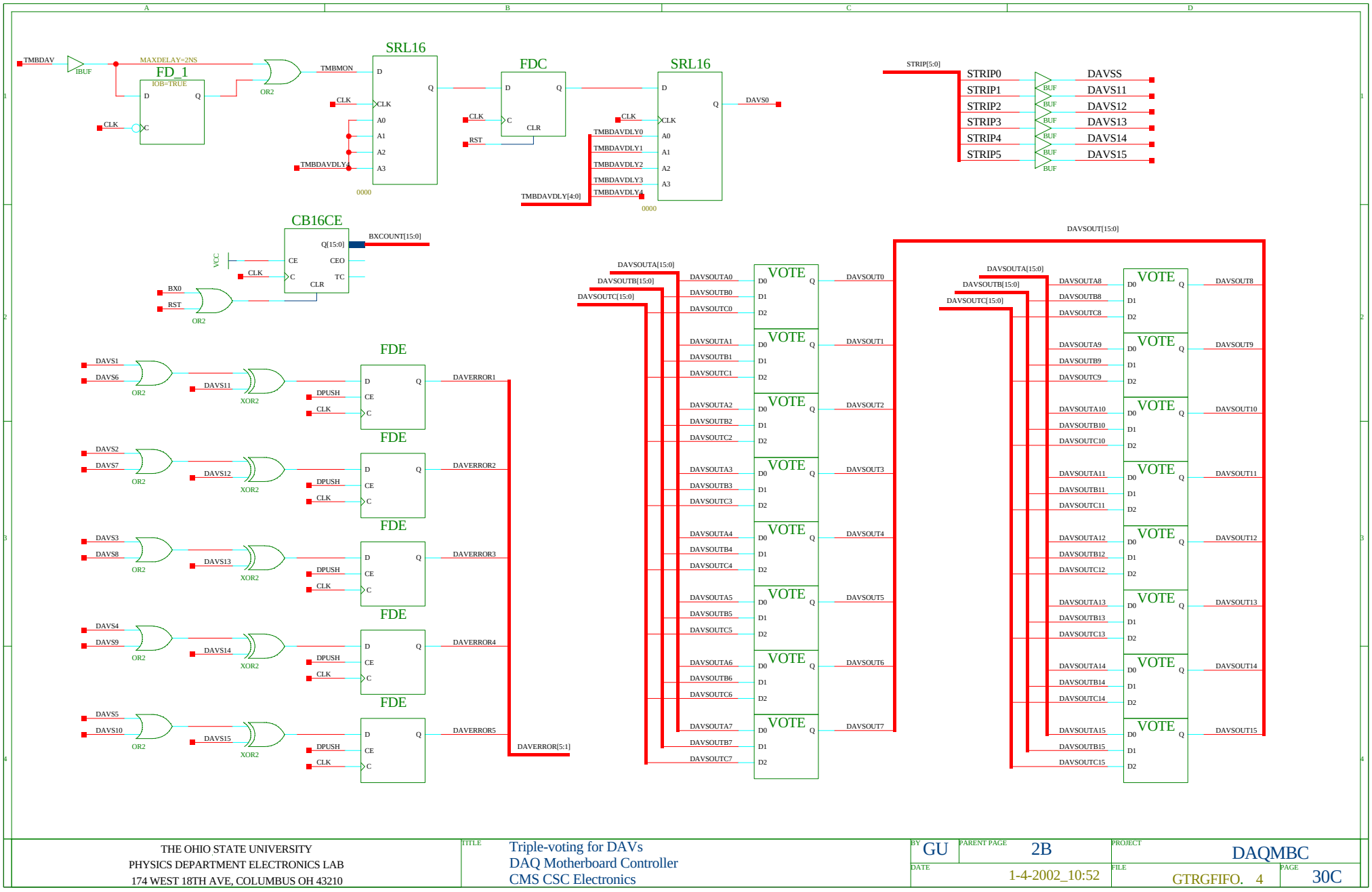
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CFEB DAV Delay DAQ Motherboard Controller CMS CSC Electronics	BY: GU DATE: 1-4-2002_11:42	PARENT PAGE: 2B FILE: GTRGFIFO. 2
		PROJECT: DAQMBC	PAGE: 30A



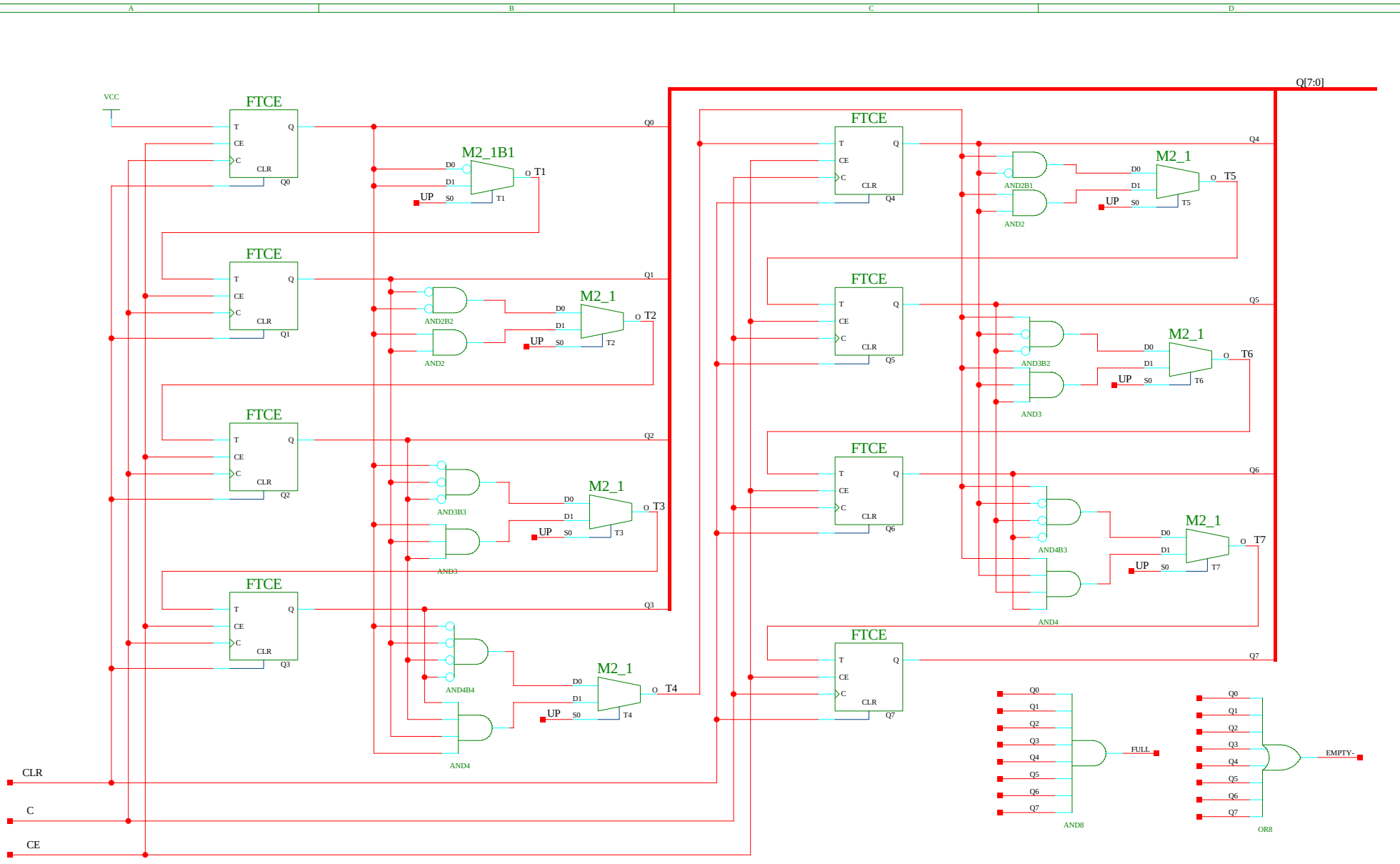
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: CFEB Multi-Overlap Delay
DAQ Motherboard Controller
CMS CSC Electronics

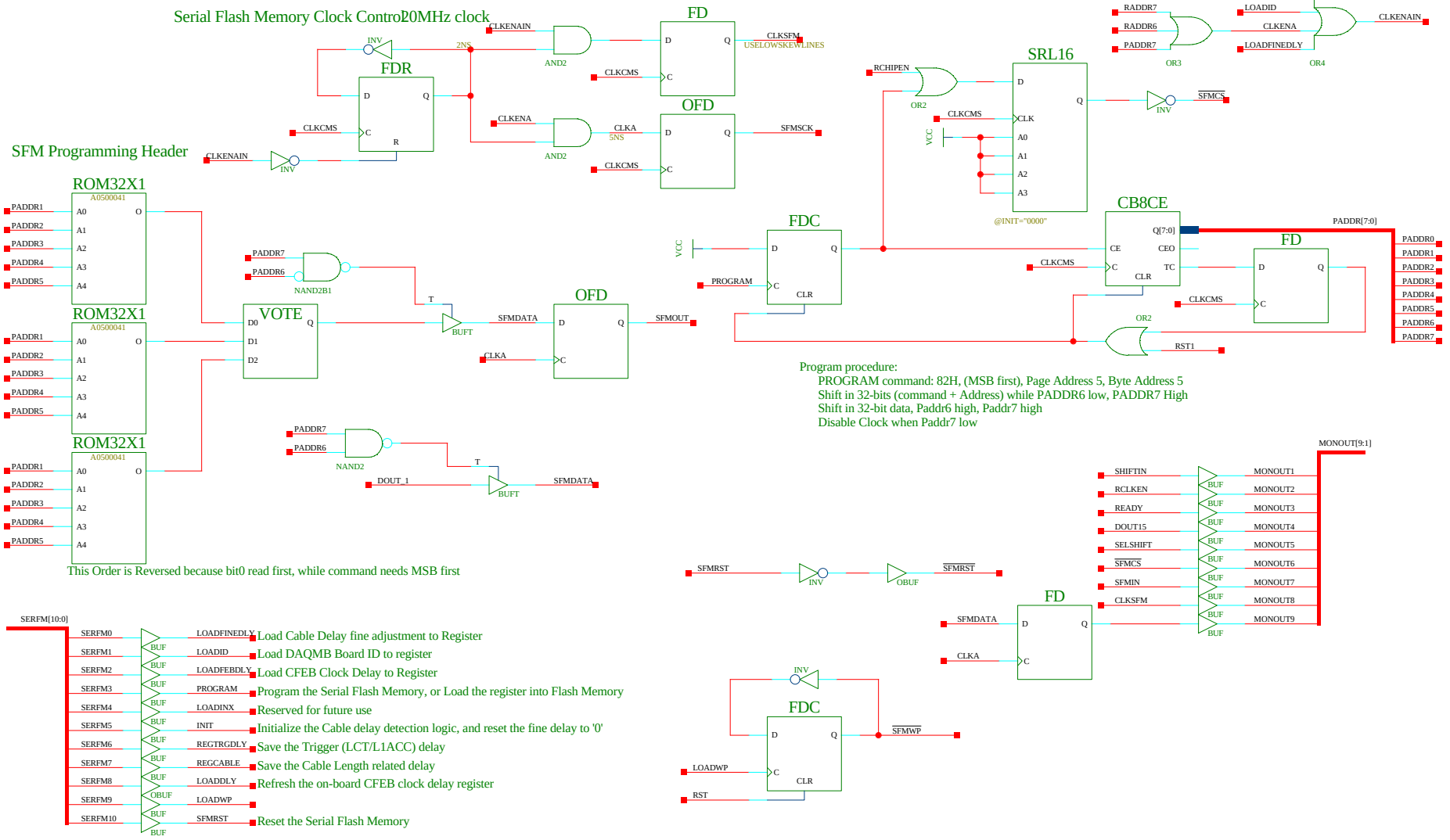
BY: GU
PARENT PAGE: 2B
PROJECT: DAQMBC
DATE: 1-4-2002_11:42
FILE: GTRGFIFO. 3
PAGE: 30B



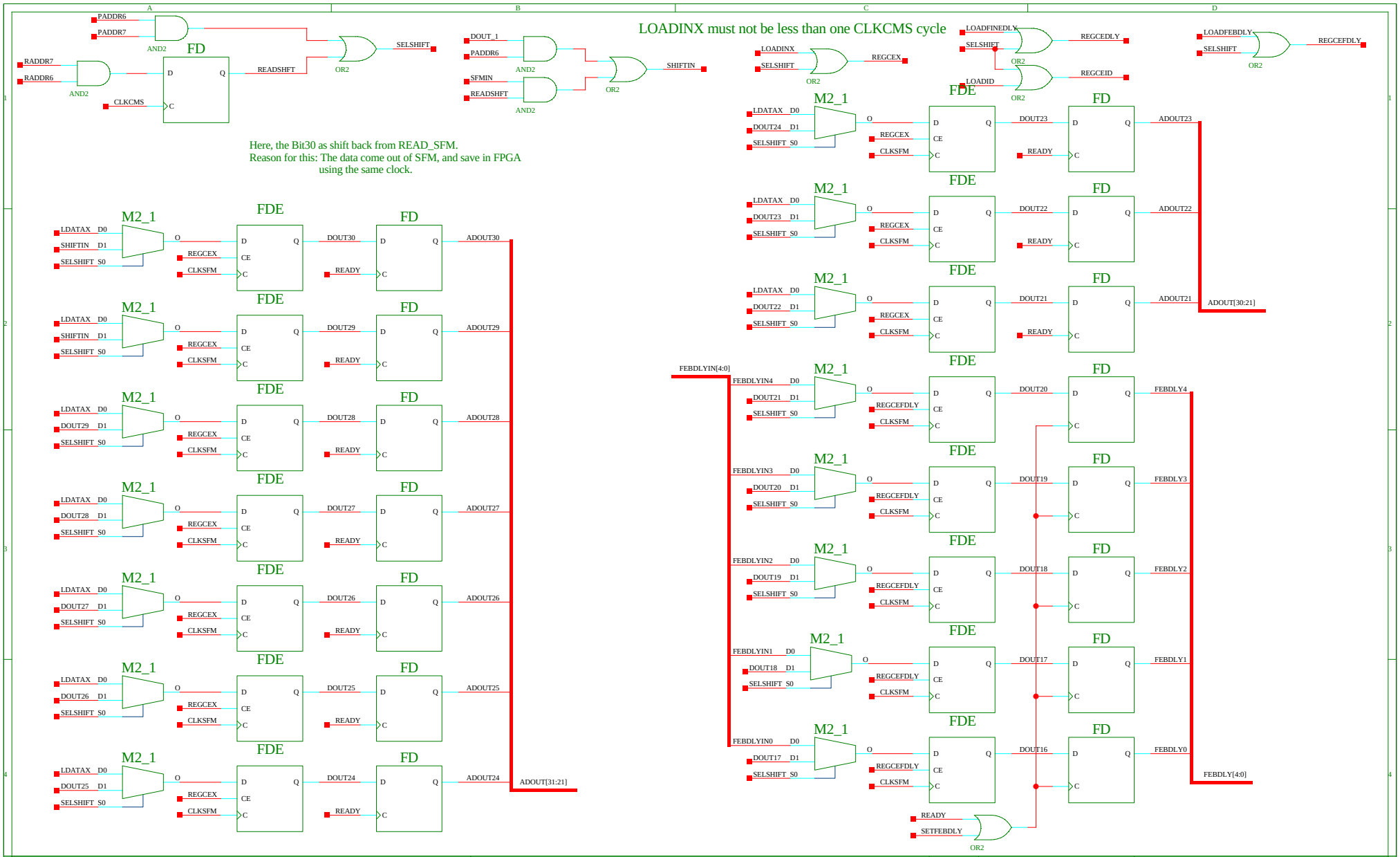
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Triple-voting for DAVs DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2B	PROJECT: DAQMBC
		DATE: 1-4-2002_10:52	FILE: GTRGFIFO. 4	PAGE: 30C



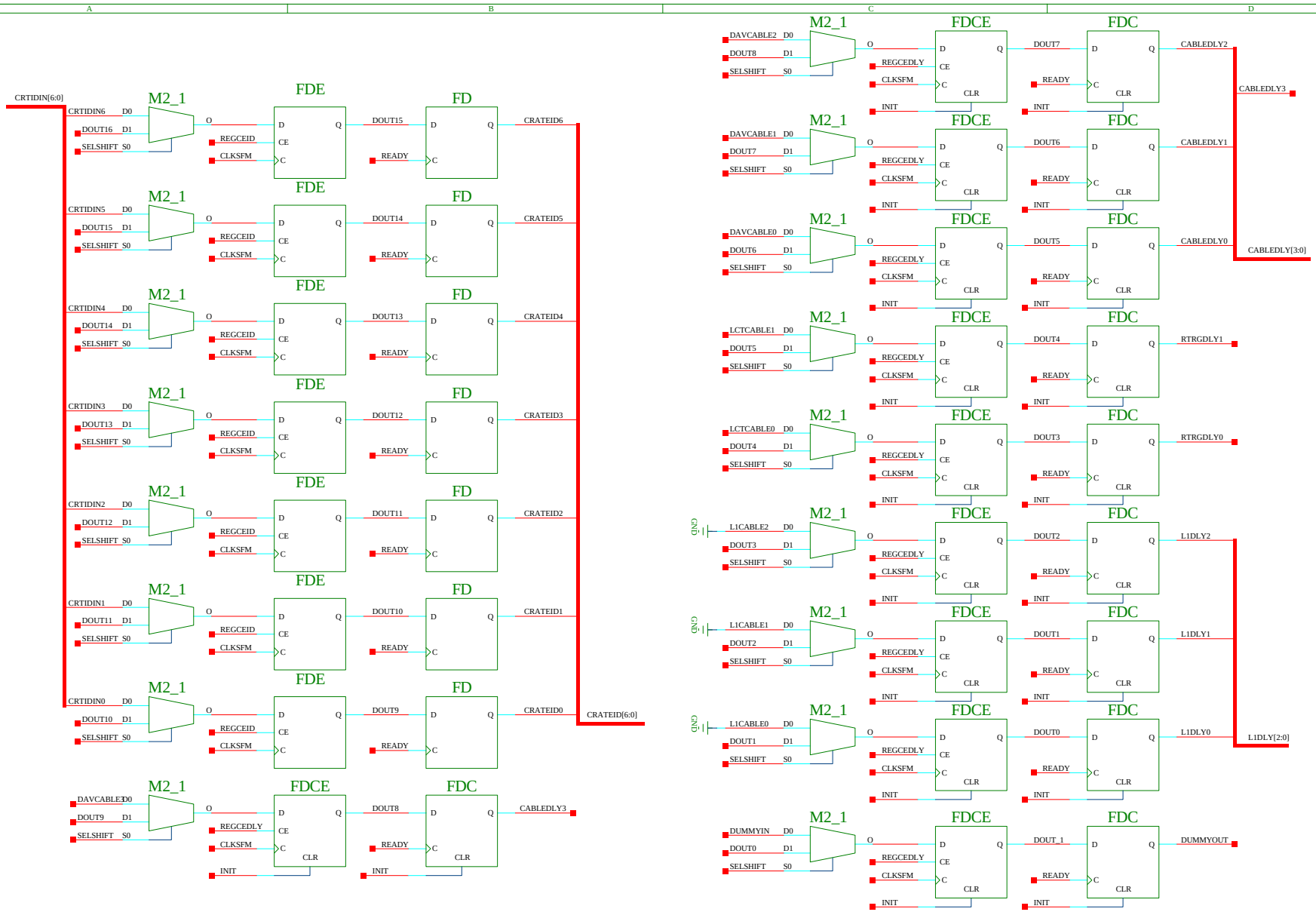
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: 8-bit Up-down Counter DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 30	PROJECT: DAQMBC
		DATE: 3-18-2002_13:33	FILE: CB8UPDN. 1	PAGE: 31



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Serial Flash Memory, Programming DAQ Motherboard Controller CMS CSC Electronics	BY GU	PARENT PAGE 2C	PROJECT DAQMBC
			DATE 1-3-2002_15:51	FILE SERFMEM . 1	PAGE 40



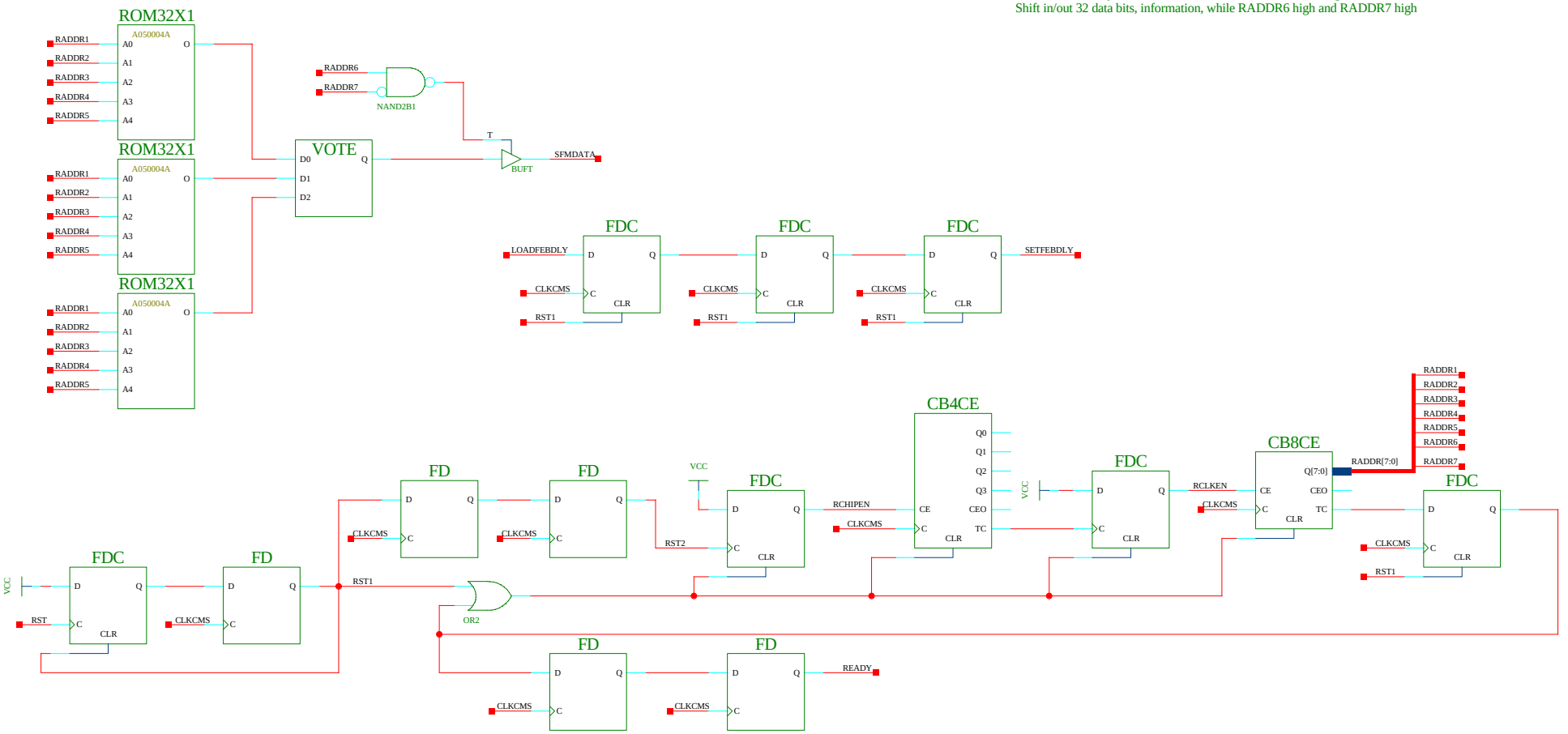
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Programming Data DAQ Motherboard Controller CMS CSC Electronics	BY: GU DATE: 8-2-2001_8:45	PARENT PAGE: 2C FILE: SERFMEM_2
		PROJECT: DAQMBC	PAGE: 40A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Serial Flash Memory, Programming DAQ Motherboard Controller CMS CSC Electronics	BY: GU DATE: 1-15-2002_12:34	PARENT PAGE: 2C FILE: SERFMEM . 3
		PROJECT: DAQMBC	PAGE: 40B

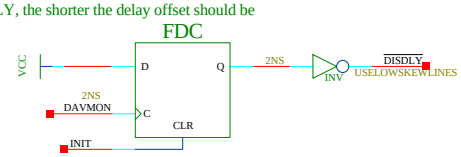
SFM Reading Header

Read Procedure: (needs about 7us)
Read Command: 52H, same page and byte address as PROGRAM
Reset, Delay 400ns, while RADDR6 low and RADDR7 low
Shift in 32 bits command and Address, while RADDR6 high and RADDR7 low
Shift in 32 Dummy bits, while RADDR6 low and RADDR7 high
Shift in/out 32 data bits, information, while RADDR6 high and RADDR7 high



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Serial Flash Memory, Reading DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2C	PROJECT: DAQMBC
		DATE: 8-2-2001_8:45	FILE: SERFMEM . 4	PAGE: 40C

The longer the cable, the longer the period between L1ACC and DISDLY, the shorter the delay offset should be

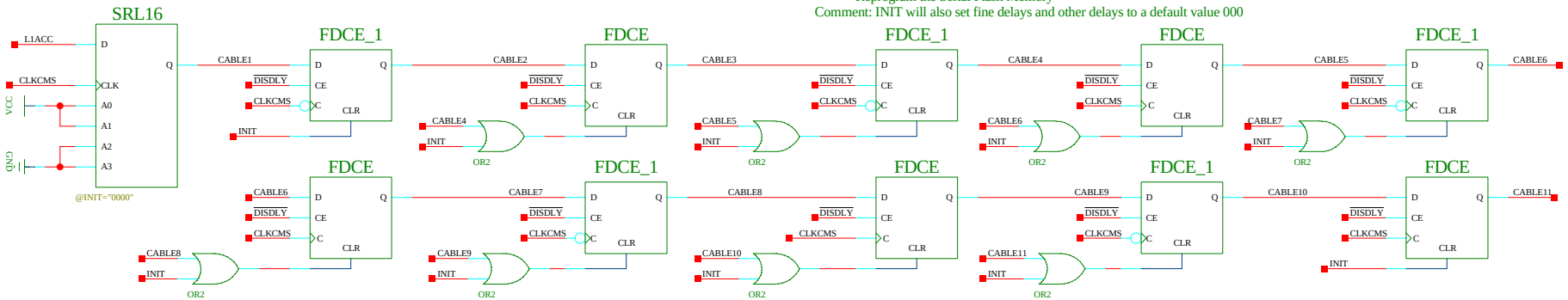


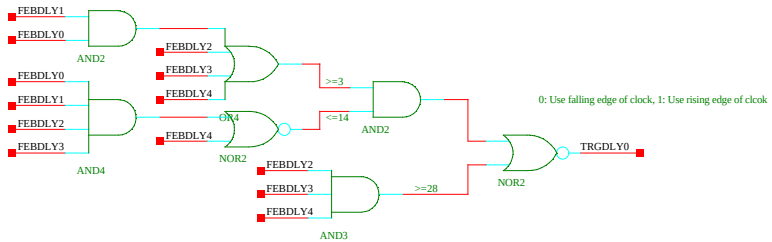
Adjust this according to CFEB FPGA delay and maximum cable length delay to 111 on BIT[2:0]

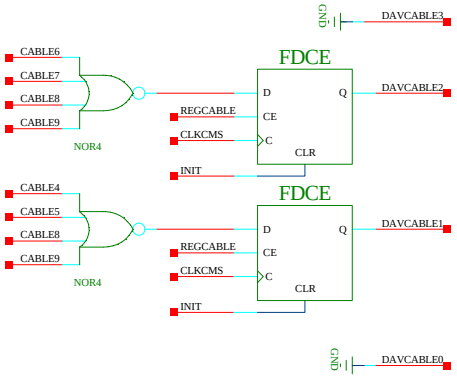
Cable Delay detection procedure:

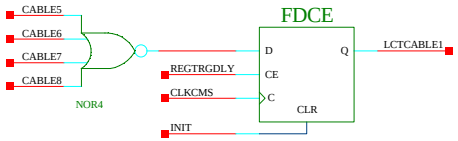
Send INIT (SERFM5), to initialize FFs, and fine delay
Load CFEB Clock Delay (SERFM2) at the nominal setting
Update the CFEB clock delay setting (SERFM8) on the external register
Trigger, send matched L1ACC and LCT to CFEB3, either pulse or inject
Latch the Trigger (LCT/L1ACC) fine delay, REGTRGDLY (SERFM6)
Update the fine delay (SERFM0) inside the FPGA
Trigger, same as previous step
Latch the Cable length-related fine delay, REGCABLE (SERFM7)
Update the fine delay (SERFM0) inside the FPGA
Reprogram the Serial Flash Memory

Comment: INIT will also set fine delays and other delays to a default value 000





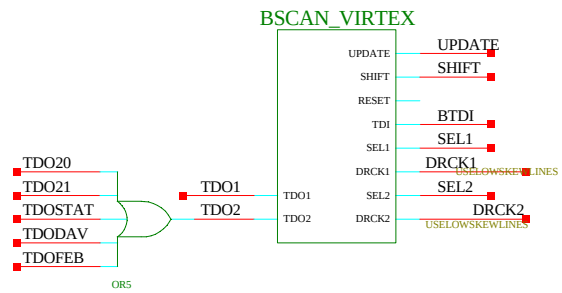


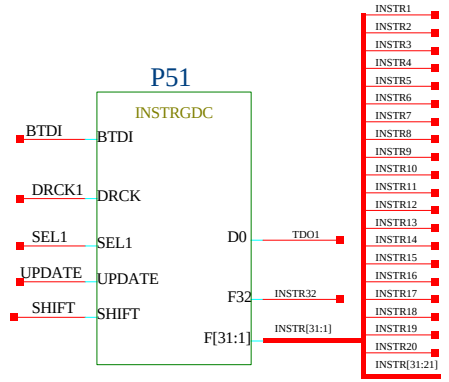


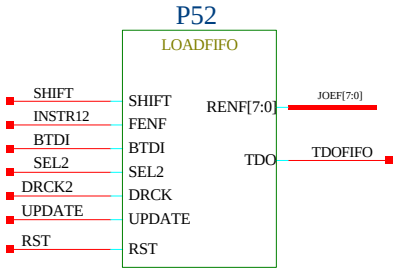
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Cable Length Detection DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2C	PROJECT: DAQMBC
		DATE: 1-15-2002_12:34	FILE: SERFMEM . 5	PAGE: 40D

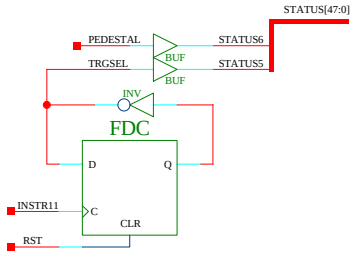
Instruction Code: (8 bits, on SEL1)

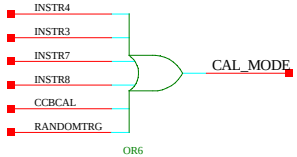
00: NO-OPERATION (Page 50)
01: JTAG Reset (page 50)
02: Global Reset (page 50)
03: BUCKEYE Inject (page 58)
04: BUCKEYE Pulse (page 58)
05: Pedestal data taking (page 58)
06: Load Trigger Register (page 57)
07: Cycle Trigger Register Once (page 57)
08: Continuously Cycle Trigger Register (page 57)
09: Load CFEB Register (page 59)
0A: DAQMB Status (page 55)
0B: Trigger select in cal_mode (page 50)
0C: FIFO mannual read control (page 52)
0D: DAV Delay Setting (page 56)
0E: FIFO Master Reset and GLINK Reset (page 50)
0F: Load DAQMB Crate ID (page 53)
10: Load CFEB Clock Delay (page 53)
11: Set Calibration timing (Calib Pulse Delay) (page 54)
12: Set Loop Back for Glink, toggling (page 70)
13: Load Random Trigger Frequency
14: Toggle Random trigger start control
15: Serial Flash Memory (page 40s)
⋮ ⋮
1F: Serial Flash Memory (page 40s)
20: Burst 1000 (really 512+256+128) Random events (L1ACC)

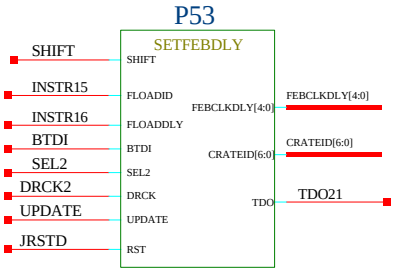


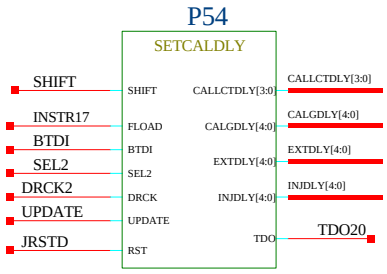


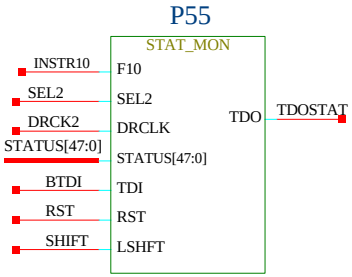


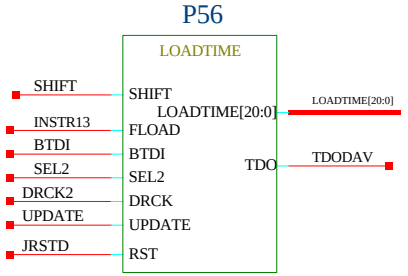








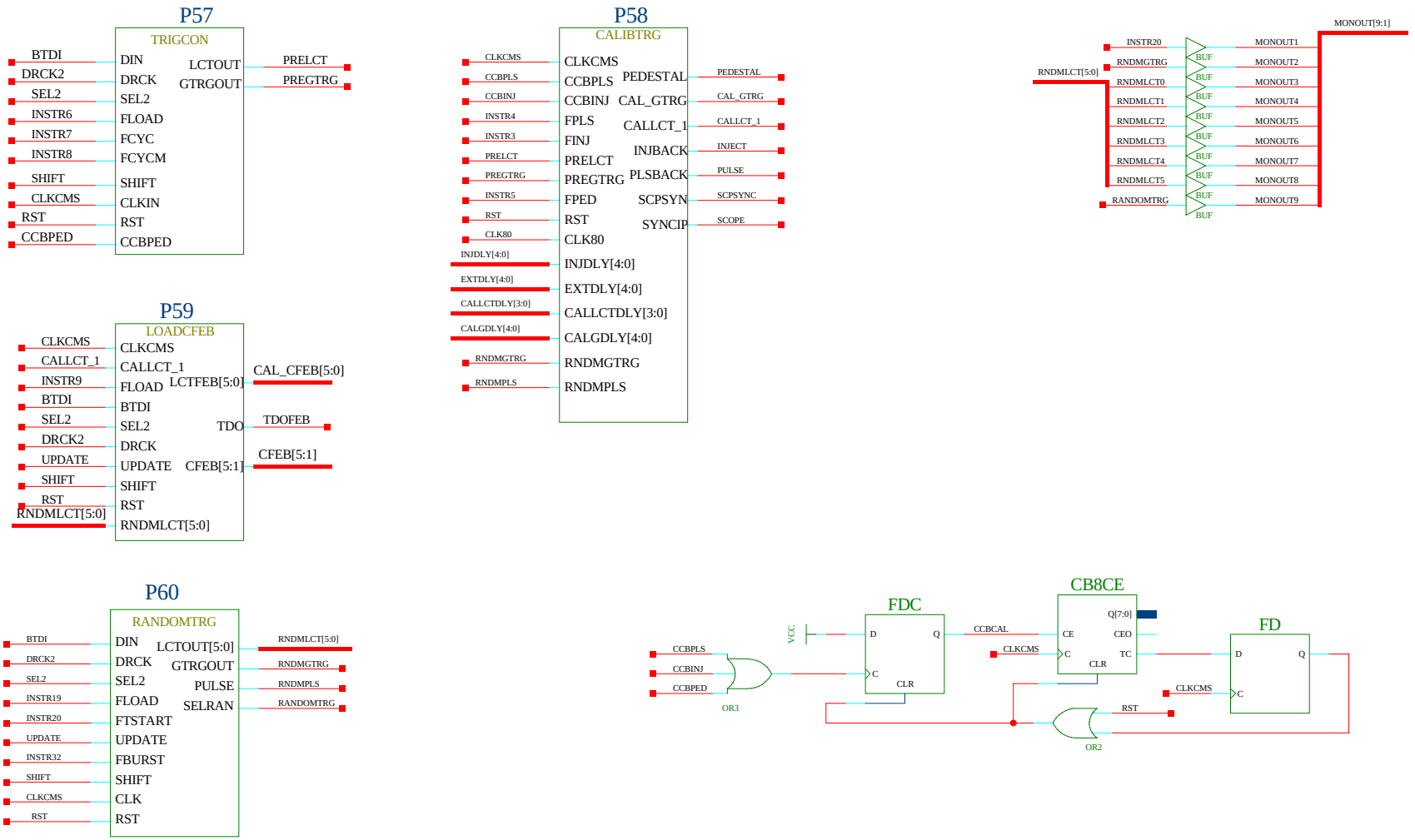




THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: JTAG Command Block
DAQ Motherboard Controller
CMS CSC Electronics

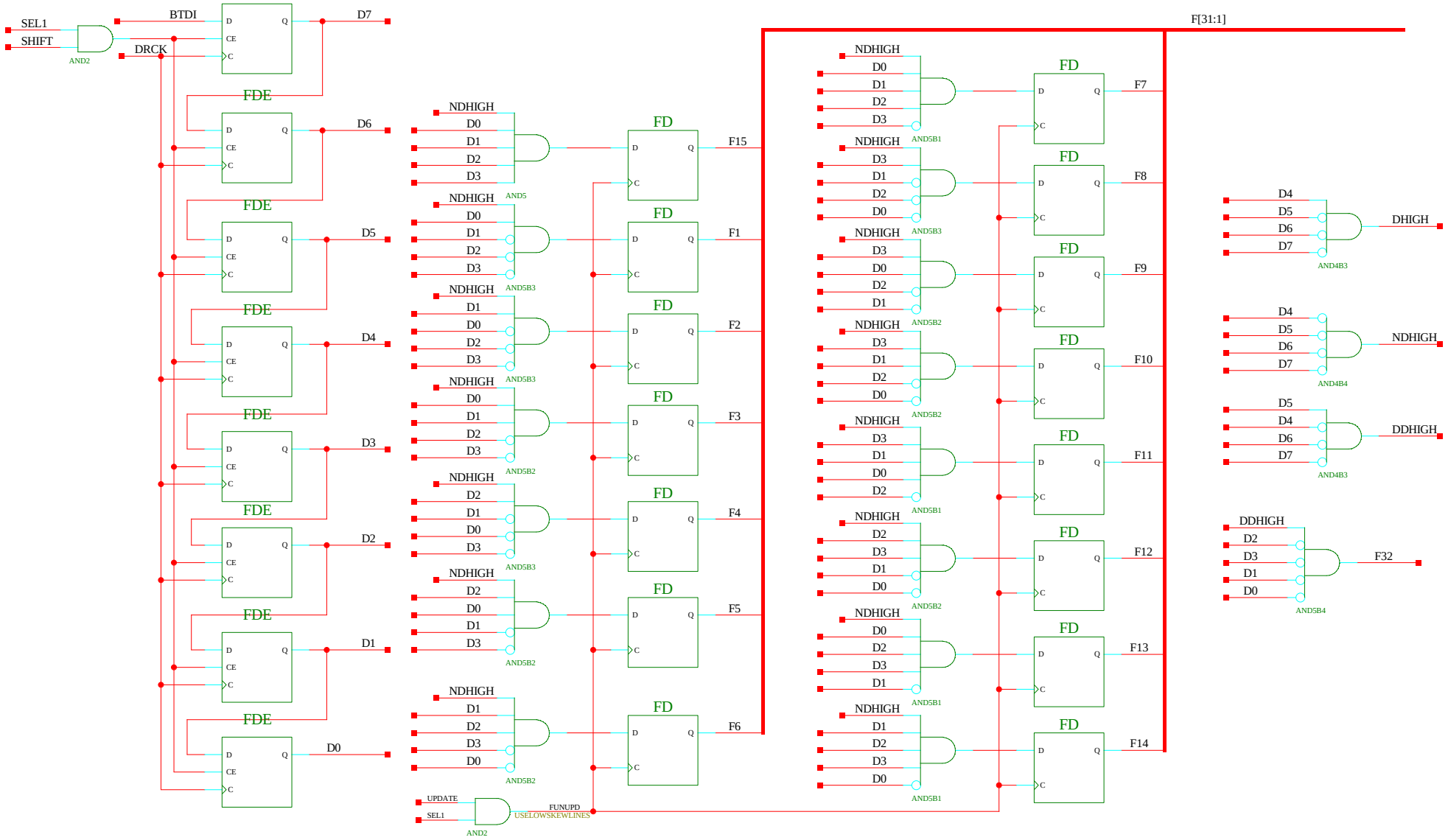
BY: GU | PARENT PAGE: 2D | PROJECT: DAQMBC
DATE: 1-14-2002_16:34 | FILE: JTAGCOM . 1 | PAGE: 50



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Command Block DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2D	PROJECT: DAQMBC
		DATE: 1-14-2002_16:34	FILE: JTAGCOM . 2	PAGE: 50A

Combination first, Register later to eliminate possible Instruction Glitches decode first 15 OpCodes (4.5 bits)

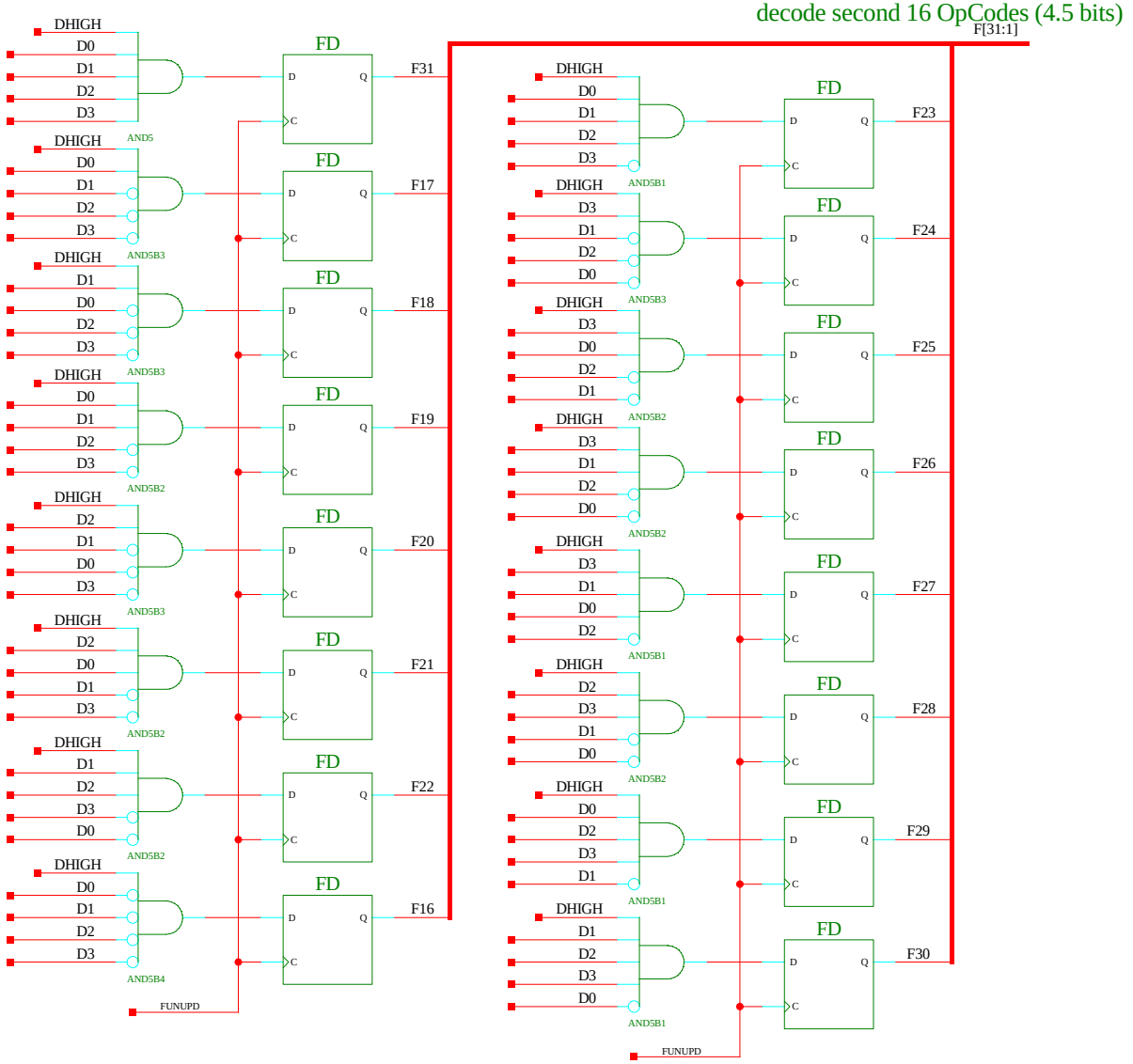
FDE 8 Bit Instruction Register



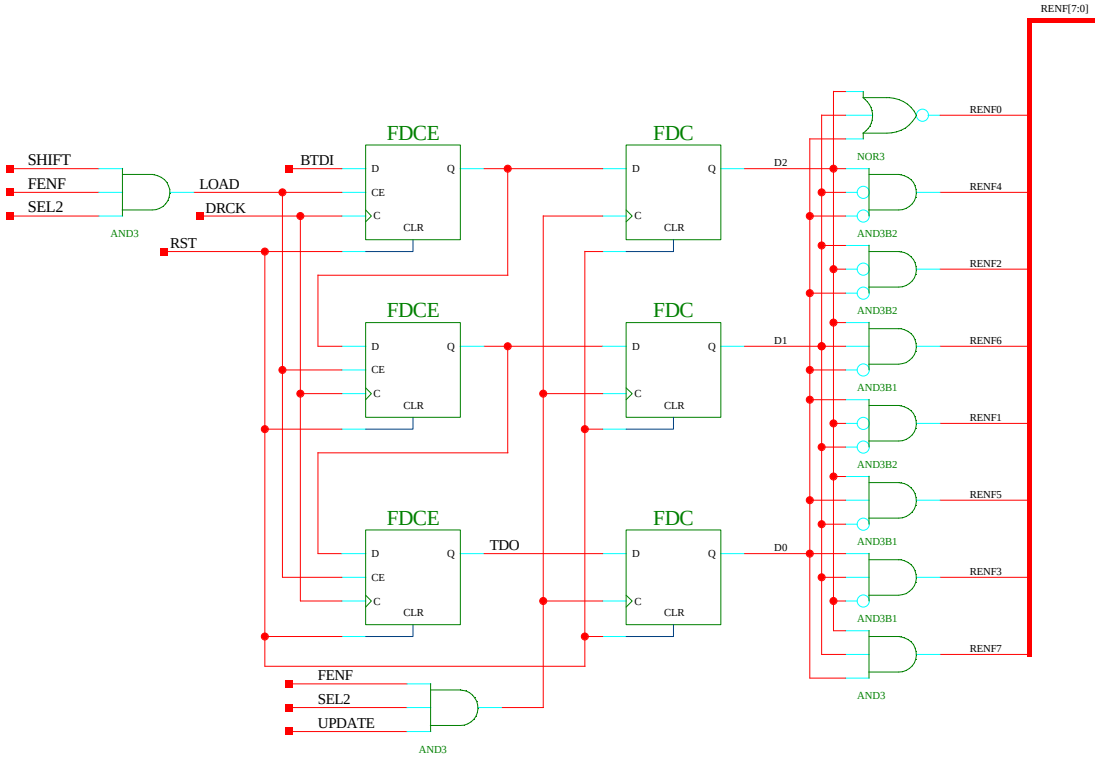
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE JTAG Instruction Decode DAQ Motherboard Controller CMS CSC ELECTRONICS	BY GU	PARENT PAGE 50	PROJECT DAQMBC
		DATE 1-14-2002_16:36	FILE INSTRGDC . 1	PAGE 51

Do combination first, register later to eliminate possible instruction glitches

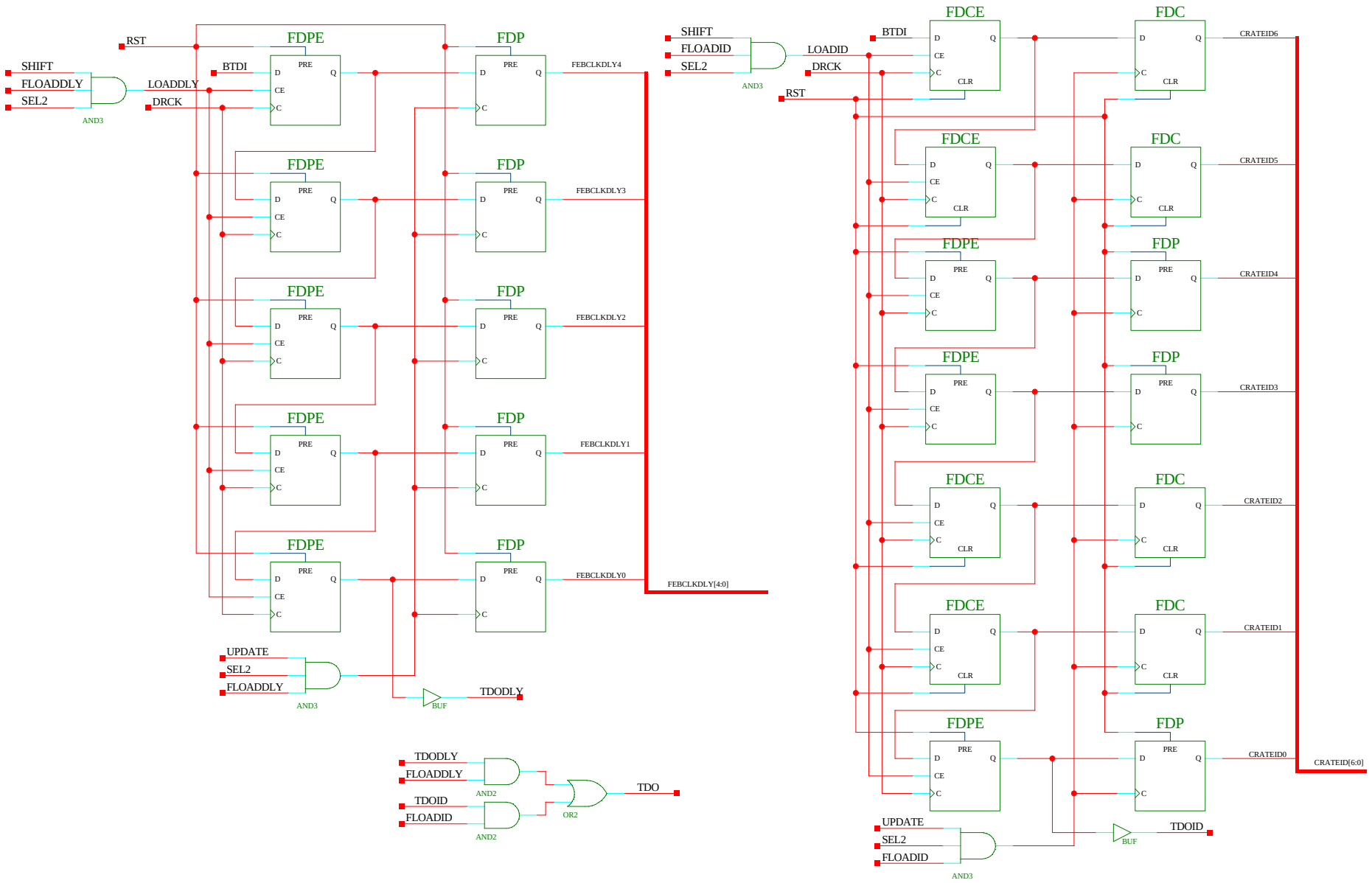
decode second 16 OpCodes (4.5 bits)



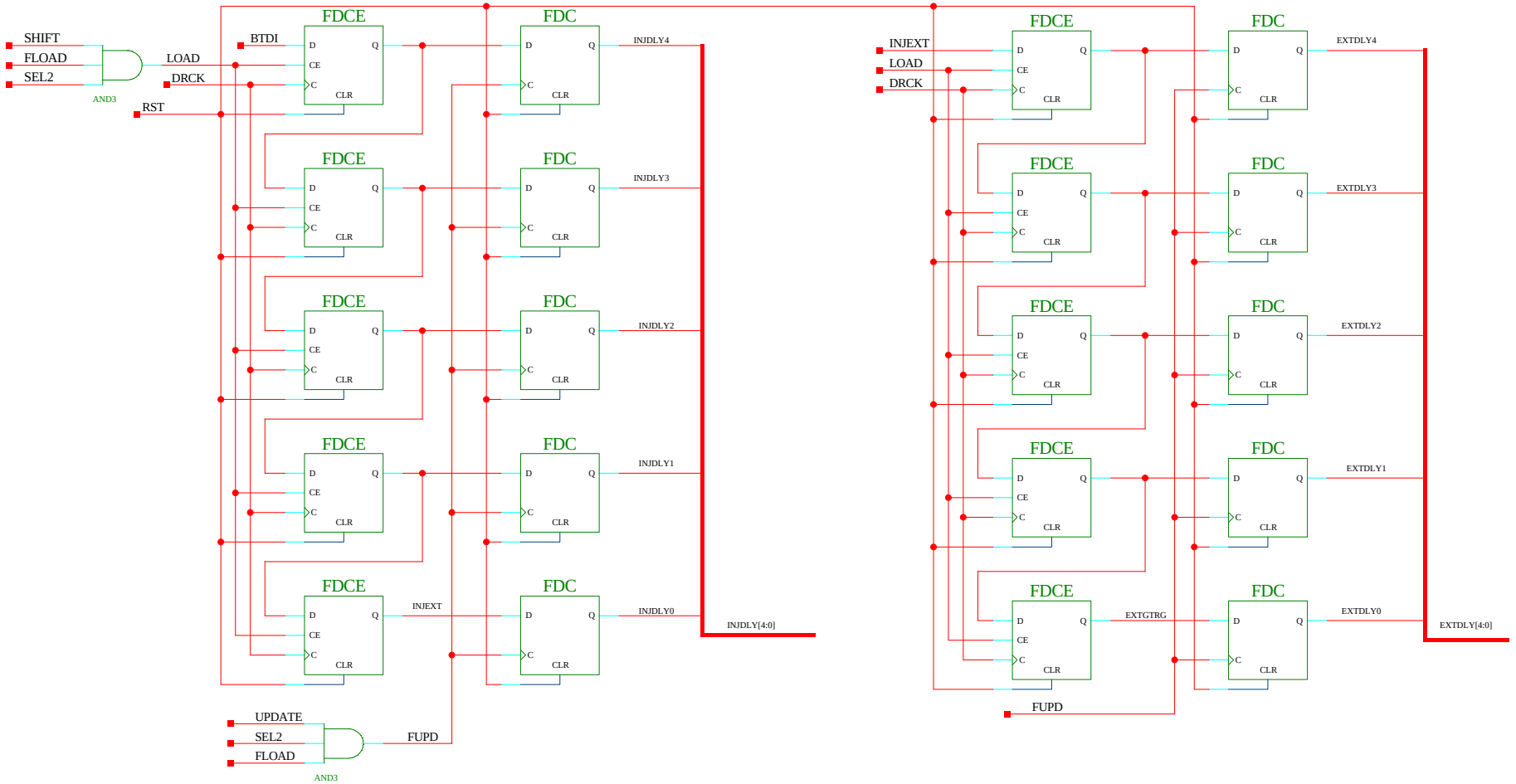
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Instruction Decode DAQ Motherboard Controller CMS CSC ELECTRONICS	BY: GU DATE: 8-2-2001_10:22	PARENT PAGE: 50	PROJECT: DAQMBC FILE: INSTRGDC . 2 PAGE: 51A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Mannual Read FIFO Select DAQ Motherboard controller CMS CSC Electronics	BY GU	PARENT PAGE 50	PROJECT DAQMBC
			DATE 8-29-2001_11:27	FILE LOADFIFO . 1	PAGE 52



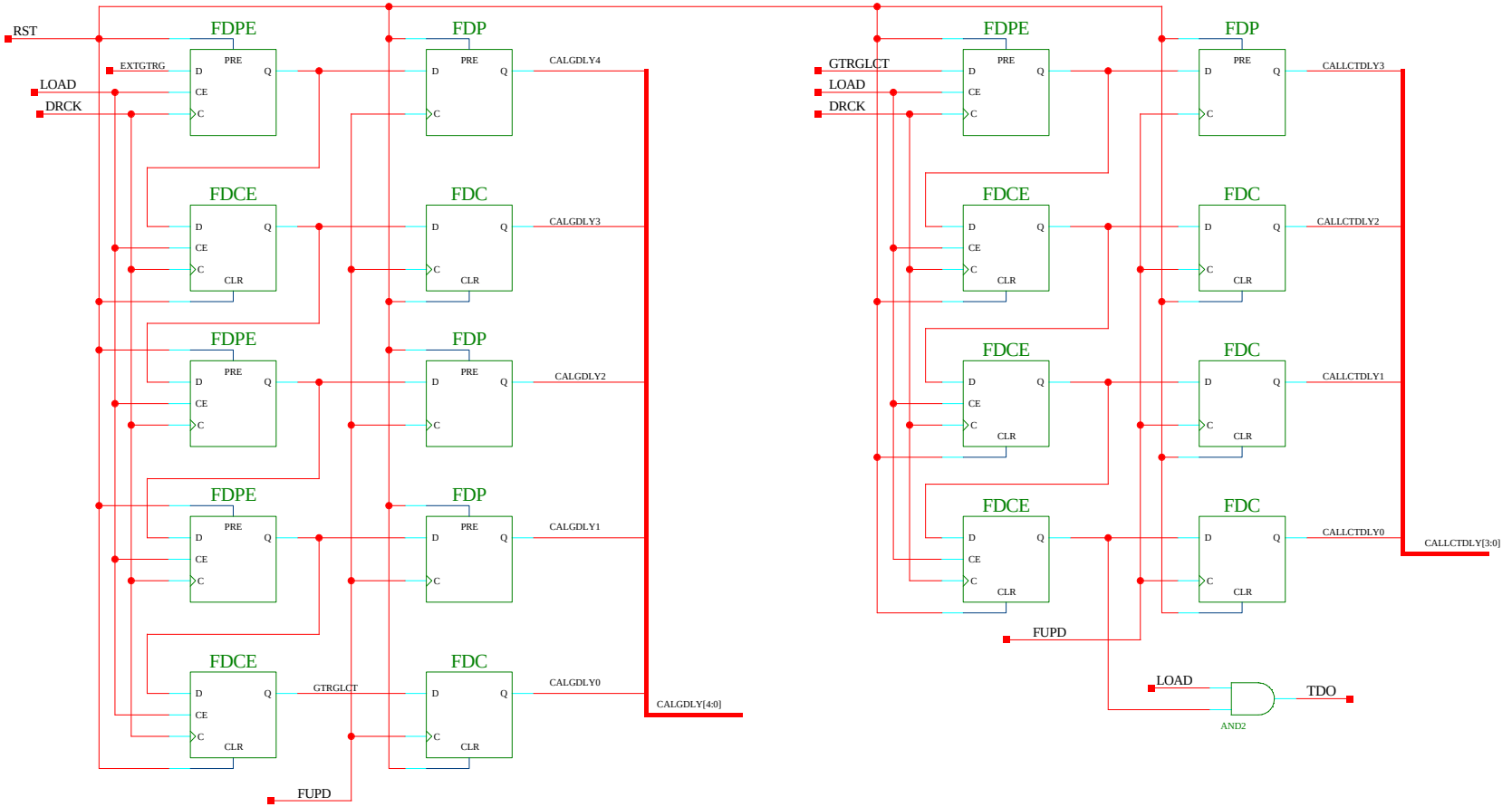
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CFEB Clock Delay DAQ Motherboard controller CMS CSC Electronics	BY: GU PARENT PAGE: 50 DATE: 8-2-2001_10:26	PROJECT: DAQMBC FILE: SETFEBDLY . 1 PAGE: 53



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

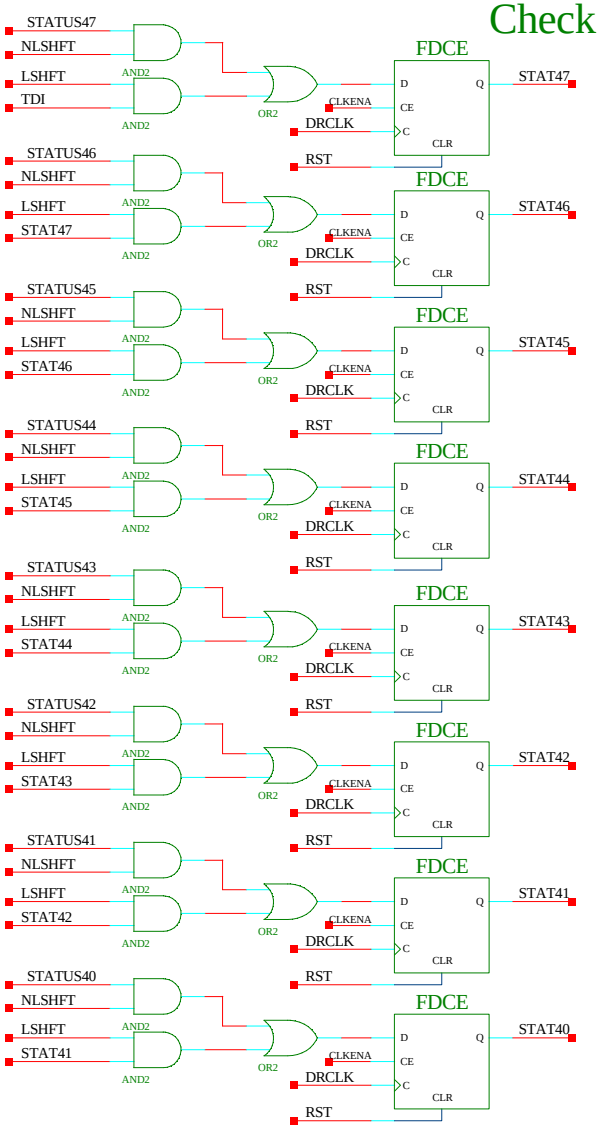
TITLE: Load INJECT, EXTPULSE delay
DAQ Motherboard controller
CMS CSC Electronics

BY: GU
PARENT PAGE: 50
PROJECT: DAQMBC
DATE: 8-2-2001_10:30
FILE: SETCALDLY . 1
PAGE: 54



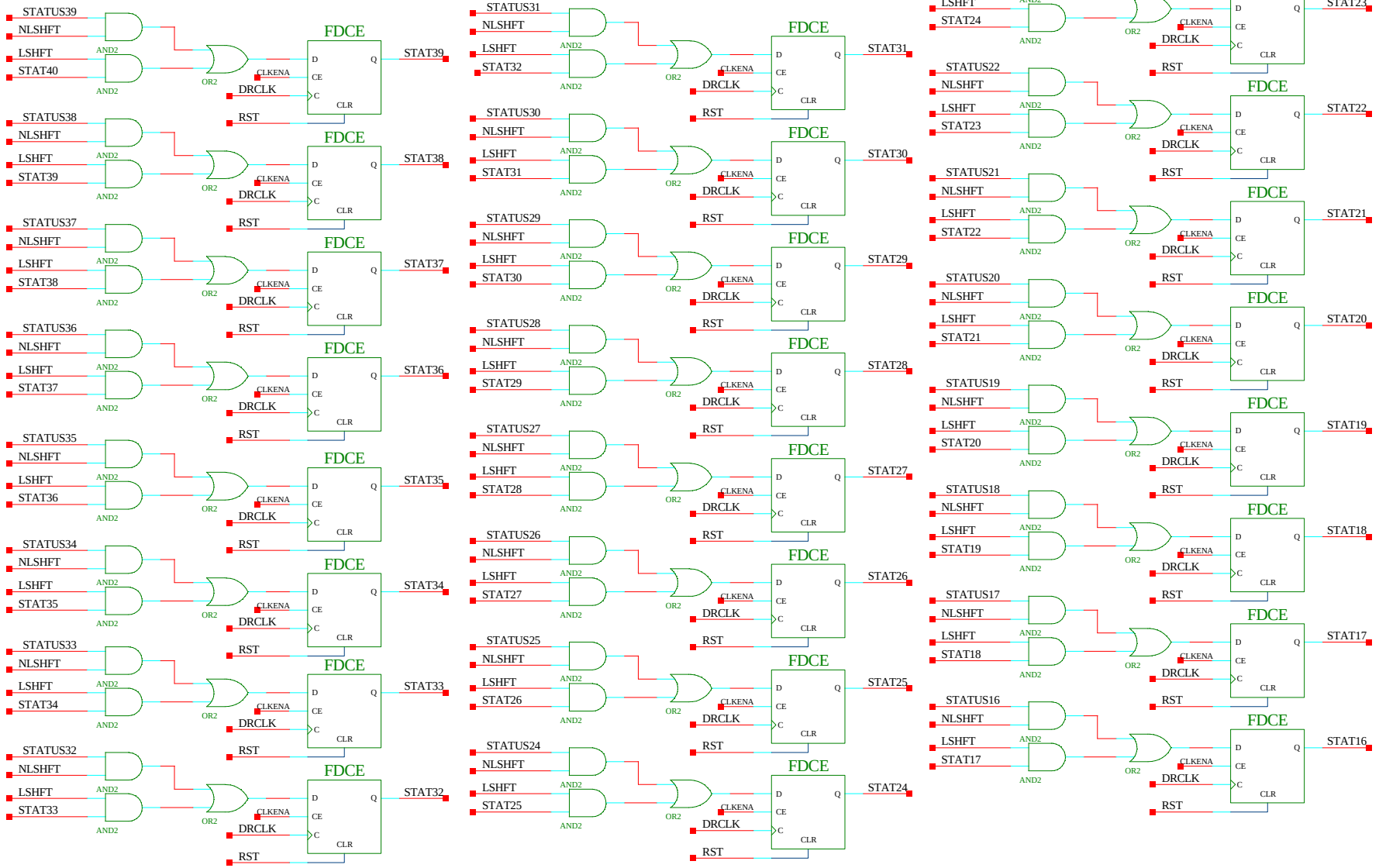
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Load CAL LCT, GTRG delay relative to PULSE DAQ Motherboard controller CMS CSC Electronics	BY: GU DATE: 8-2-2001_11:27	PARENT PAGE: 50	PROJECT: DAQMBC FILE: SETCALDLY . 2 PAGE: 54A

Check Status LOGIC (F10)



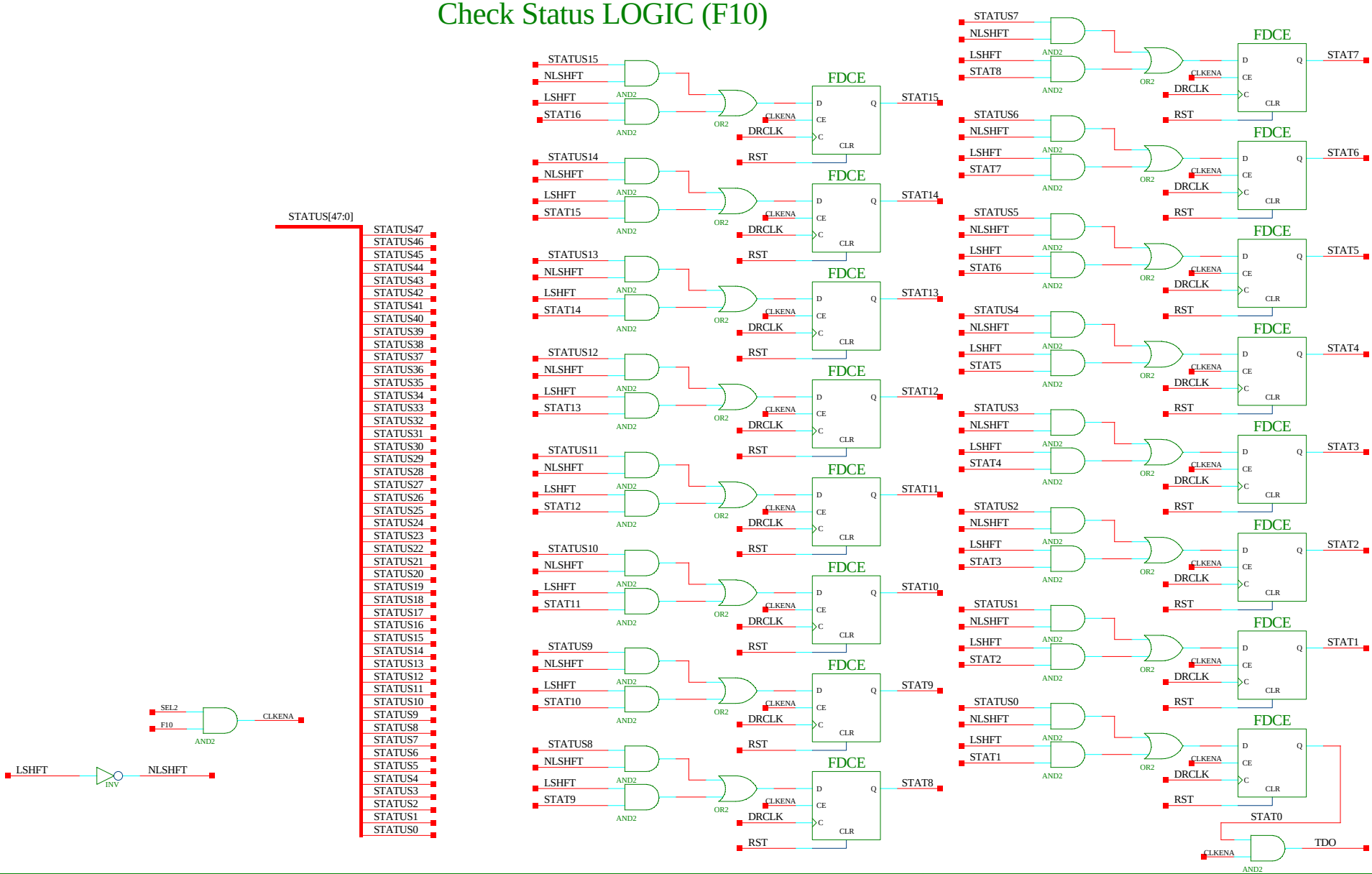
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Status Monitor DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50	PROJECT: DAQMBC
		DATE: 3-18-2002_13:34	FILE: STAT_MON . 1	PAGE: 55

Check Status LOGIC (F10)

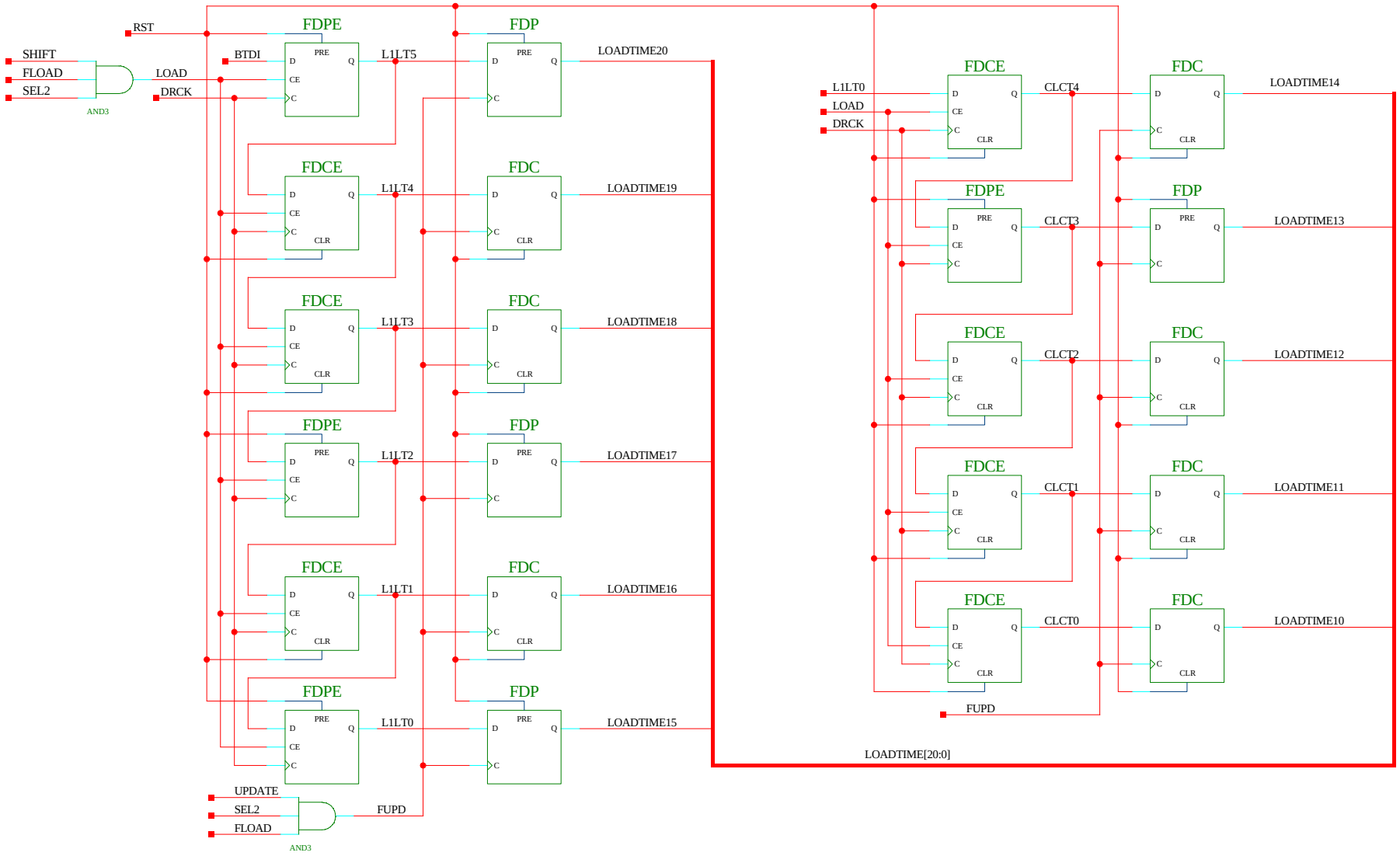


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Status Monitor DAQ Motherboard Controller CMS CSC Electronics	BY: GU DATE: 3-18-2002_13:34	PARENT PAGE: 50 FILE: STAT_MON . 2
		PROJECT: DAQMBC	PAGE: 55A

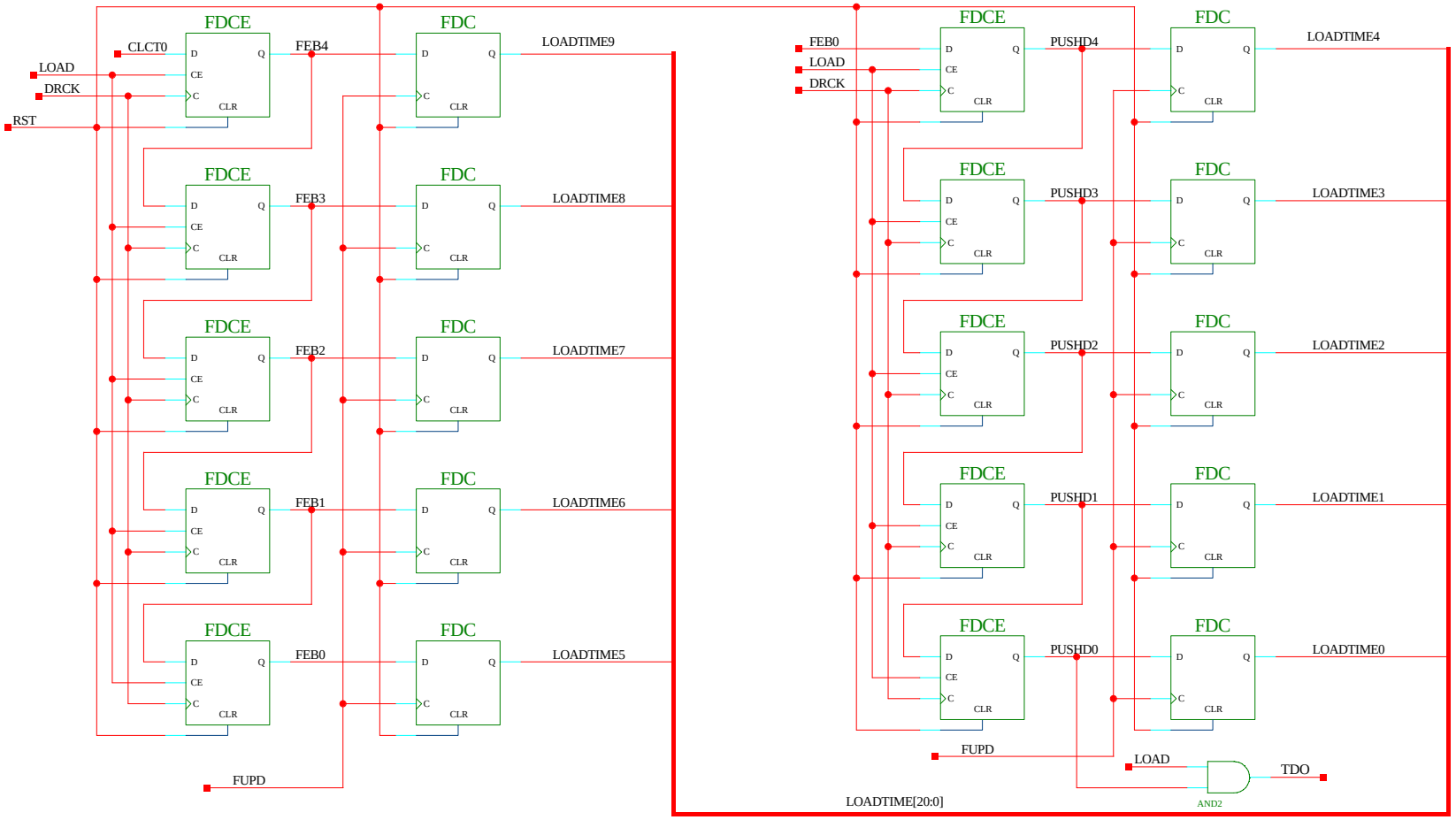
Check Status LOGIC (F10)



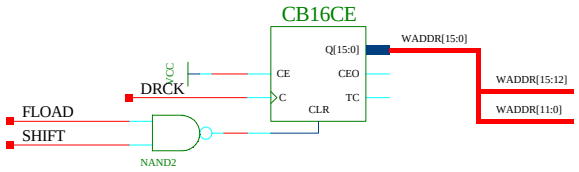
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Status Monitor DAQ Motherboard Controller CMS CSC Electronics	BY GU	PARENT PAGE 50	PROJECT DAQMBC
			DATE 3-18-2002_13:34	FILE STAT_MON_3	PAGE 55B

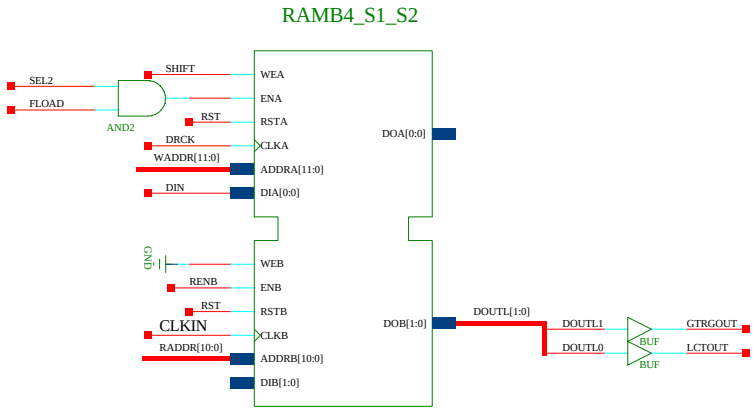


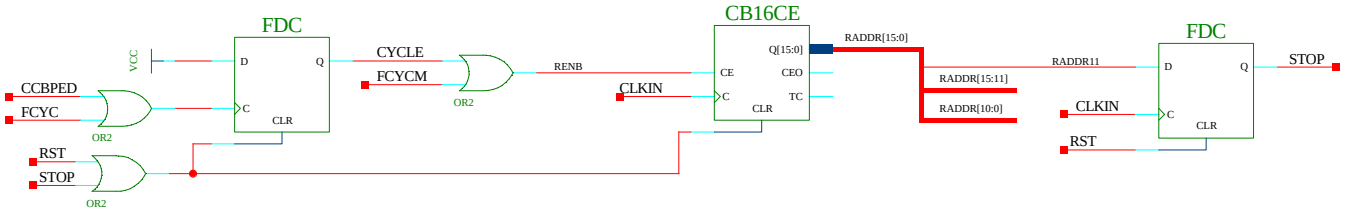
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Load L1latency, TMB DAV, CFEB DAV, GPUSH Delay DAQ Motherboard controller CMS CSC Electronics	BY GU	PARENT PAGE 50	PROJECT DAQMBC
			DATE 8-2-2001_11:42	FILE LOADTIME . 1	PAGE 56



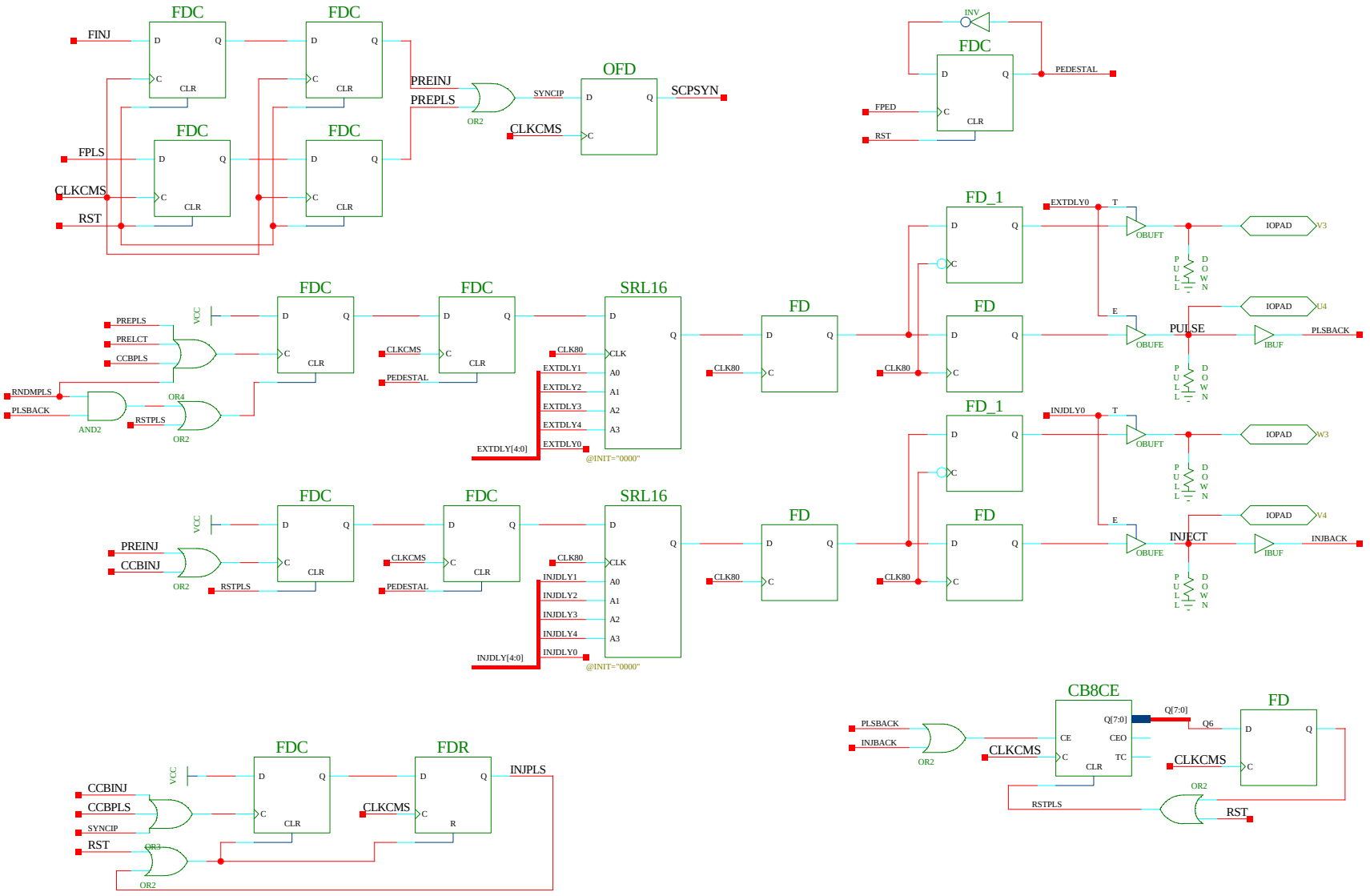
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Load L1latency, TMB DAV, CFEB DAV, GPUSH Delay DAQ Motherboard controller CMS CSC Electronics	BY GU	PARENT PAGE 50	PROJECT DAQMBC
			DATE 8-2-2001_11:45	FILE LOADTIME . 2	PAGE 56A



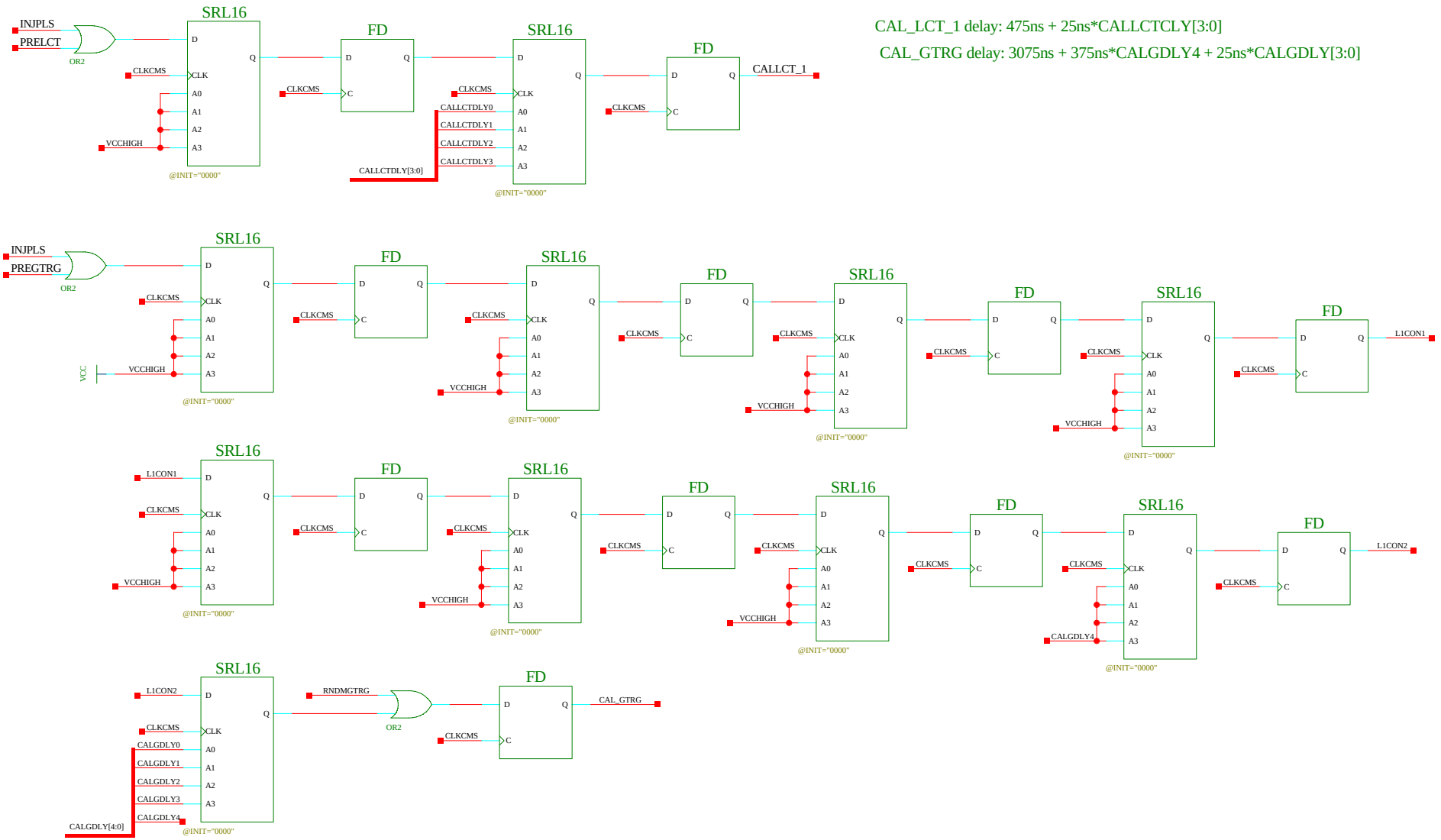




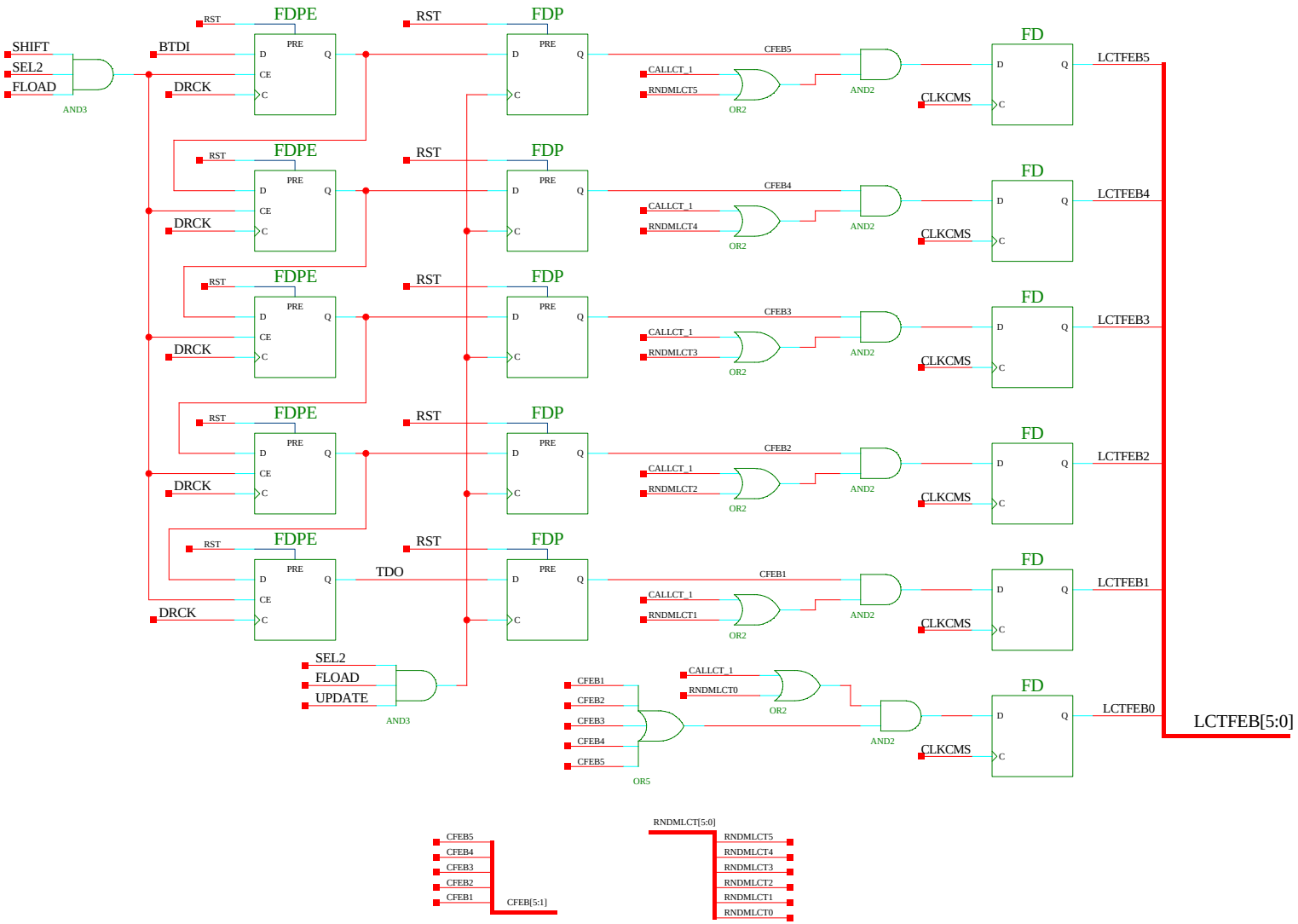
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Trigger Generator DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A	PROJECT: DAQMBC
		DATE: 12-4-2001_15:25	FILE: TRIGCON. 1	PAGE: 57



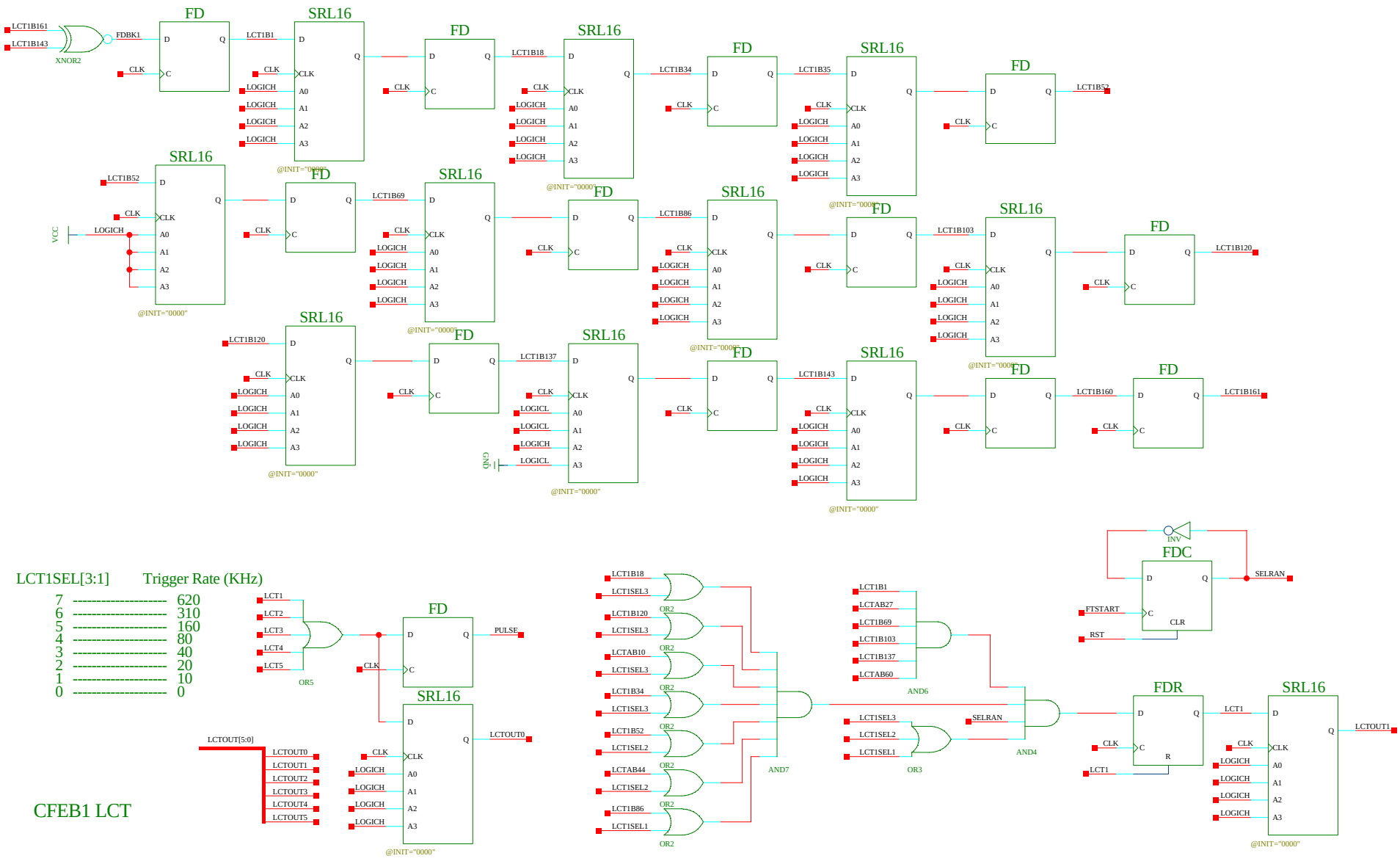
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Calibration Trigger, Pulse delay DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A	PROJECT: DAQMBC
		DATE: 12-4-2001_16:40	FILE: CALIBTRG . 1	PAGE: 58



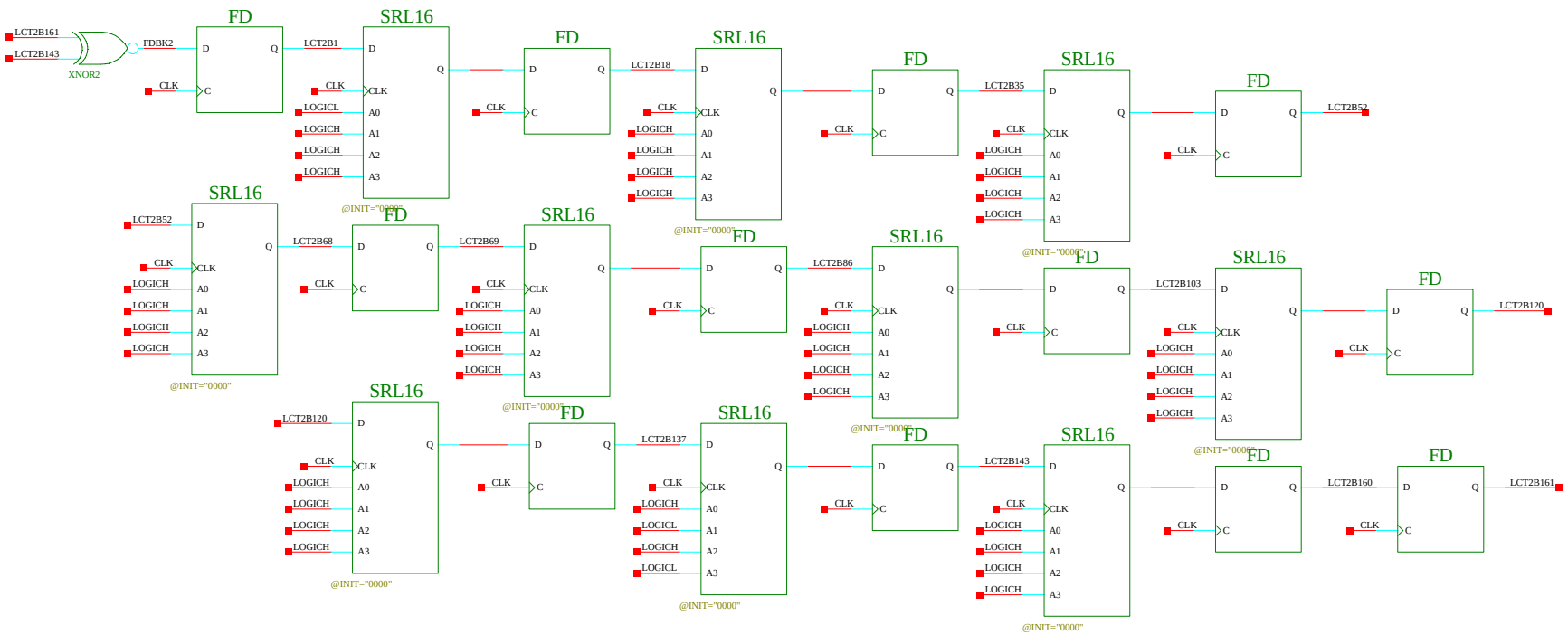
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Calibration Trigger, Delay Adjustment DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A	PROJECT: DAQMBC
		DATE: 12-4-2001_15:40	FILE: CALIBTRG . 2	PAGE: 58A



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CFEB Selection DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A	PROJECT: DAQMBC
		DATE: 12-4-2001_15:37	FILE: LOADCFEB . 1	PAGE: 59

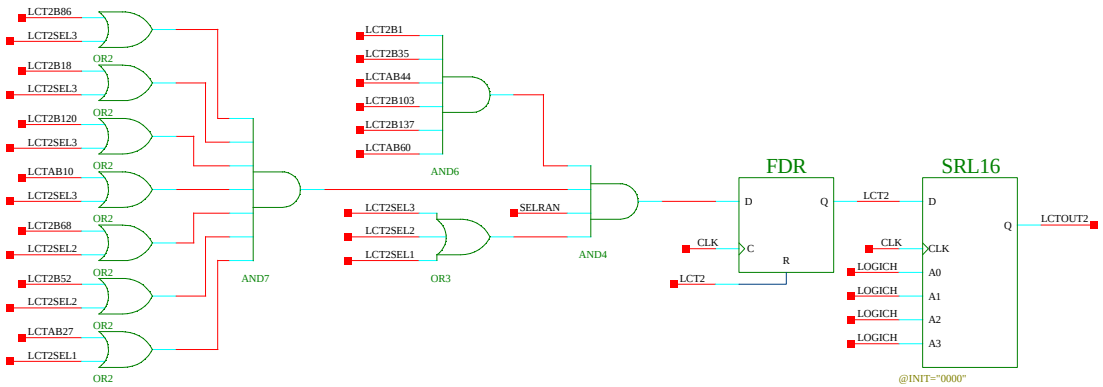


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Random LCT for CFEB1 DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A	PROJECT: DAQMBC
		DATE: 1-14-2002_14:46	FILE: RANDOMTRG. 1	PAGE: 60



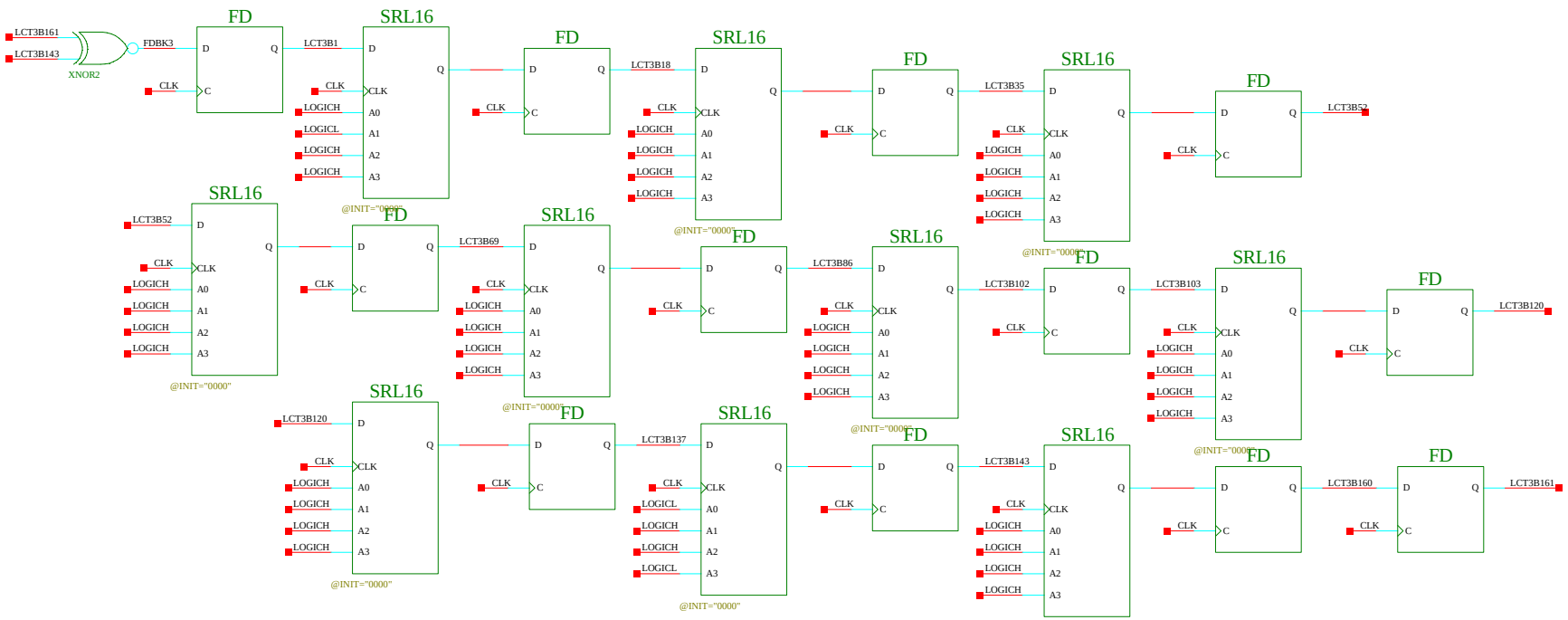
LCT2SEL[3:1] Trigger Rate (KHz)

7	----------	620
6	----------	310
5	----------	160
4	----------	80
3	----------	40
2	----------	20
1	----------	10
0	----------	0



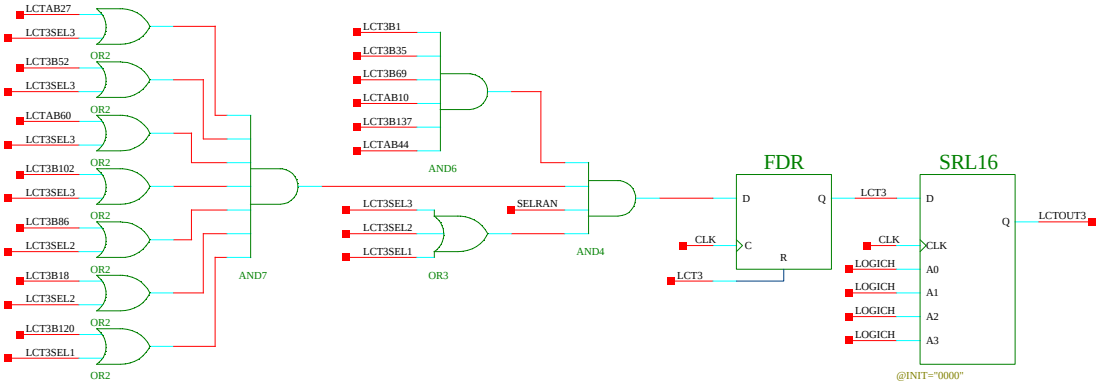
CFEB1 LCT

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Random LCT for CFEB2 DAQ Motherboard Controller CMS CSC Electronics	BY GU / PARENT PAGE 50A DATE 1-14-2002_14:46	PROJECT DAQMBC FILE RANDOMTRG. 2 / PAGE 60A



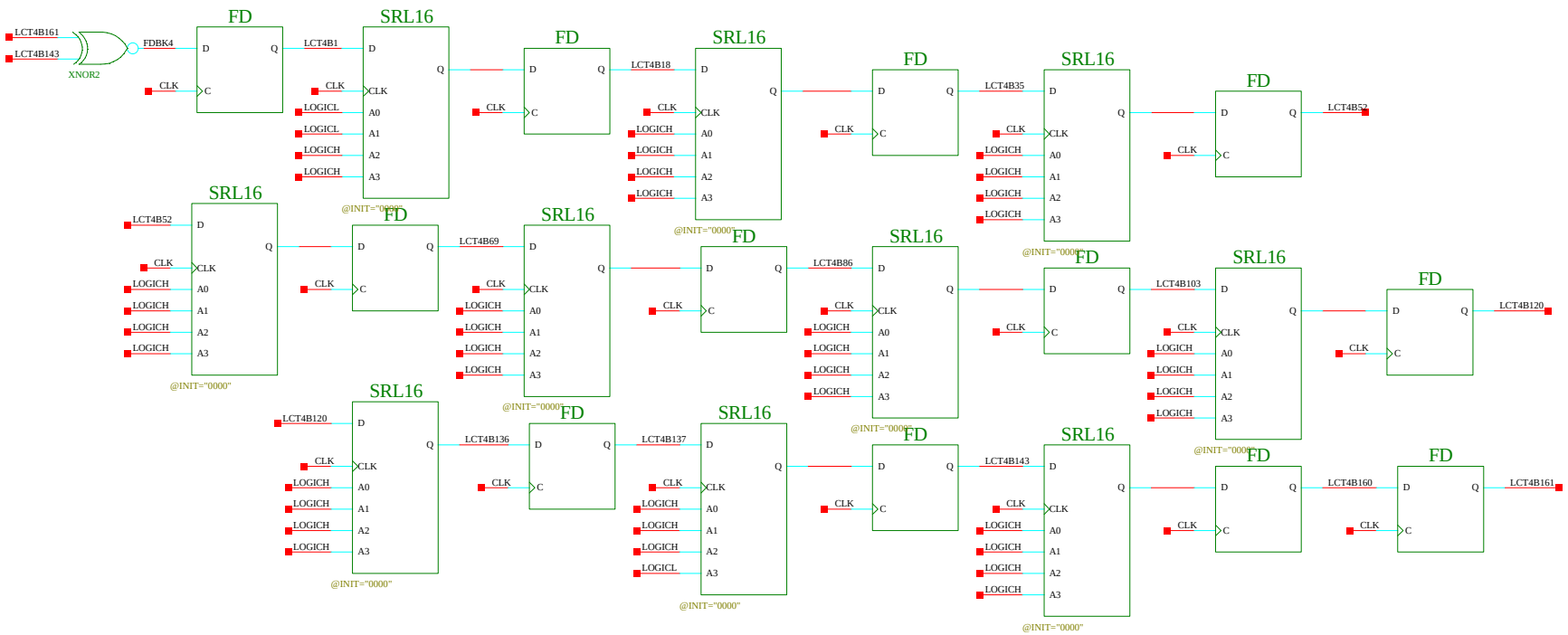
LCT3SEL[3:1] Trigger Rate (KHz)

7	----------	620
6	----------	310
5	----------	160
4	----------	80
3	----------	40
2	----------	20
1	----------	10
0	----------	0



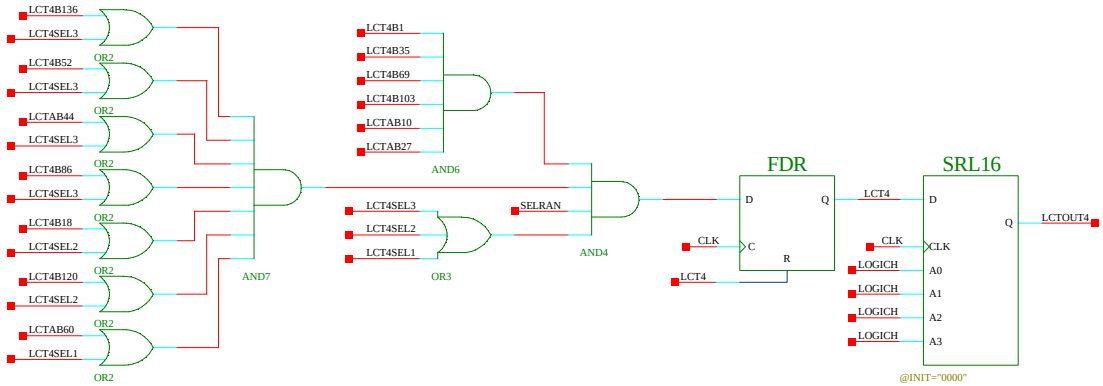
CFEB1 LCT

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE	Random LCT for CFEB3 DAQ Motherboard Controller CMS CSC Electronics	BY GU DATE 1-14-2002_14:46	PARENT PAGE 50A FILE RANDOMTRG. 3	PROJECT DAQMBC PAGE 60B



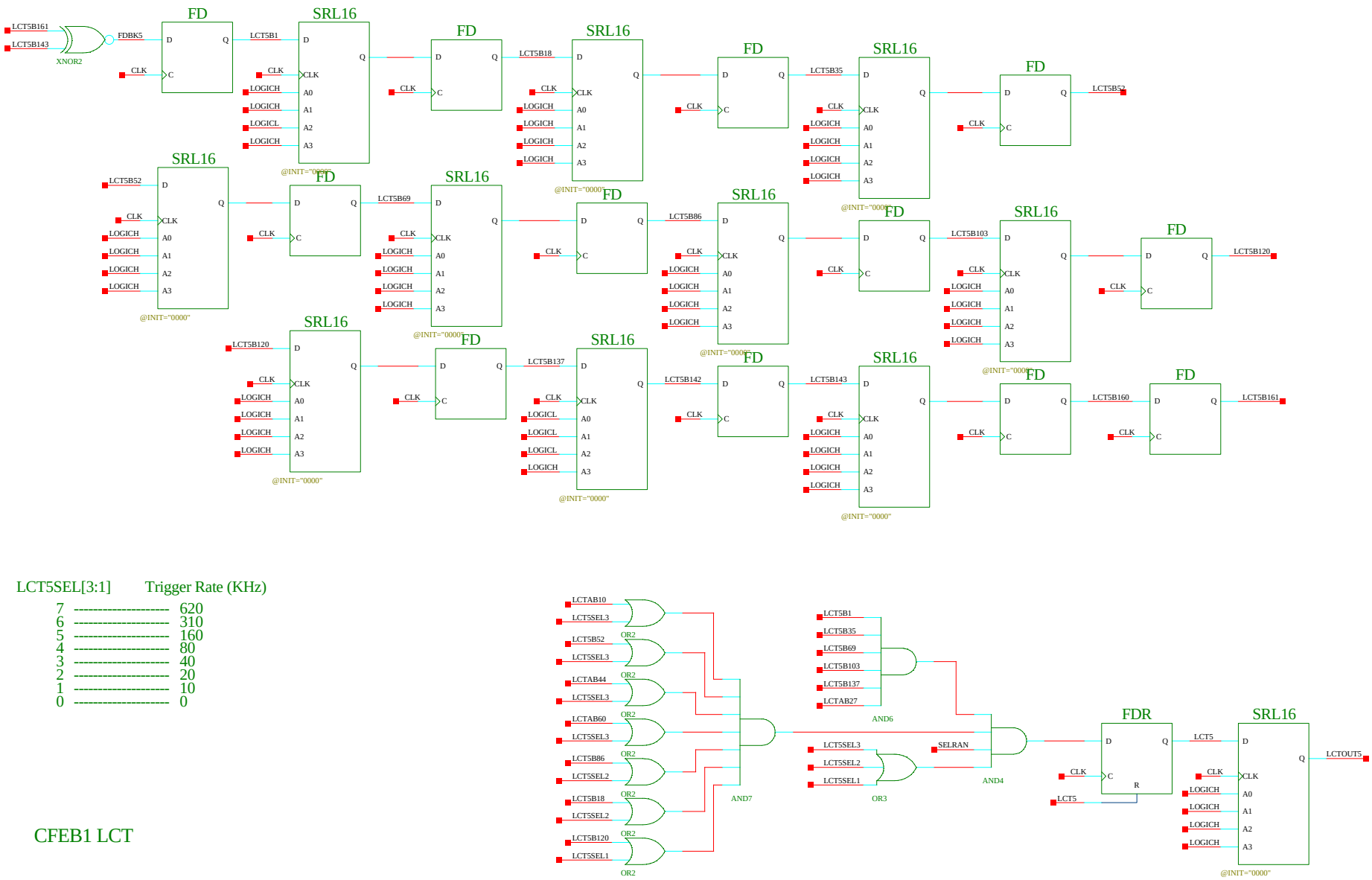
LCT4SEL[3:1] Trigger Rate (KHz)

7	----------	620
6	----------	310
5	----------	160
4	----------	80
3	----------	40
2	----------	20
1	----------	10
0	----------	0



CFEB1 LCT

THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Random LCT for CFEB4 DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A
		DATE: 1-14-2002_14:46	PROJECT: DAQMBC
		FILE: RANDOMTRG. 4	PAGE: 60C

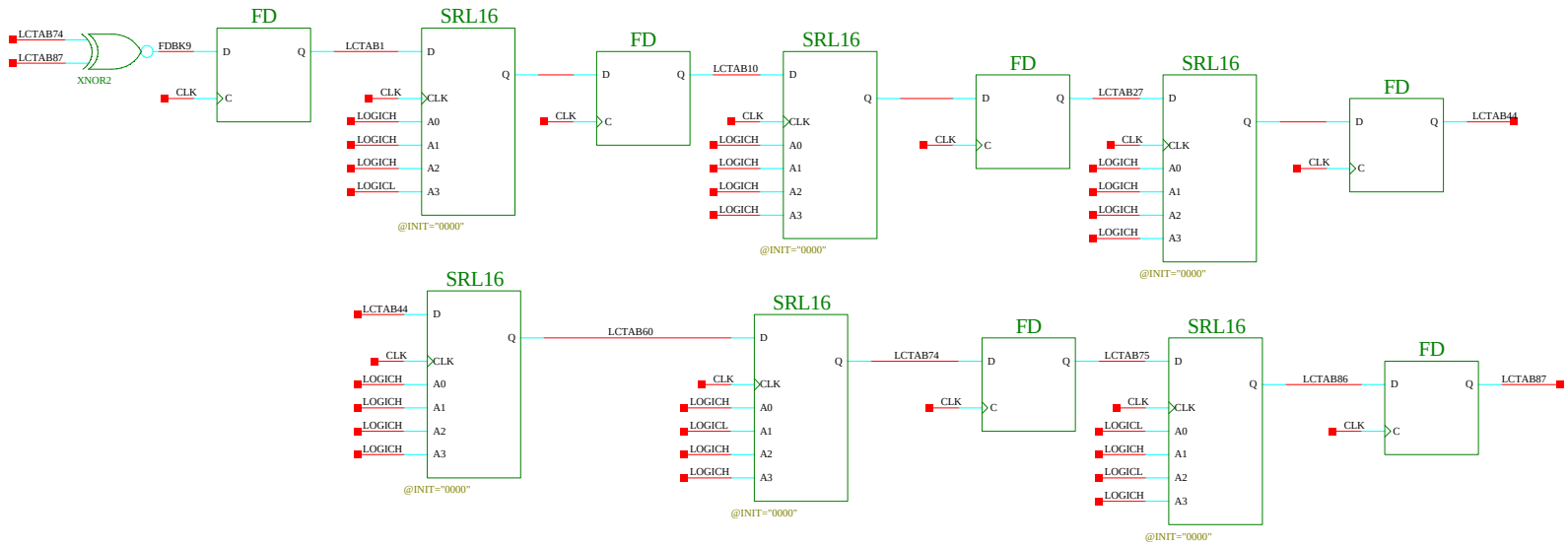


LCT5SEL[3:1] Trigger Rate (KHz)

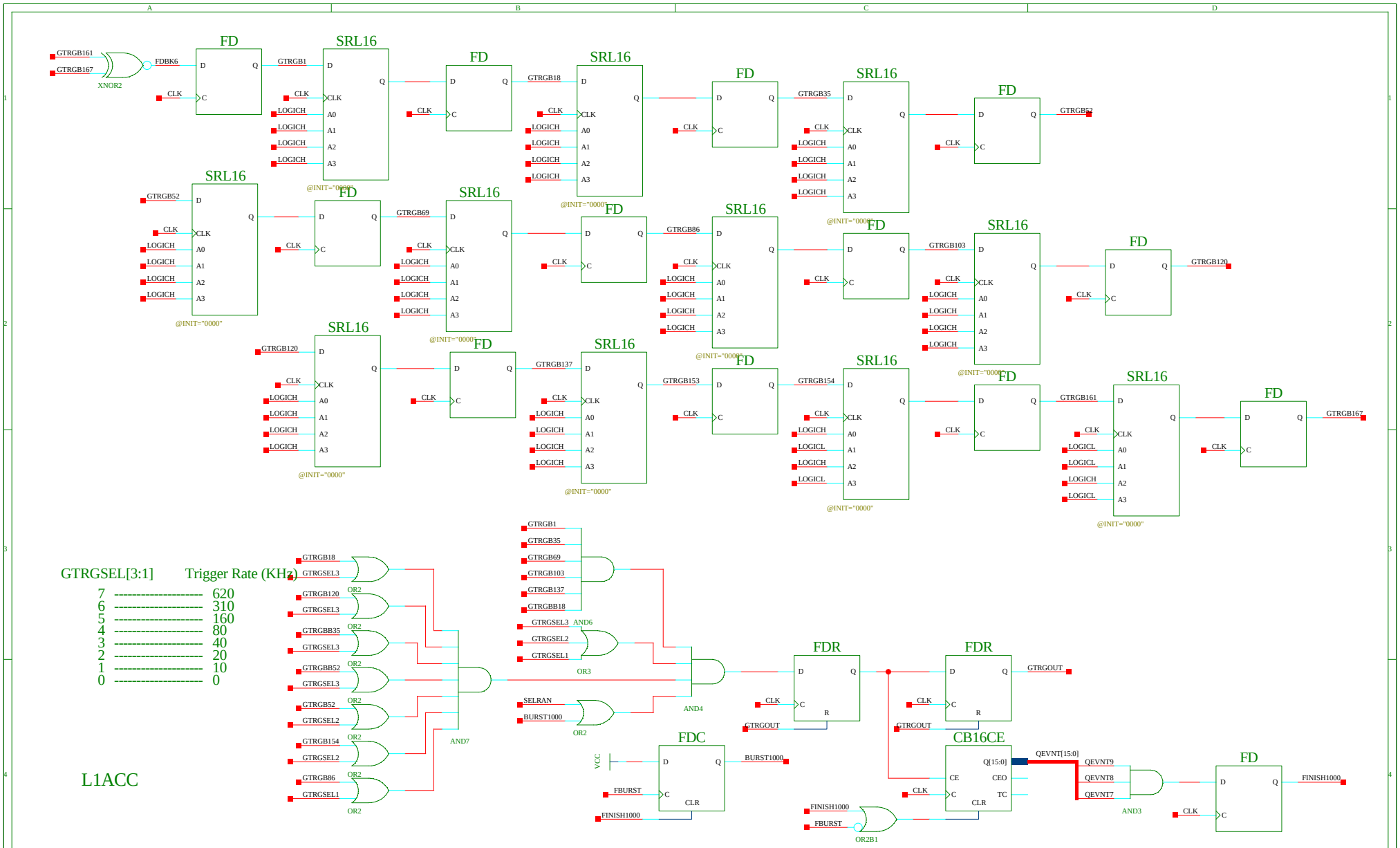
7	----------	620
6	----------	310
5	----------	160
4	----------	80
3	----------	40
2	----------	20
1	----------	10
0	----------	0

CFEB1 LCT

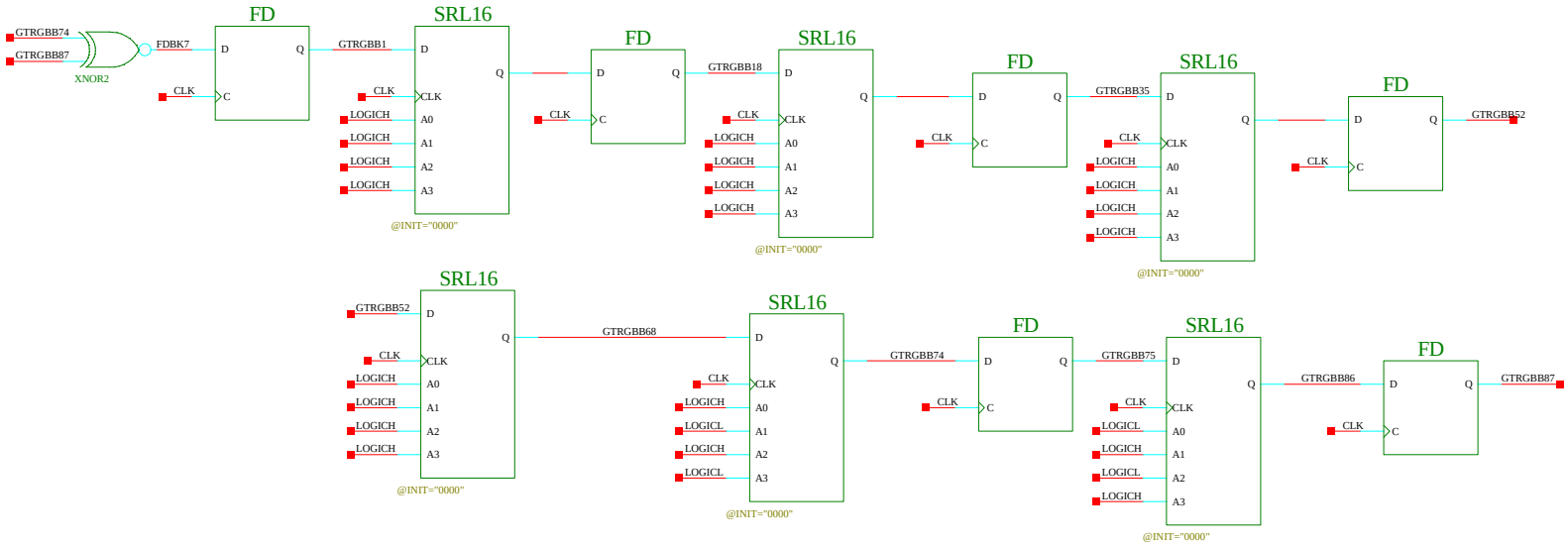
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Random LCT for CFEB5 DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A
		DATE: 1-14-2002_14:46	PROJECT: DAQMBC
		FILE: RANDOMTRG. 5	PAGE: 60D



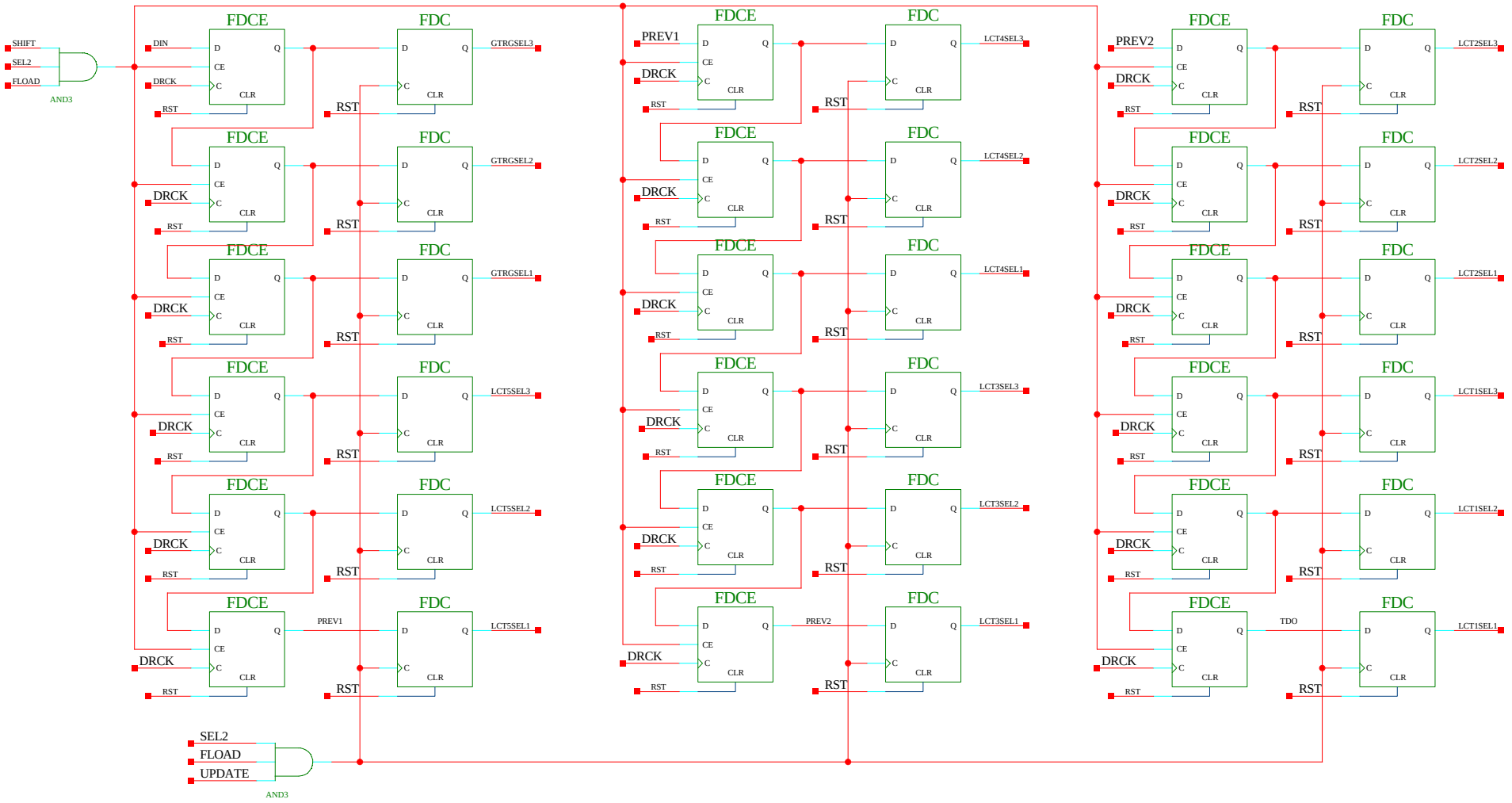
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: More Random LCT DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A	PROJECT: DAQMBC	
		DATE: 1-14-2002_15:07		FILE: RANDOMTRG. 6	PAGE: 60E



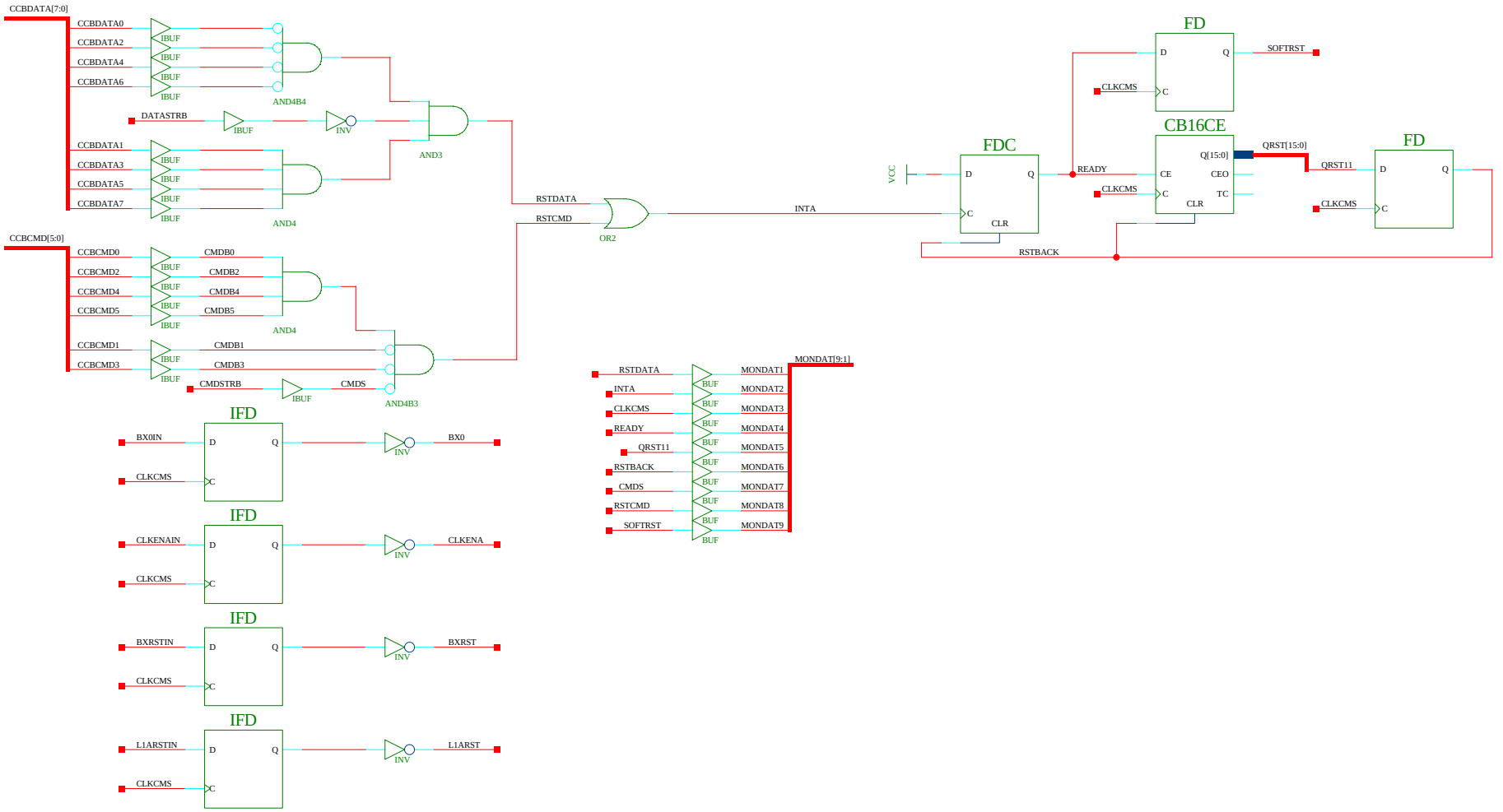
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Random L1ACC DAQ Motherboard Controller CMS CSC Electronics	BY: GU PARENT PAGE: 50A DATE: 1-14-2002_16:31	PROJECT: DAQMBC FILE: RANDOMTRG. 7 PAGE: 60F



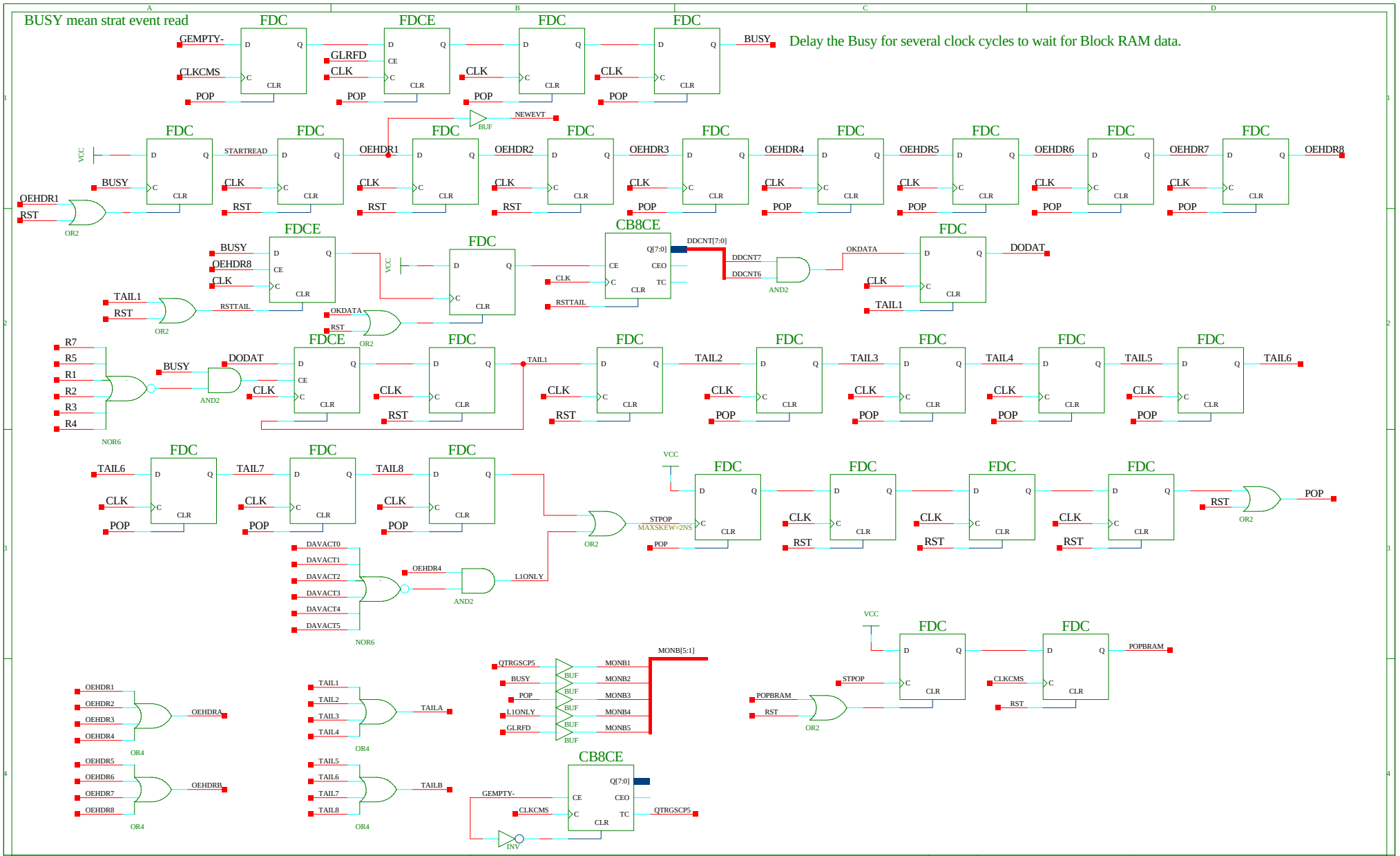
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: More Random L1ACC DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A	PROJECT: DAQMBC	
		DATE: 1-14-2002_14:39		FILE: RANDOMTRG. 8	PAGE: 60G



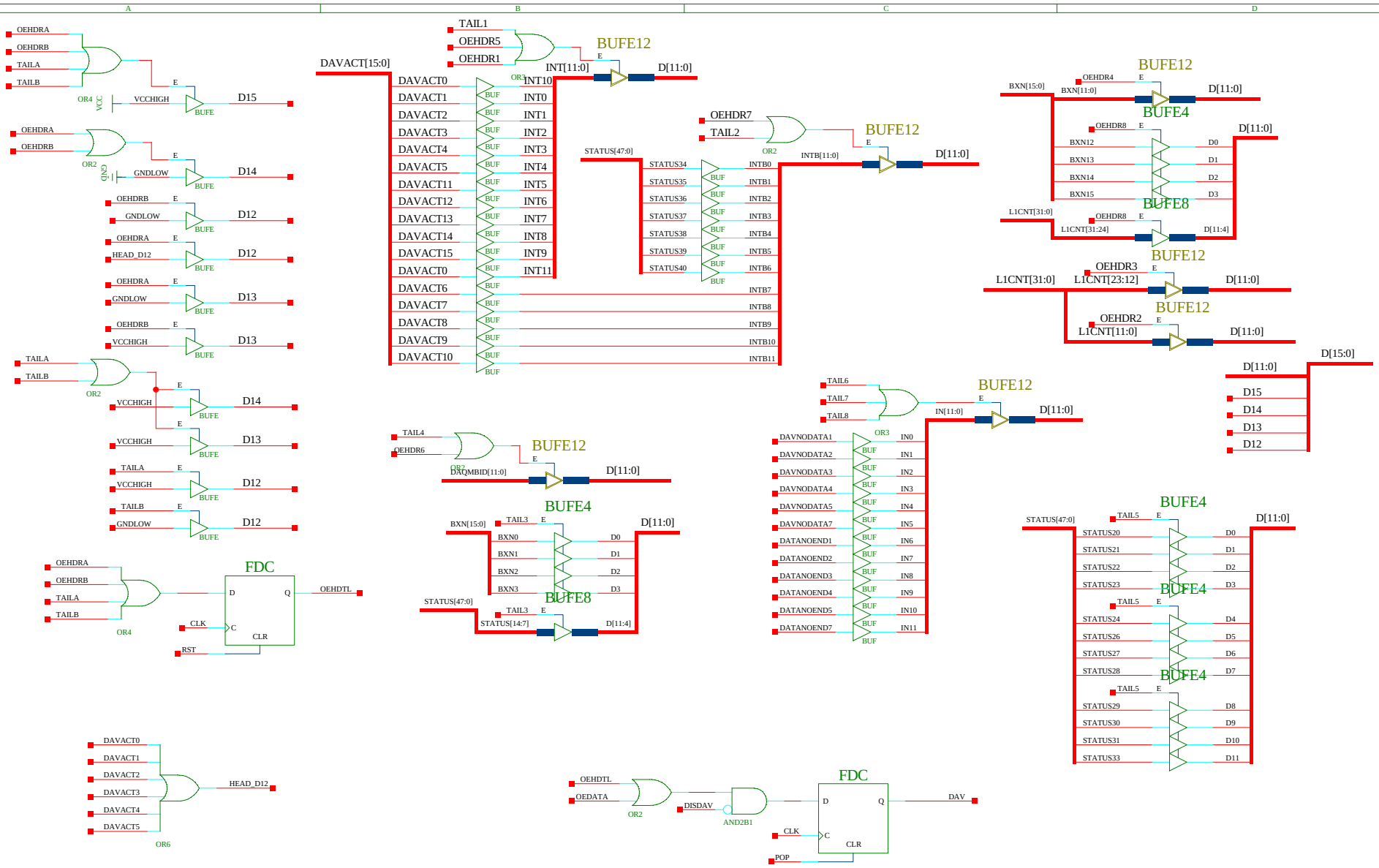
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Random Trigger Rate Selection DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 50A	PROJECT: DAQMBC
		DATE: 1-14-2002_14:39	FILE: RANDOMTRG . 9	PAGE: 60H



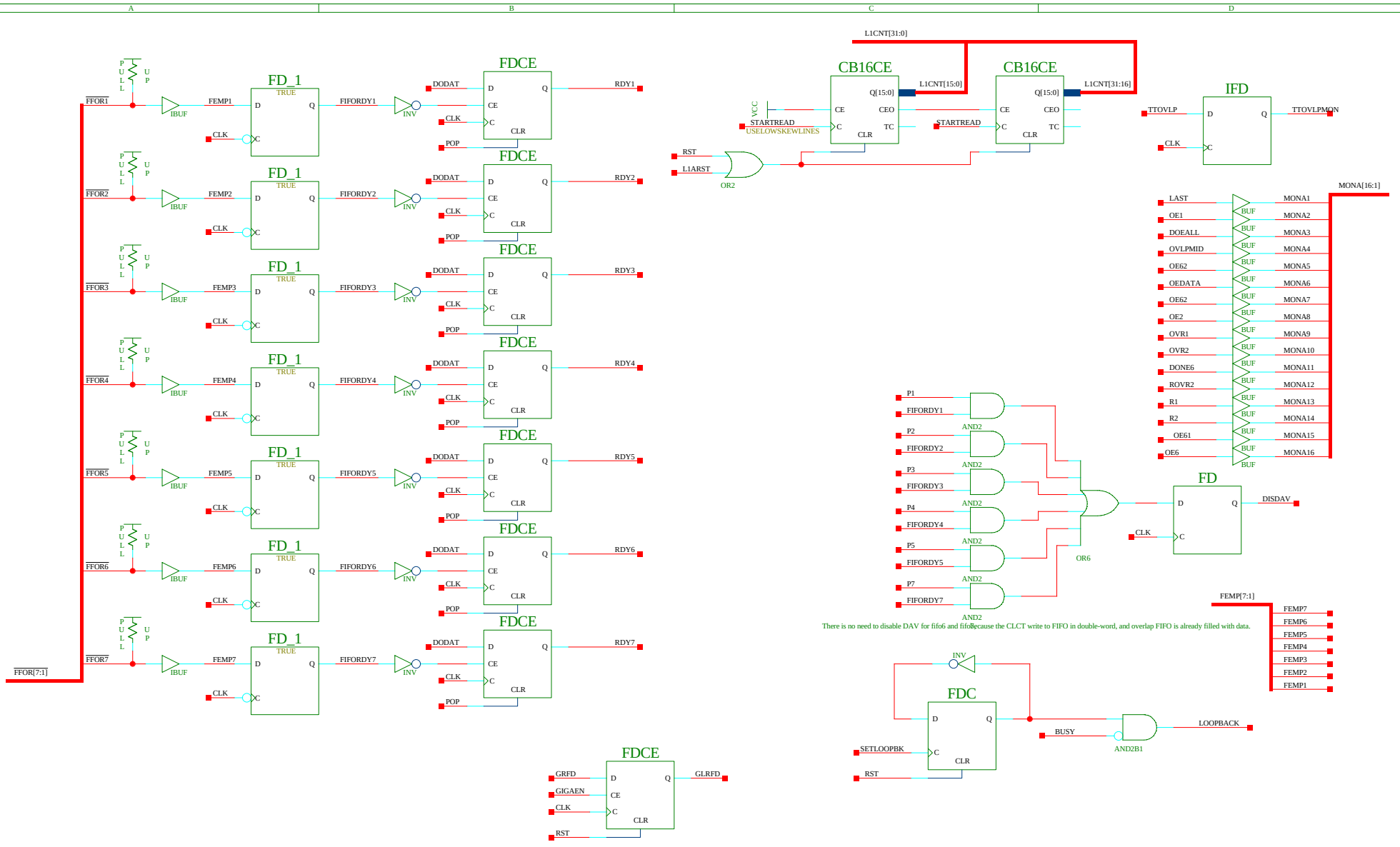
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CCB Command interface DAQMB Controller CMS CSC ELECTRONICS	BY: GU	PARENT PAGE: 2E	PROJECT: DAQMBC
		DATE: 3-18-2002_13:35	FILE: CCBCODE . 1	PAGE: 65



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Output Control Block, and Header/Trailer generation DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2F	PROJECT: DAQMBC
		DATE: 2-14-2002_16:40	FILE: CONTROL . 1	PAGE: 70

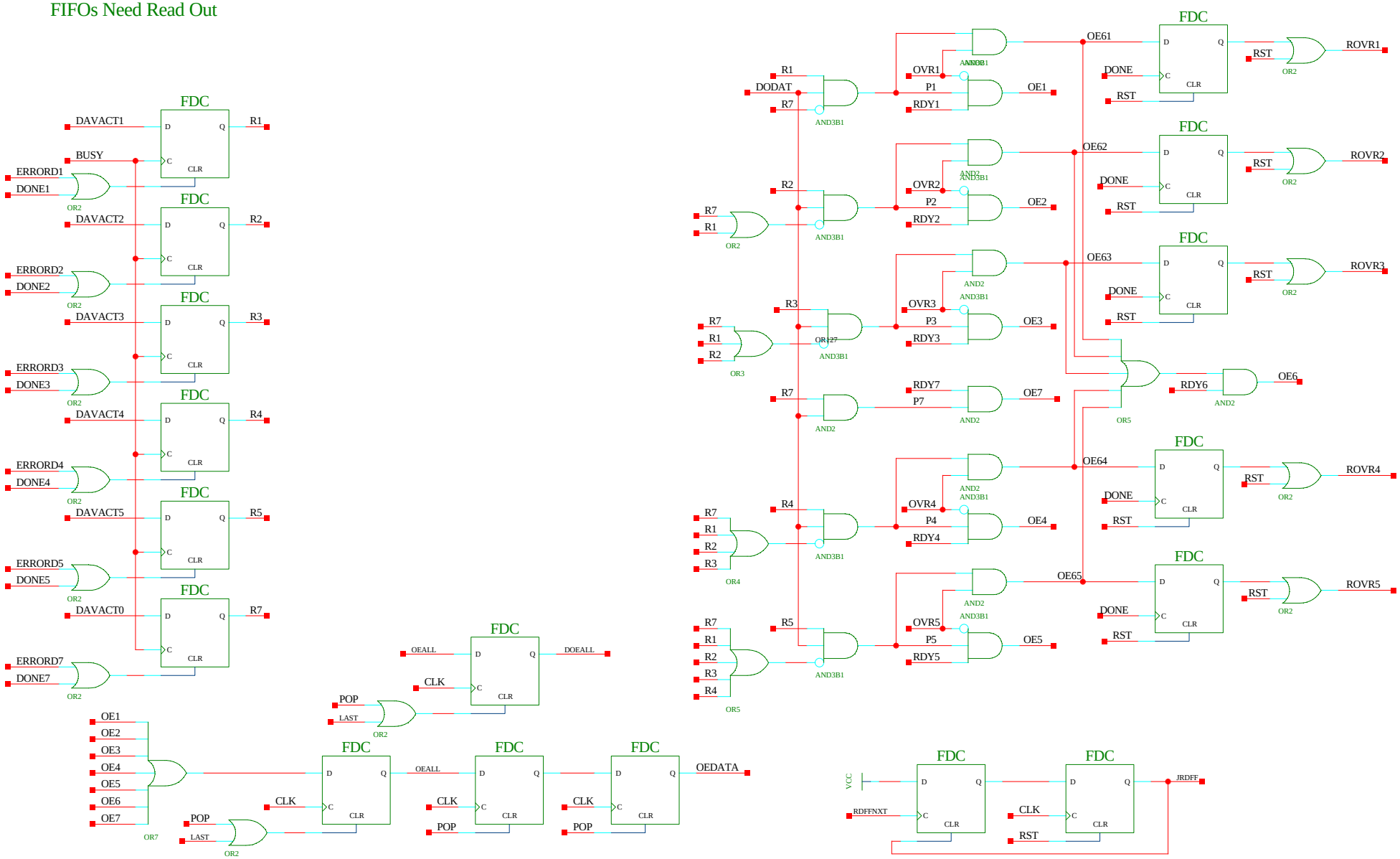


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Output Control Block, and Header/Trailer generation DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2F	PROJECT: DAQMBC
		DATE: 9-28-2001_11:34	FILE: CONTROL . 2	PAGE: 70A

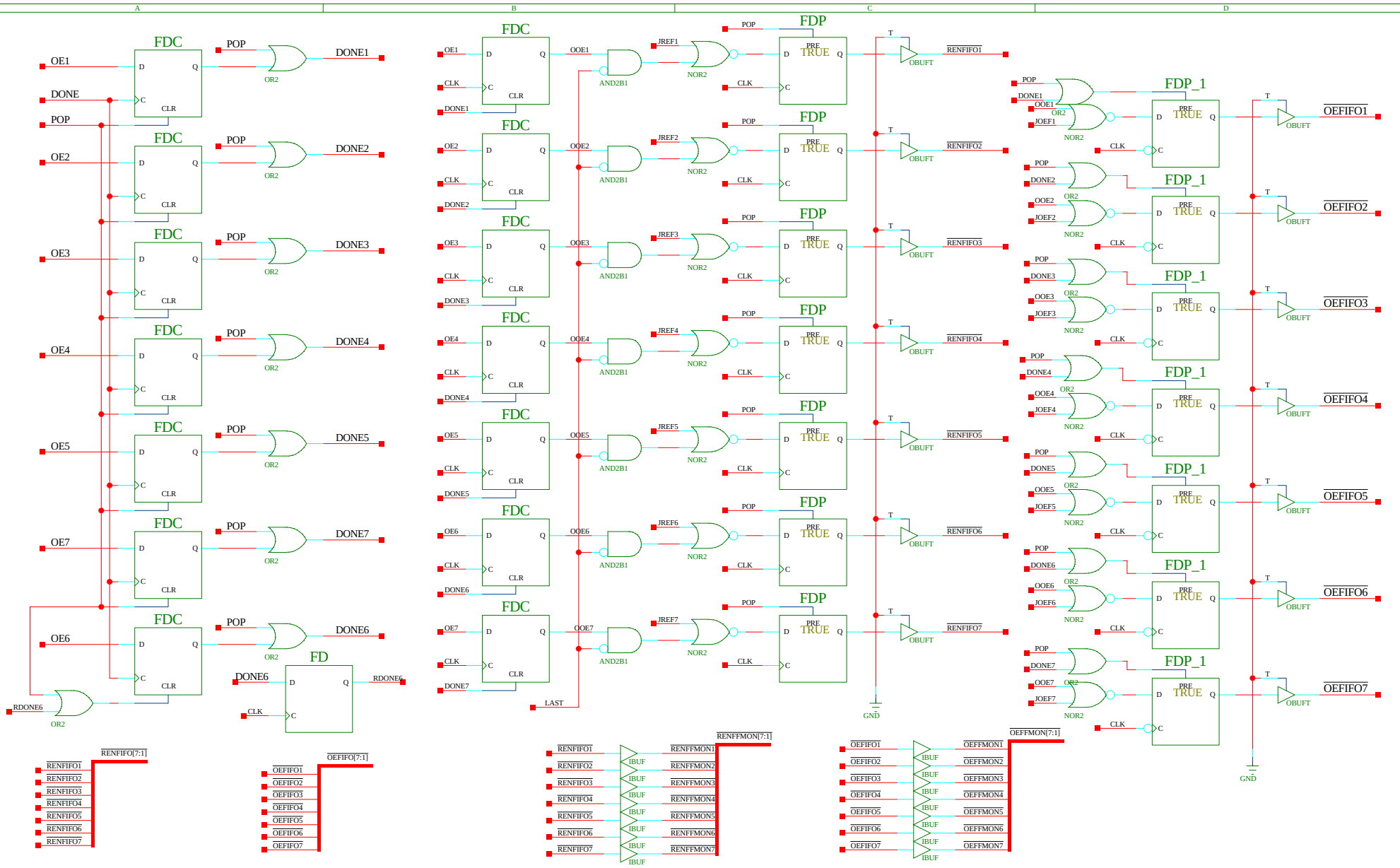


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: FIFO Readout Controller, Fifo Output Ready control DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2F	PROJECT: DAQMBC
		DATE: 12-7-2001_10:22	FILE: CONTROL . 3	PAGE: 70B

FIFOs Need Read Out



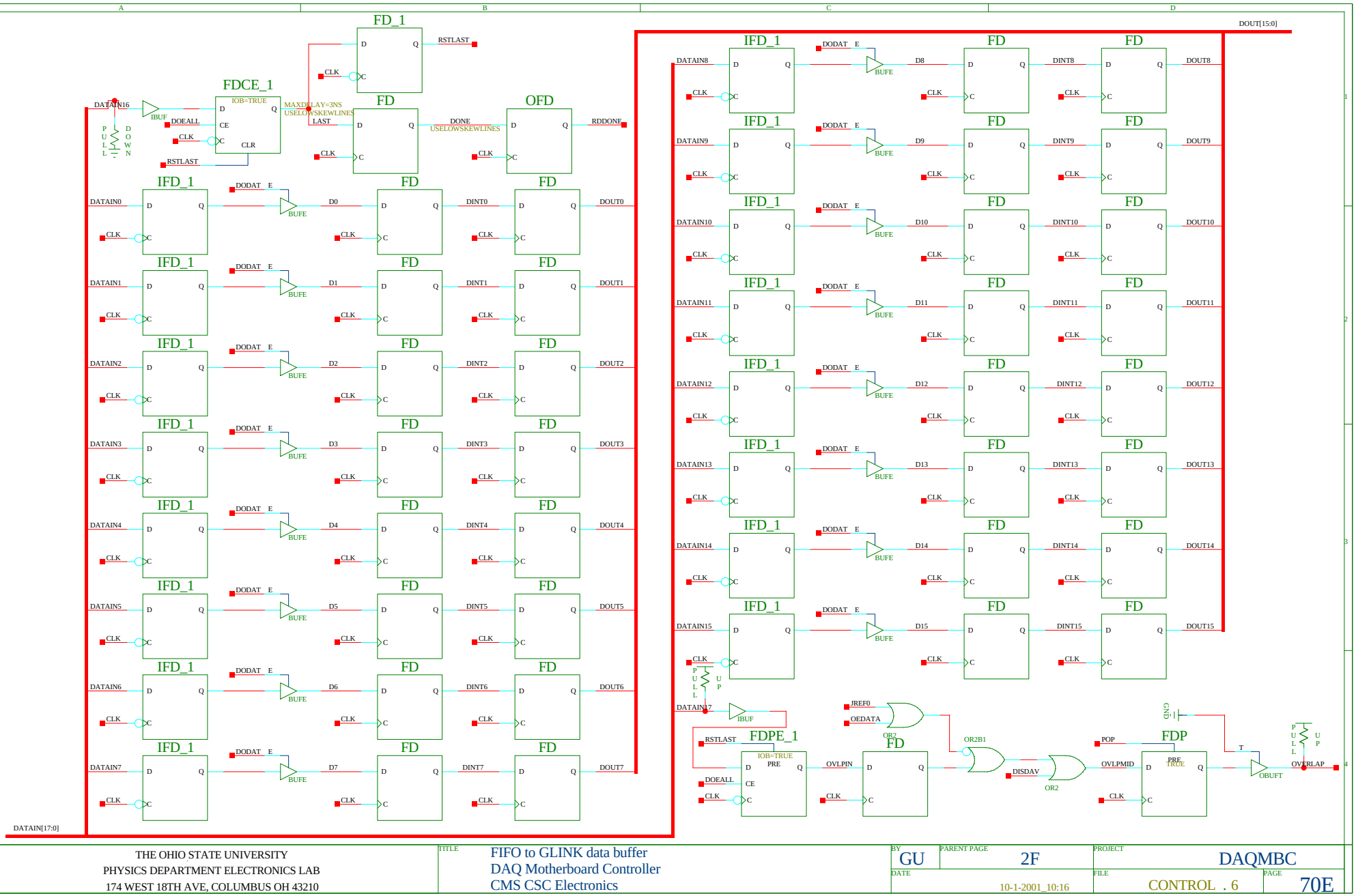
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: FIFO Readout Controller, esp. OVERLAP fifo controller DAQ Motherboard Controller CMS CSC Electronics	BY: GGS DATE: 10-1-2001_9:39	PARENT PAGE: 2F FILE: CONTROL . 4
		PROJECT: DAQMBC	PAGE: 70C



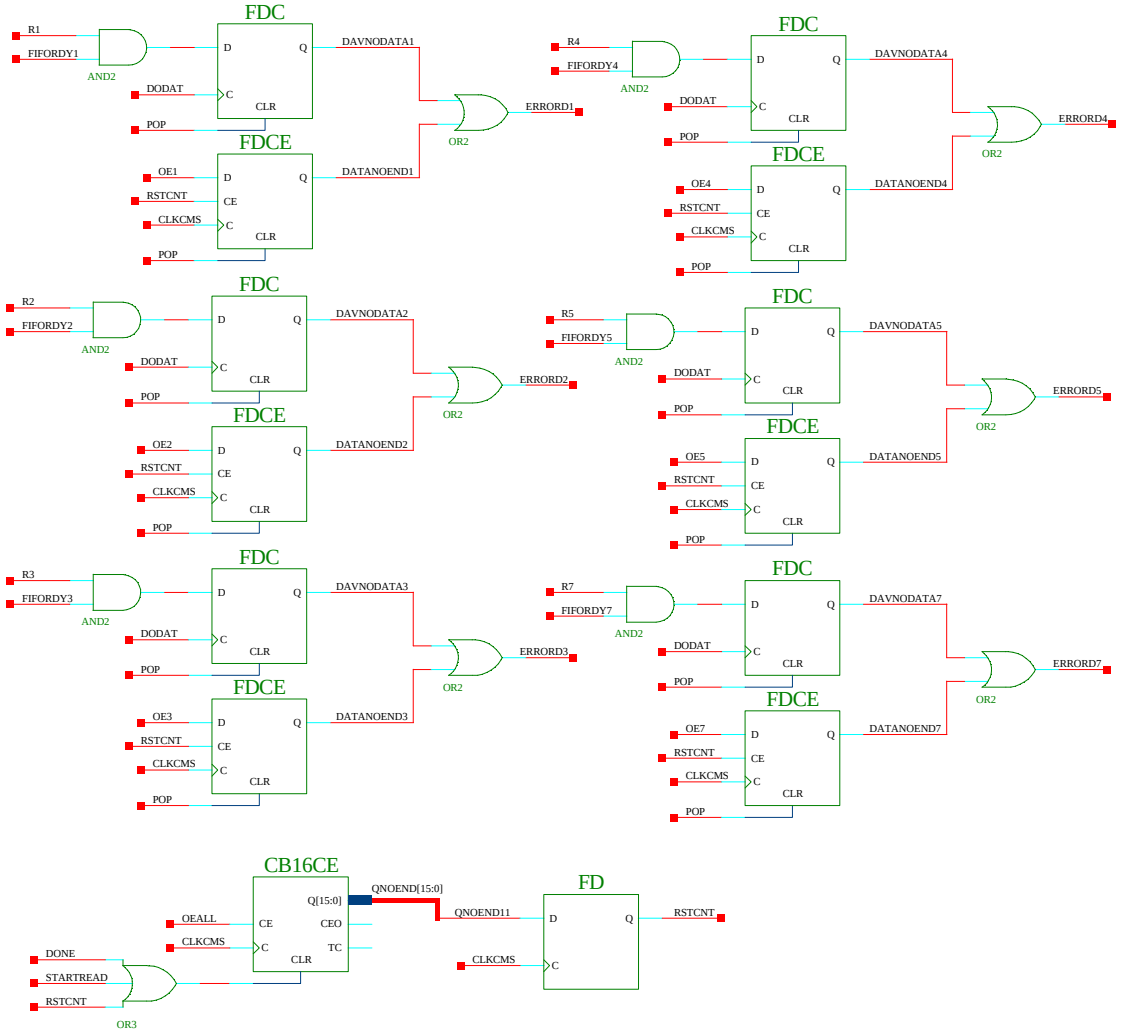
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: FIFO Readout Controller
DAQ Motherboard Controller
CMS CSC Electronics

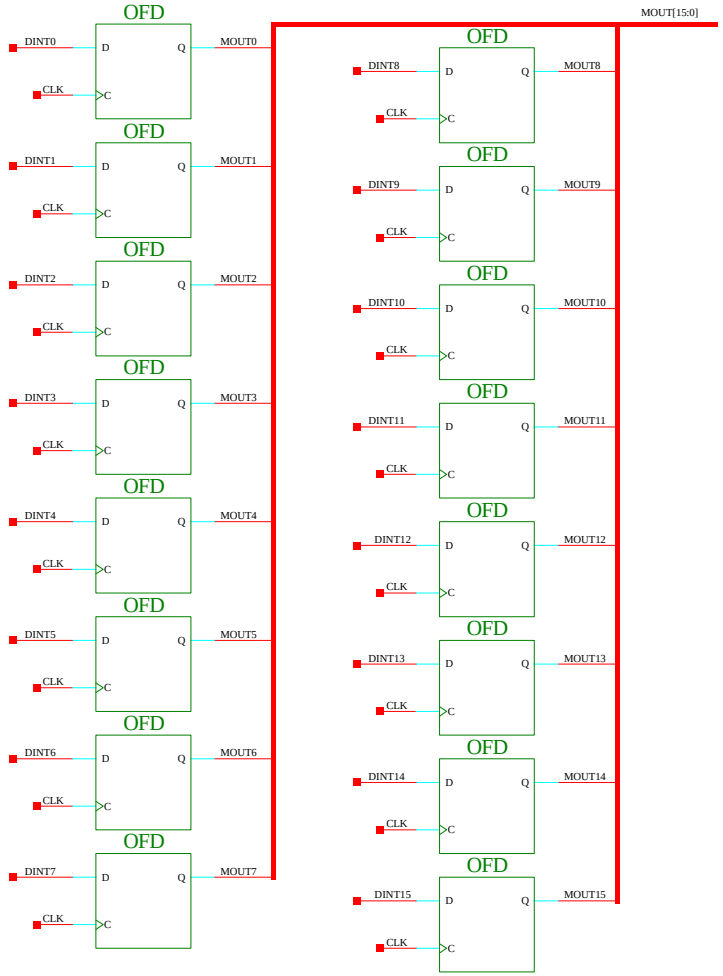
BY: GU
PARENT PAGE: 2F
PROJECT: DAQMBC
DATE: 10-1-2001_14:01
FILE: CONTROL . 5
PAGE: 70D



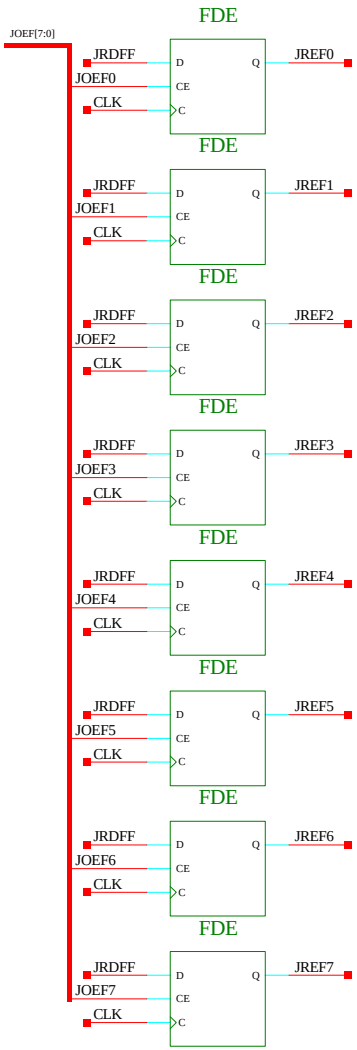
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: FIFO to GLINK data buffer DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2F	PROJECT: DAQMBC
		DATE: 10-1-2001_10:16	FILE: CONTROL . 6	PAGE: 70E

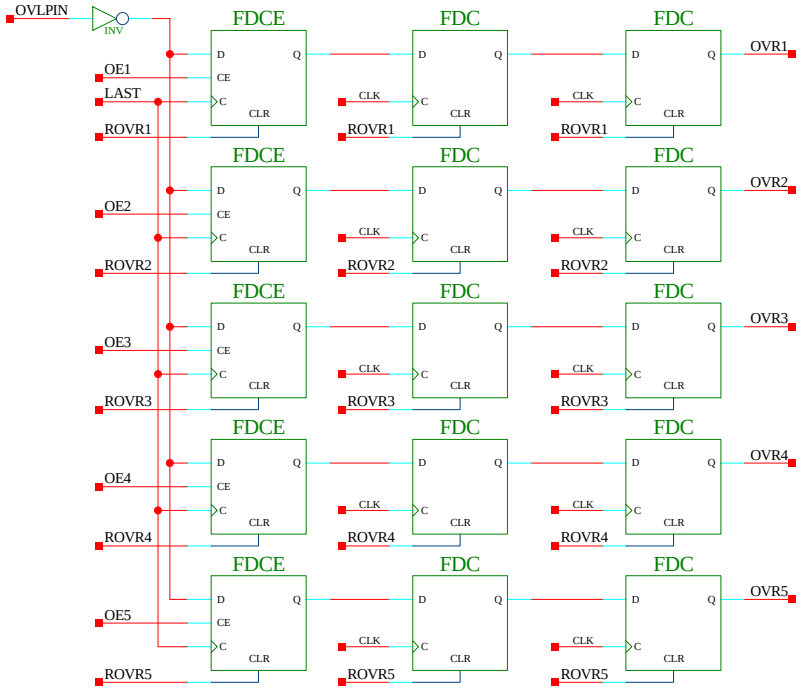


To Overlap FIFO, This is a duplicate output of DOUT[15:0] to minimize the 80MHz Bus leng



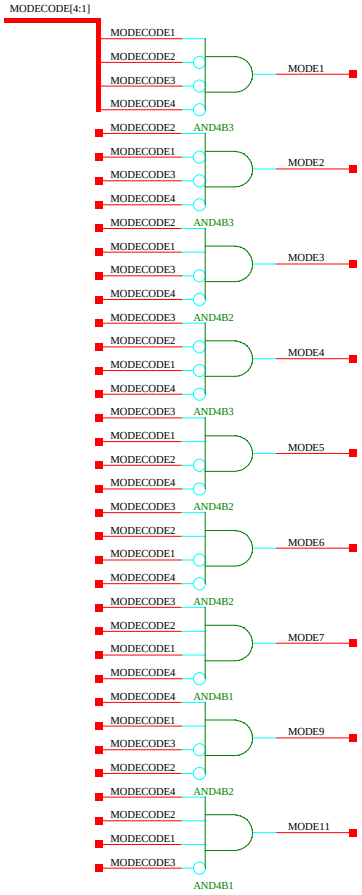
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Data Transfer timeout logic, Overlap FIFO data DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2F	PROJECT: DAQMBC
		DATE: 9-28-2001_11:59	FILE: CONTROL . 7	PAGE: 70F

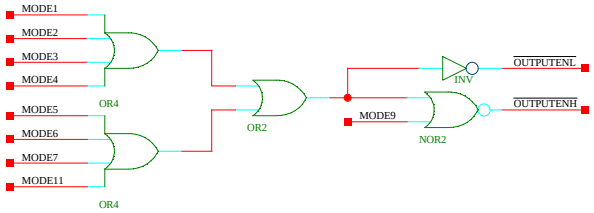




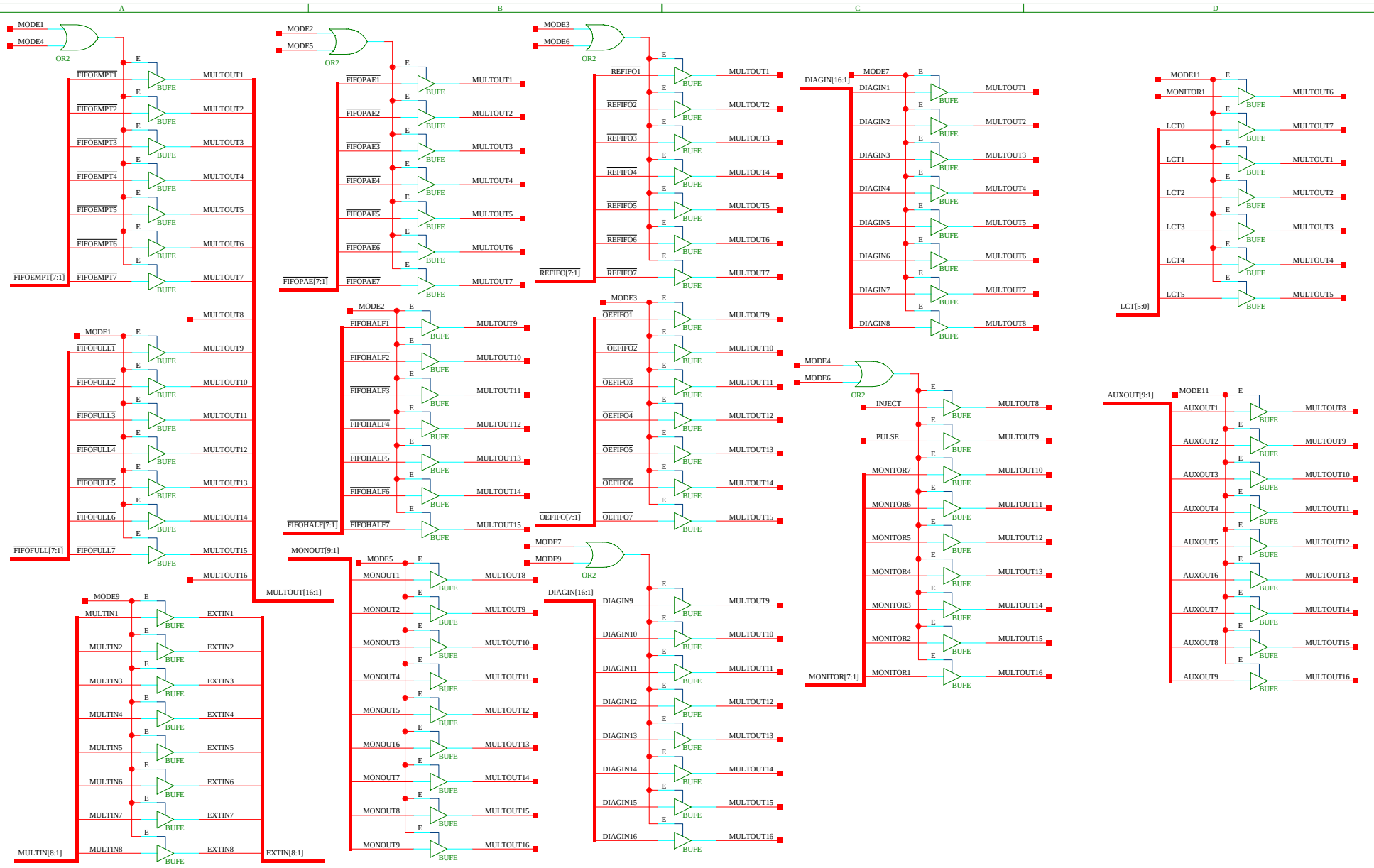
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: JTAG Read FIFO Control DAQ Motherboard Controller CMS CSC Electronics	BY: GU DATE: 10-1-2001_15:29	PARENT PAGE: 2F FILE: CONTROL . 8
		PROJECT: DAQMBC	PAGE: 70G

Mode Decode





THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Front Pannal Connector Control DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2G	PROJECT: DAQMBC
		DATE: 7-18-2001_13:38	FILE: FRONTMON . 1	PAGE: 80

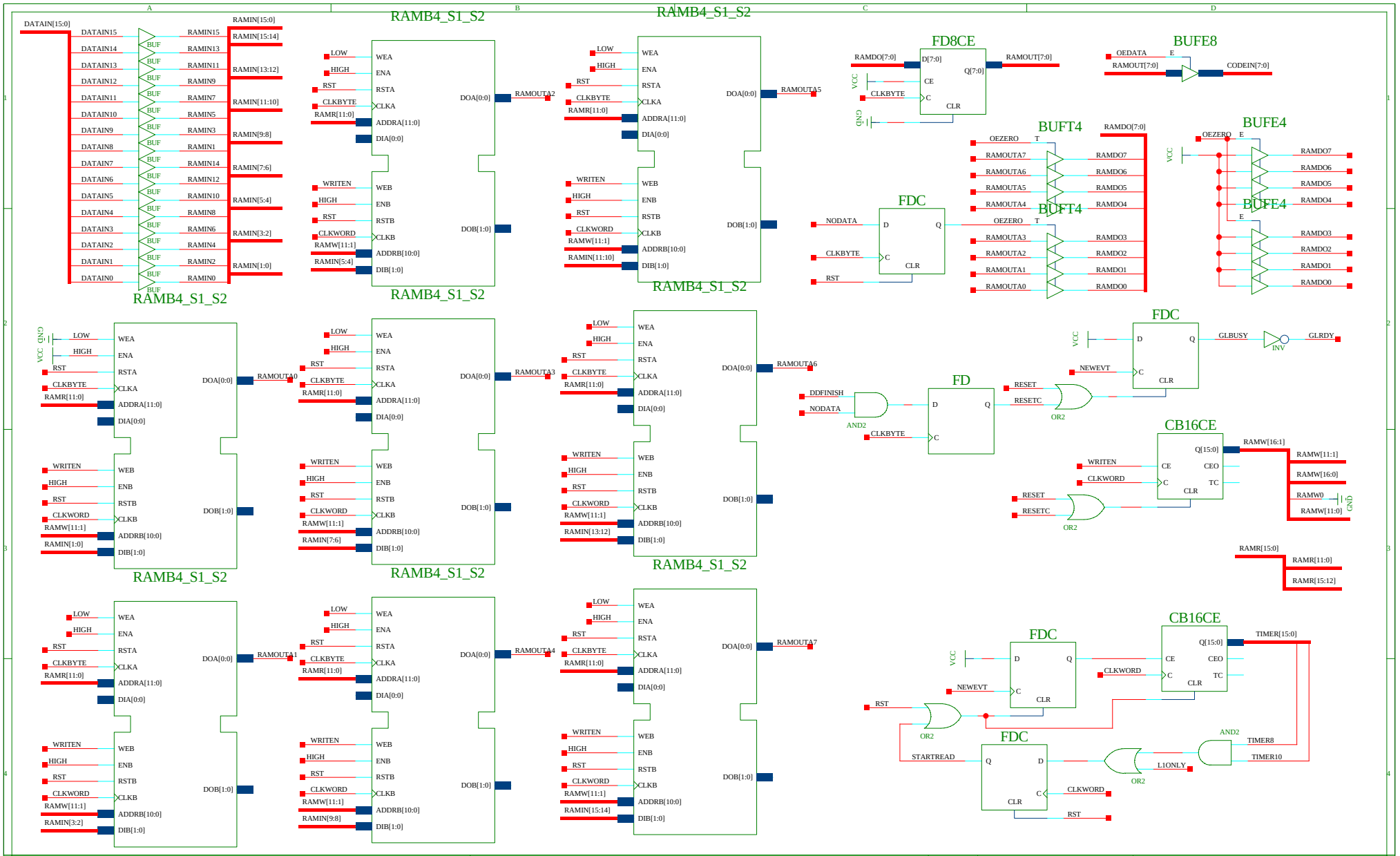


THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

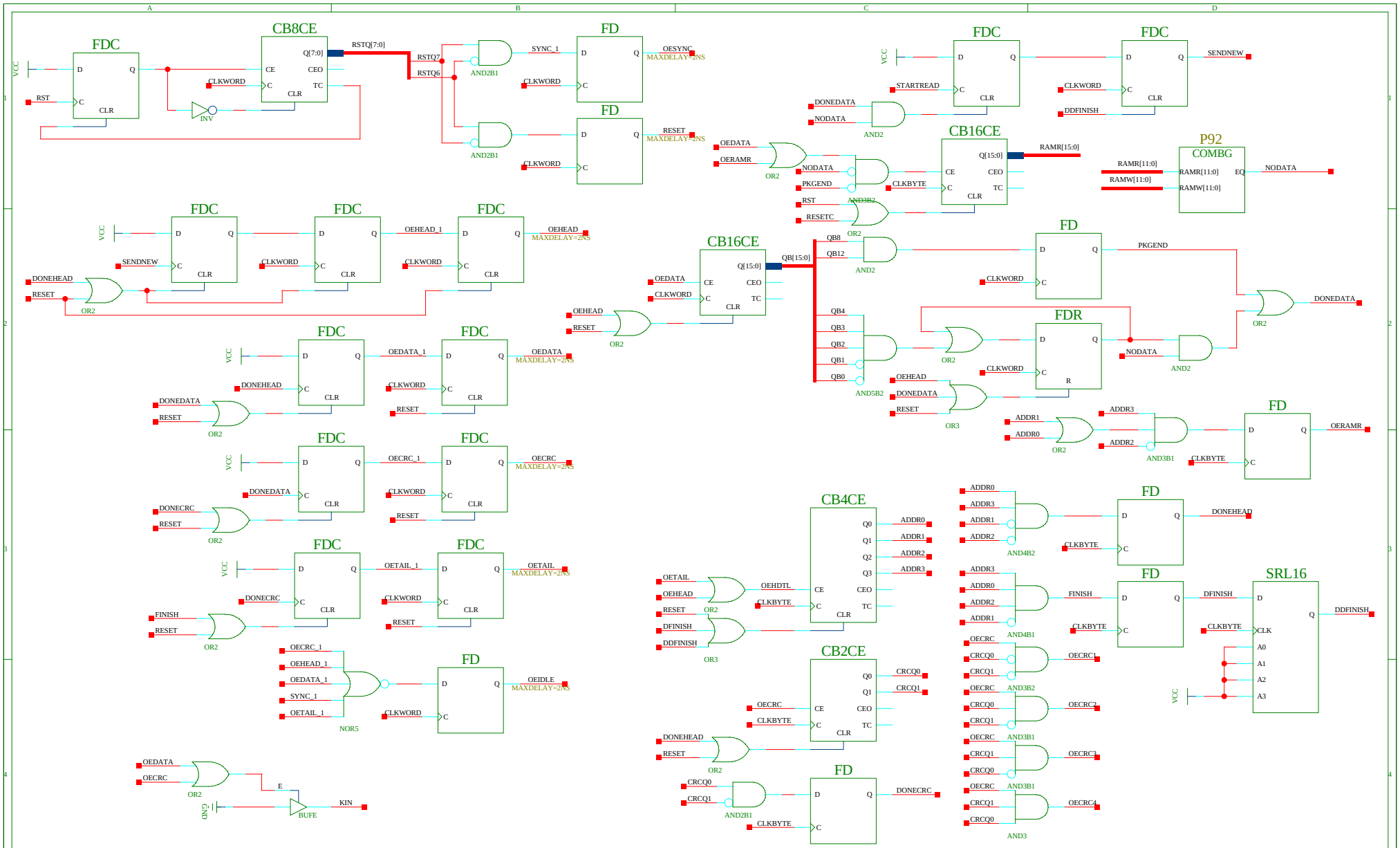
TITLE

Front Pannal Connector Control
DAQ Motherboard Controller
CMS CSC Electronics

BY GU	PARENT PAGE 2G	PROJECT DAQMBC	
DATE 1-4-2002_11:46		FILE FRONTMON_2	PAGE 80A

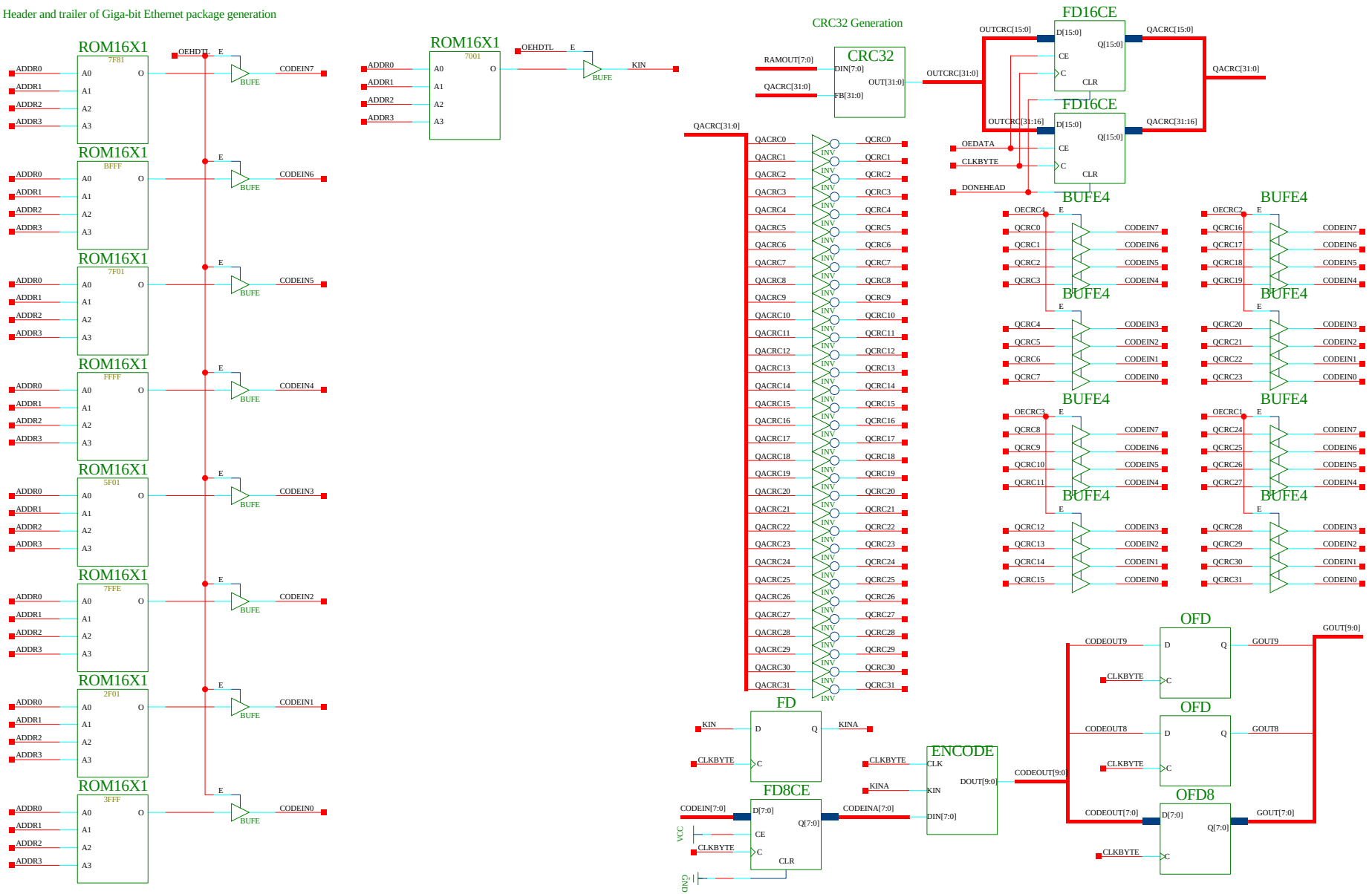


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Giga-bit Ethernet Interface DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2H	PROJECT: DAQMBC
		DATE: 12-6-2001_16:32	FILE: GIGANET . 1	PAGE: 90

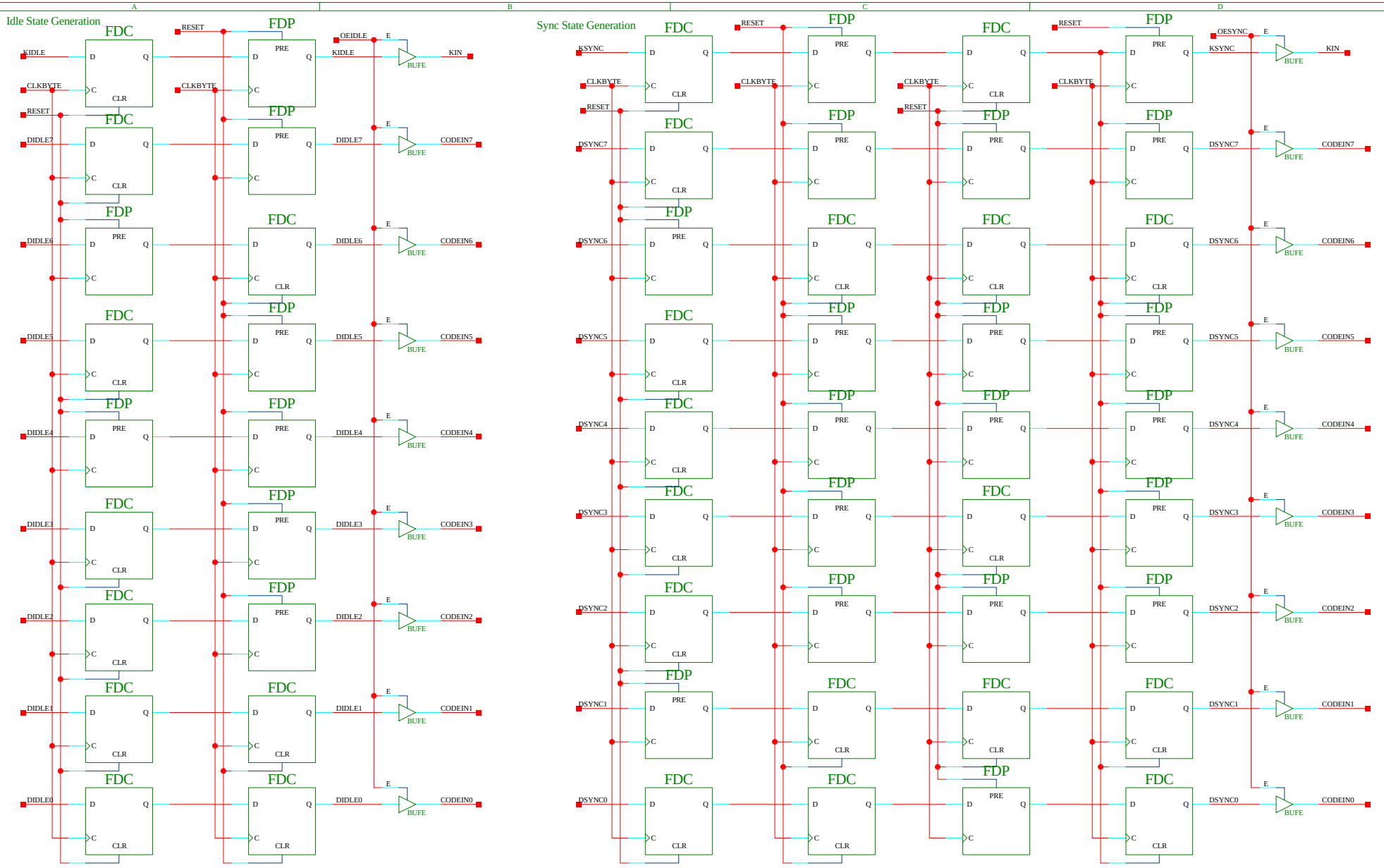


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Giga-bit Ethernet Interface DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2H	PROJECT: DAQMBC
		DATE: 12-7-2001_9:59	FILE: GIGANET . 2	PAGE: 90A

Header and trailer of Giga-bit Ethernet package generation



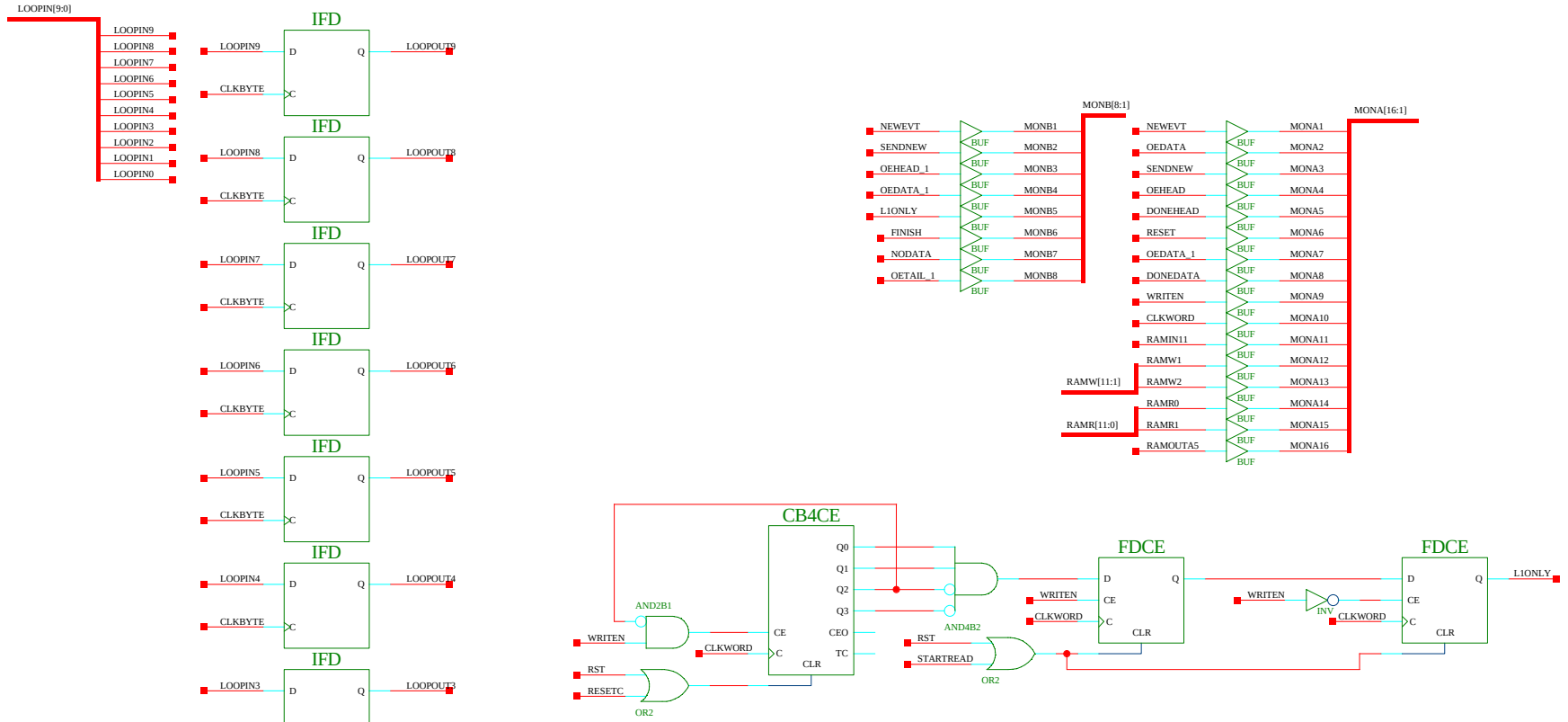
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Giga-bit Ethernet Interface DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 2H	PROJECT: DAQMBC
		DATE: 8-17-2001_10:15	FILE: GIGANET . 3	PAGE: 90B



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Giga-bit Ethernet Interface
DAQ Motherboard Controller
CMS CSC Electronics

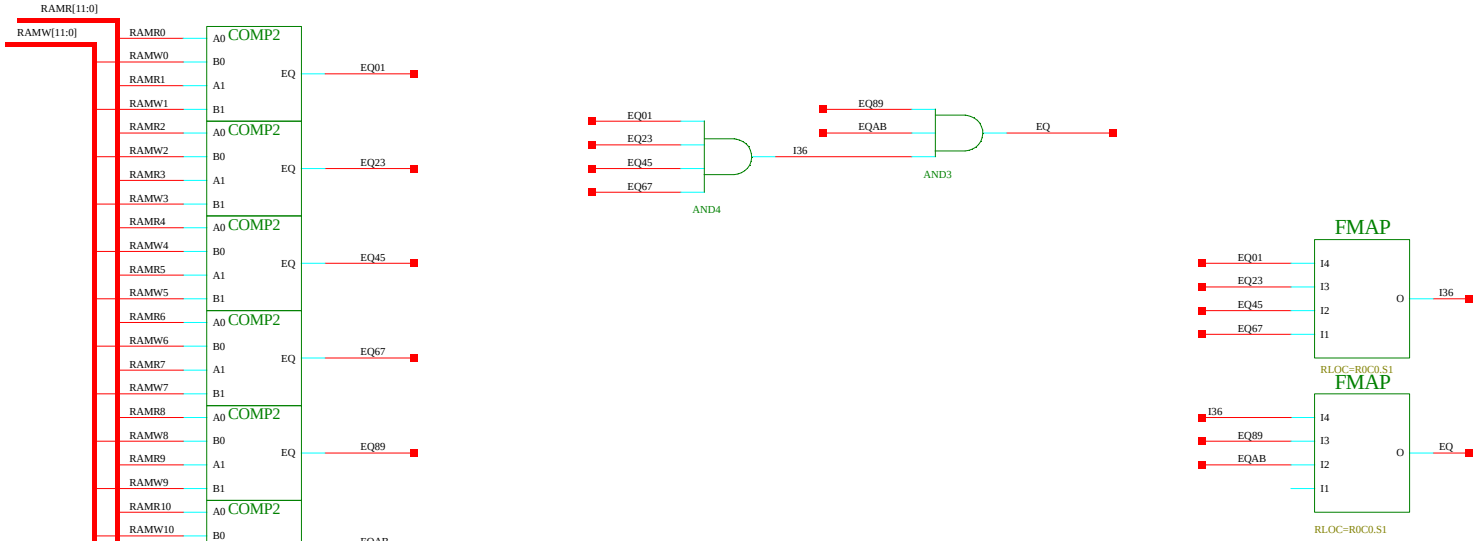
BY: GU
PARENT PAGE: 2H
PROJECT: DAQMBC
DATE: 8-15-2001_10:55
FILE: GIGANET . 4
PAGE: 90C



THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Giga-bit Ethernet Interface
DAQ Motherboard Controller
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
GU	2H	DAQMBC
DATE		FILE / PAGE
12-7-2001_9:48		GIGANET . 5 / 90D



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: 12 bit comparator, try to minimize the logic level DAQ Motherboard Controller CMS CSC Electronics	BY: GU	PARENT PAGE: 90A	PROJECT: DAQMBC
		DATE: 8-27-2001_8:43	FILE: COMBG . 1	PAGE: 92