DMB Data Format

General Data Format (when data is present)		
Word Type	Number of 16 bit words	Comments
Header	8 words	
TMB data	0 or xx words	Refer to UCLA documents
CFEB 1 data	0, 800 or 1600 words	8 or 16 time samples
CFEB 2 data	0, 800 or 1600 words	8 or 16 time samples
CFEB 3 data	0, 800 or 1600 words	8 or 16 time samples
CFEB 4 data	0, 800 or 1600 words	8 or 16 time samples
CFEB 5 data	0, 800 or 1600 words	8 or 16 time samples
Trailer	8 words	

General Data Format (when data is absent)		
Word Type	Number of 16 bit words	Comments
Header	4 words	

Note : Data can be present in any combination of TMB, or CFEBx including TMB data only. However regardless of the combination of data, the order indicated above is always observed.

DMB Data Format

Decode of Special Word Flags					
Bit Position					
15	14	13	12	Meaning	Comments
0	X	X	d12	Data Words 1 thru 96 Bit 12 : high order data bit Bit 13 : Serialized SCA info Bit 14 : ~OVERLAP flag	Bits 12 -13 have the meaning shown at the left for data words 1 thru 96.
0	R14	R13	R12	High order bits of 15 bit CRC register	Data Word 97 of one time sample
0	1	1	1	CFEB information word	Data Word 98, 99, and 100
1	0	0	0	Header Word 1-4 for no data case	
1	0	0	1	Header Word 1-4 for data exist case	
1	0	1	0	Header Word 5-8 for data exist case	
1	0	1	1	Reserved	
1	1	0	0	Reserved	
1	1	0	1	Reserved	
1	1	1	0	Trailer Word 5-8 for data exits case	
1	1	1	1	Trailer Word 1-4 for data exits case	

Note: Bit 15 distinguishes between data words and header/trailer words. However within data type words, bits 12, 13, and 14 can not be used to uniquely identify the CFEB information words. This must be accomplished by the relative position in the current time sample.

DMB Data Format

Header Format (when data is present)																	
	Bit Positions																
Header	special word flags				Event Information Bits												
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Comments
1	1	0	0	1	TMB Data Avl.	LCT's sent to Active FEB's 5..1						CFEB 5..1 Data Available					
2	1	0	0	1	L1ACC [11:0]												
3	1	0	0	1	L1ACC [23:12]												
4	1	0	0	1	Bunch Crossing Number [11:0]												
5	1	0	1	0	TMB Data Avl.	LCT's sent to Active FEB's 5..1						CFEB 5..1 Data Available					Duplicate of Header Word 1
6	1	0	1	0	Peripheral Crate ID								DMB Board ID				
7	1	0	1	0	Multi-event overlap CFEB 5..1					TMB ~HF	OVLP ~HF	FIFO ~HALF FULL flags CFEB 5..1					Note inverted logic for ~HF
8	1	0	1	0	L1ACC [31:24]								BCN [15:12]				

Header Format (when data is absent)																	
	Bit Positions																
Header	special word flags				Event Information Bits												
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Comments
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
2	1	0	0	0	L1ACC [11:0]												
3	1	0	0	0	L1ACC [23:12]												
4	1	0	0	0	Bunch Crossing Number [11:0]												

Trailer Format (when data is present)																	
	Bit Positions																
Trailer	special word flags				Event Information Bits												
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Comments
1	1	1	1	1	TMB Data Avl.	LCT's sent to Active FEB's 5..1						CFEB 5..1 Data Available					Duplicate of Header Word 1
2	1	1	1	1	Multi-event overlap CFEB 5..1					TMB ~HF	OVLP ~HF	FIFO ~HALF FULL flags CFEB 5..1					Duplicate of Header Word 7
3	1	1	1	1	Number of L1ACC's in FIFO in DMB Controller FPGA								BCN [3:0]				
4	1	1	1	1	Peripheral Crate ID								DMB Board ID				Duplicate of Header Word 6
5	1	1	1	0	TMB ~FF	FIFO ~FULL flags CFEB 5..1					TMB ~FE	FIFO ~EMPTY flags CFEB 5..1					Note inverted logic
6	1	1	1	0	TMB TO	Time out reading data CFEB 5..1					TMB no data	no data found when expected CFEB 5..1					
7	1	1	1	0	TMB TO	Time out reading data CFEB 5..2					TMB no data	no data found when expected CFEB 5..2					Duplicate of Trailer Word 6
8	1	1	1	0	TMB TO	Time out reading data CFEB 5..3					TMB no data	no data found when expected CFEB 5..3					Duplicate of Trailer Word 6

CFEB Data Format for one Time Sample

	Bit Position			ADC Value (12+1 bits)	
Word	15	14	13	Layer	Channel
1	0	OVLP	b0	3	0
2	0	OVLP	b0	1	0
3	0	OVLP	b0	5	0
4	0	OVLP	b0	6	0
5	0	OVLP	b0	4	0
6	0	OVLP	b0	2	0
7	0	OVLP	b1	3	1
8	0	OVLP	b1	1	1
9	0	OVLP	b1	5	1
10	0	OVLP	b1	6	1
11	0	OVLP	b1	4	1
12	0	OVLP	b1	2	1
13-18	0	OVLP	b2	3,1,5,6,4,2	3
19-24	0	OVLP	b3	3,1,5,6,4,2	2
25-30	0	OVLP	b4	3,1,5,6,4,2	6
31-36	0	OVLP	b5	3,1,5,6,4,2	7
37-42	0	OVLP	b6	3,1,5,6,4,2	5
43-48	0	OVLP	b7	3,1,5,6,4,2	4
49-54	0	OVLP	b8	3,1,5,6,4,2	12
55-60	0	OVLP	b9	3,1,5,6,4,2	13
61-66	0	OVLP	b10	3,1,5,6,4,2	15
67-72	0	OVLP	b11	3,1,5,6,4,2	14
73-78	0	OVLP	b12	3,1,5,6,4,2	10
79-84	0	OVLP	b13	3,1,5,6,4,2	11
85-90	0	OVLP	b14	3,1,5,6,4,2	9
91-96	0	OVLP	b15	3,1,5,6,4,2	8

Serialized SCA data bit definitions

Serialized bit	
b0	LCT position relative to SCA Capacitors
b1	
b2	
b3	
b4	
b5	
b6	
b7	
b8	SCA block number
b9	
b10	
b11	
b12	L1ACC Phase (20 MHz SCA clock high or low)
b13	LCT Phase (20 MHz SCA clock high or low)
b14	SCA Overwrite
b15	Time Samples (1=16 time samples, 0=8 time samples)

	Bit Position															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
97	0	15 bit CRC register bits. (Only the low 13 bits are checked in hardware)														
98	0	1	1	1	L1ACC buffer empty	LCT buffer empty	L1ACC buffer full	LCT buffer full	Current LCT FIFO depth				Free SCA Blocks (10 max)			
99	0	1	1	1	System Busy	SCA overwrite	PUSH valid data	LCT buffer POP	Current L1ACC FIFO depth							
100	0	Garbage bits														