

DAQMBP

CMS CSC DAQ Motherboard PCB Schematic

PRODUCTION

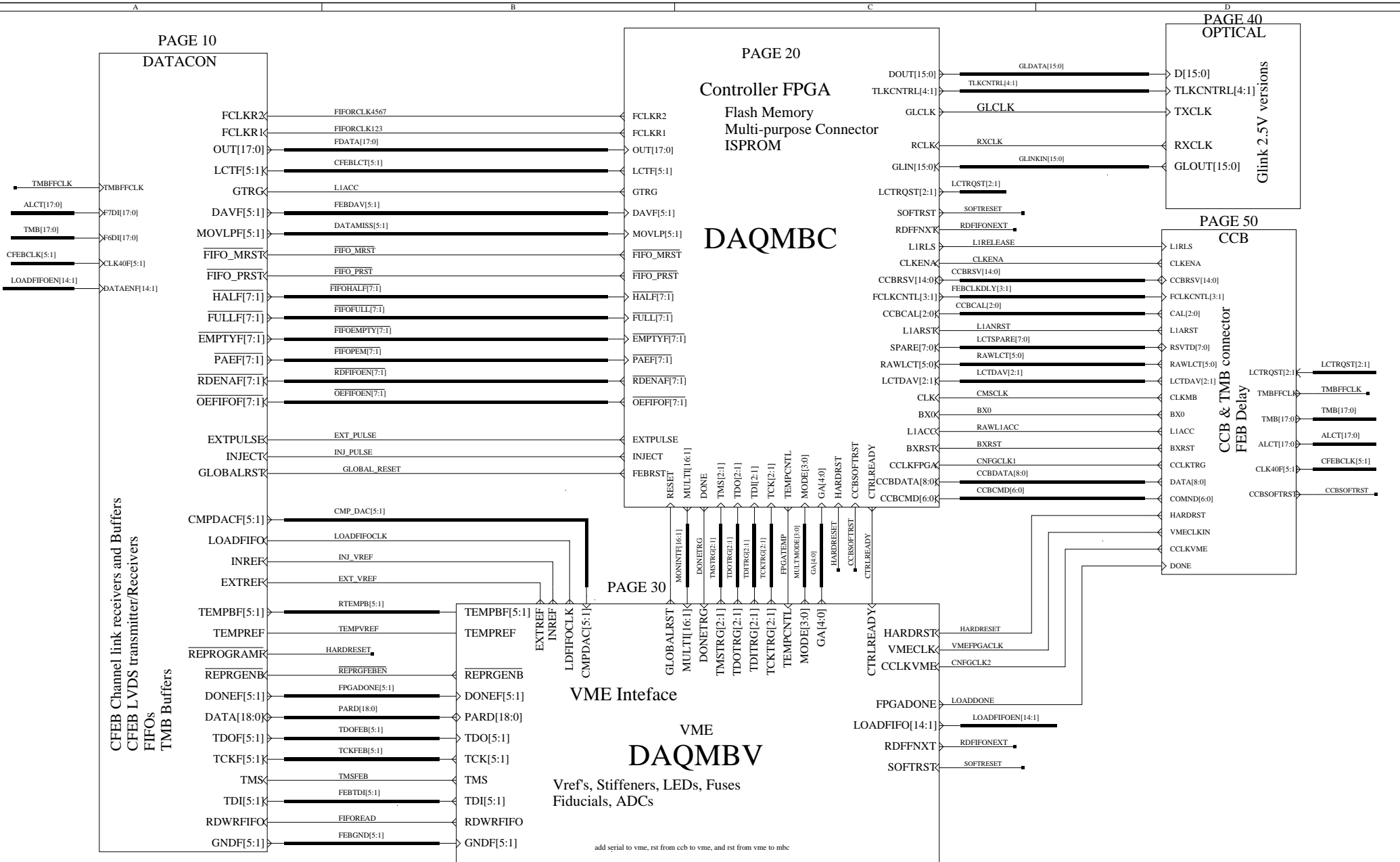
MBRD_BLK

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

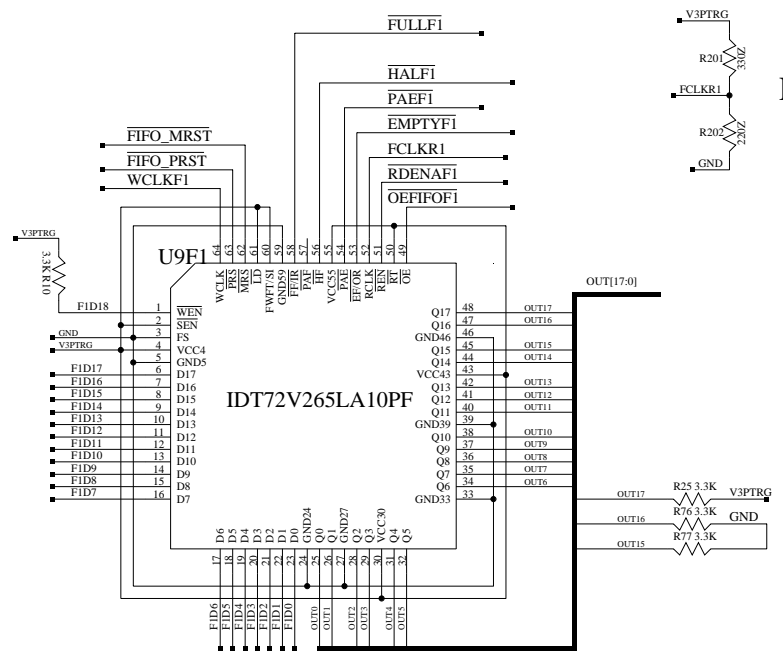
DAQMB, It check and concentrate the DATA (CFEB, CLCT/TMB/ALCT) from one chamber, and then send to DDU

Oct. 23, 2000: Modify the design based on m:\wv\d741t\rev3\, an intermediary design
Nov. 1, 2000: The new scheme is ready, need update the CCB link, and CLCT/TMB link, and possibly CLCT/TMB FIFO.
Nov. 2, 2000: Preliminary design is ready. Need feedback from Dan, and coordination with UCLA, Rice and FLorida for backplane
Dec. 6, 2000: Double checked the signals by feed backs from FPGA design
Jan. 18, 2001: Modify the ADC design, use three MAX1271, and one ADS7809/AD977
Jan. 22, 2001: Modify the Backplane interface design. For CCB, use GTLP/LVTTL transceiver, TMB, use FPGA GTLP property
Feb. 7, 2001: Modify according to backplane PCB design, Add Flash ram
Feb. 14, 2001: Double check, and modify the VME interface and "emergency" handling
Feb. 26, 2001: Further check, Changed the DAC to MAX5154
Mar. 5, 2001: Add TLK2501/1501 for GLINK, and Changed the Temprature ADC Refs
July 3, 2001: Modifications by the Rev3 PCB debug
Nov. 20, 2001: New Rev5, Major change: Virtex-E --> Virtex-II, CPLD --> Discrete logic
Mar. 12, 2002: Use radiation-tolerant part, like the SHARP regulator.
Dec. 17, 2002: Add one fifo for ALCT data, change the TMB fifo to 18-bit wide; using AT49BV512 flash memory
Jan. 10, 2003: Add the termination for clock signals
June, July, 2003: Modify the resister values, and add a clock driver for FPGA gigabit clock
Sept. 24, 2003: Finalize the Parallel Flash memory, added an inductor for +5V.
Sept. 25, 2003: Final check on the schematics for production of ten boards

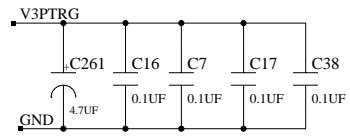
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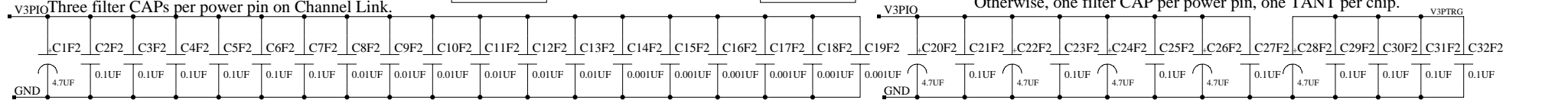
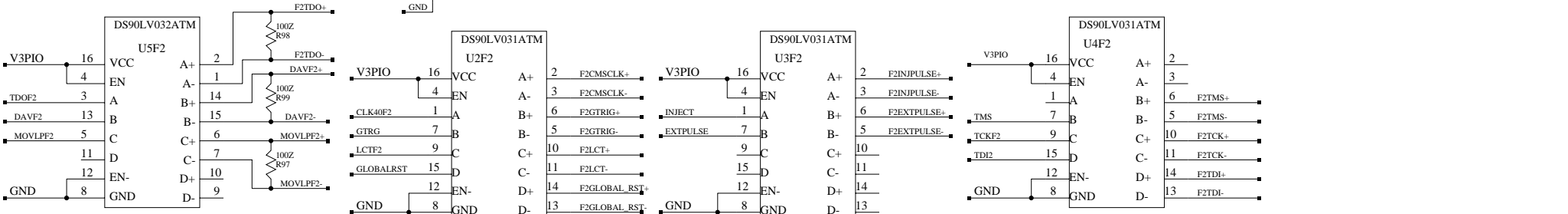
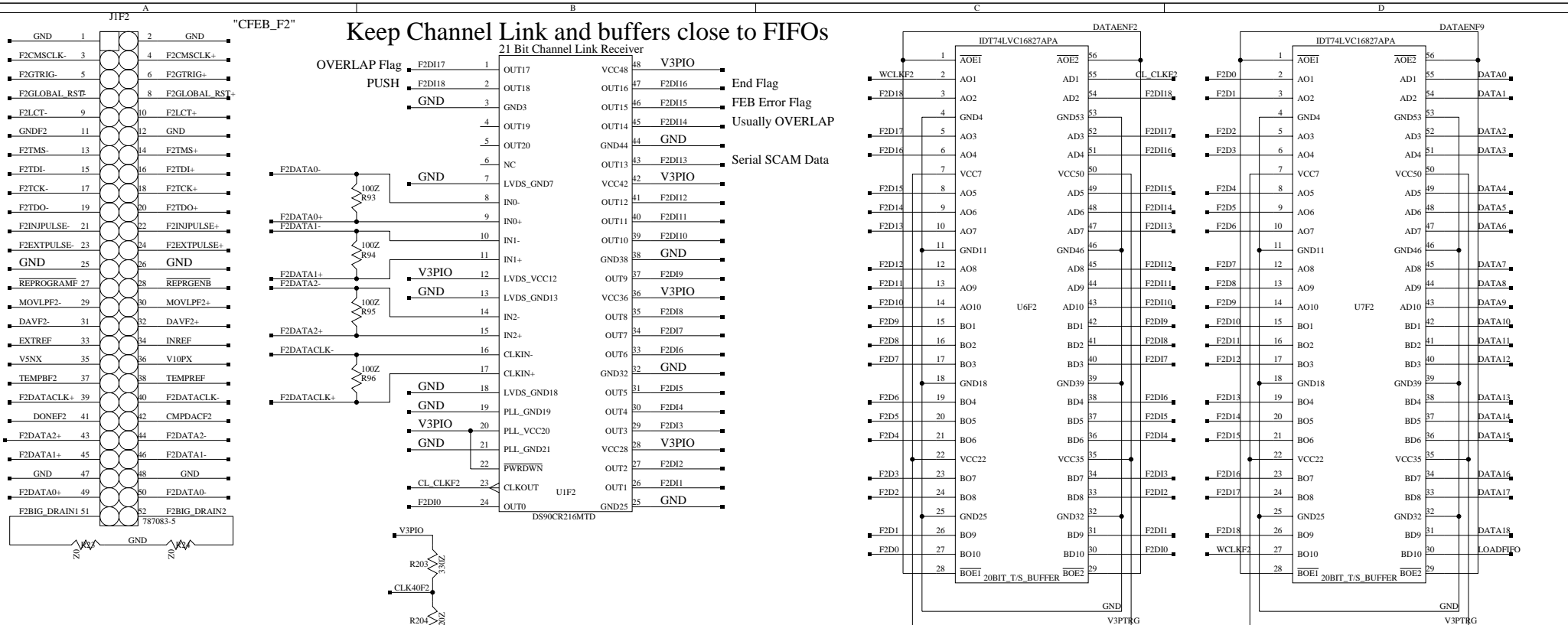


Need PULL-DOWNS on:
 Lastword, Eflag, OEN, read_one
 Need PULL-UPS on:
 Overlap, rst, f_rst, kill_dav, dav, emptyf*

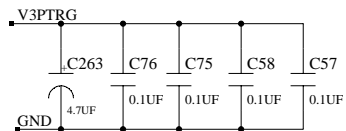
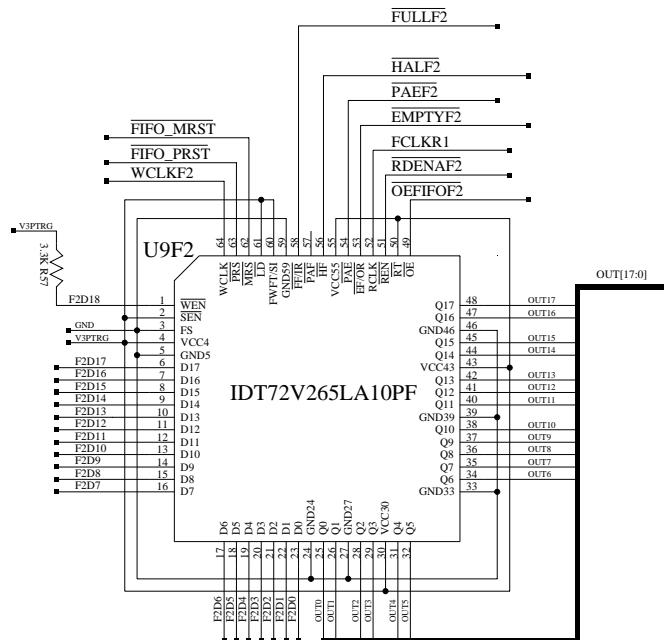


Put these terminator at the end of the trace

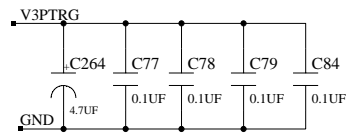
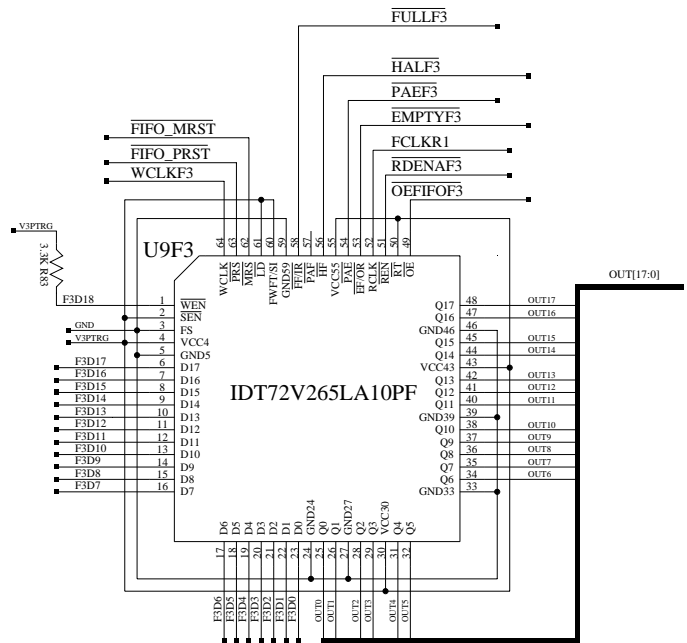




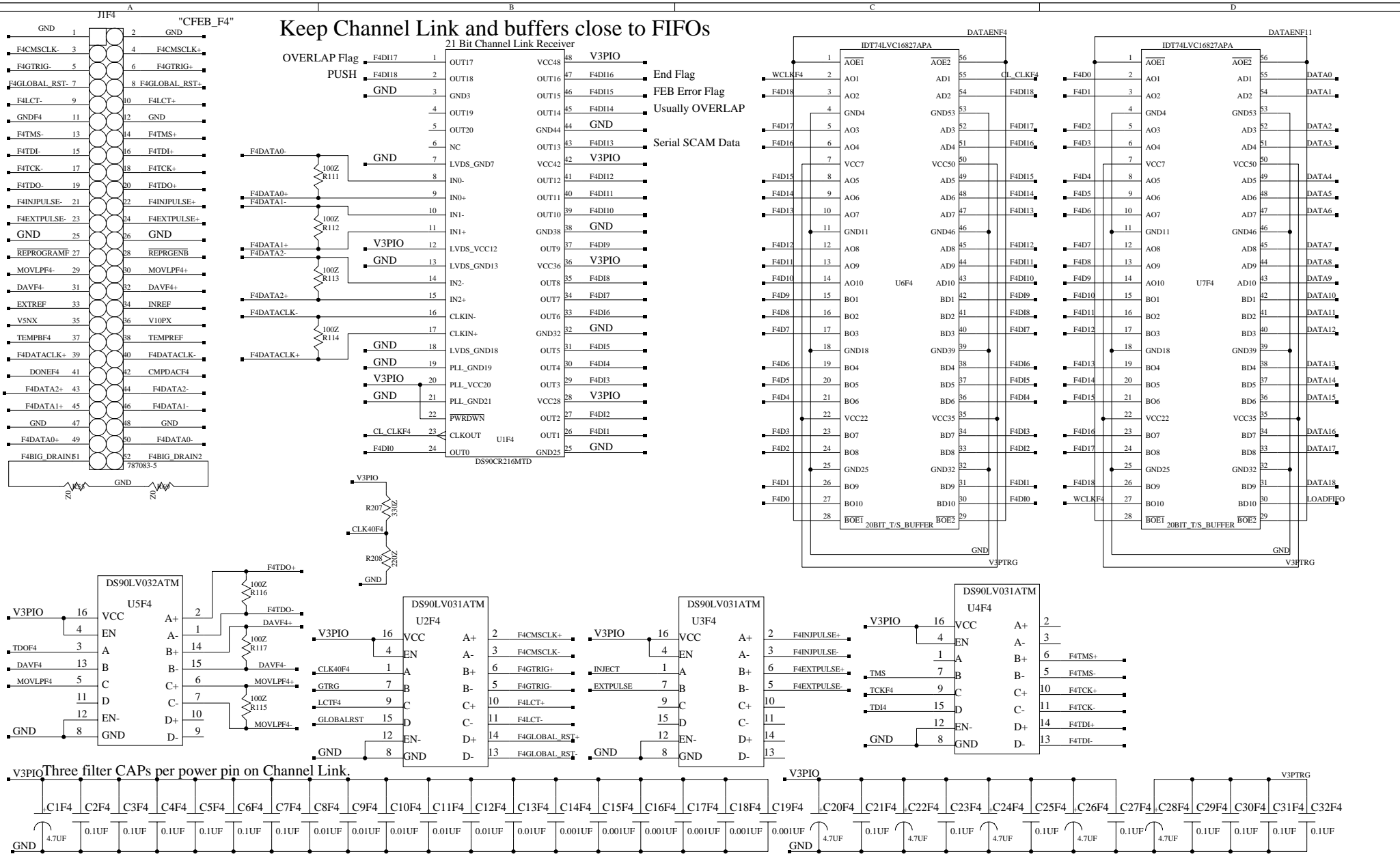
F2 Input/Output



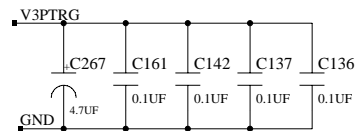
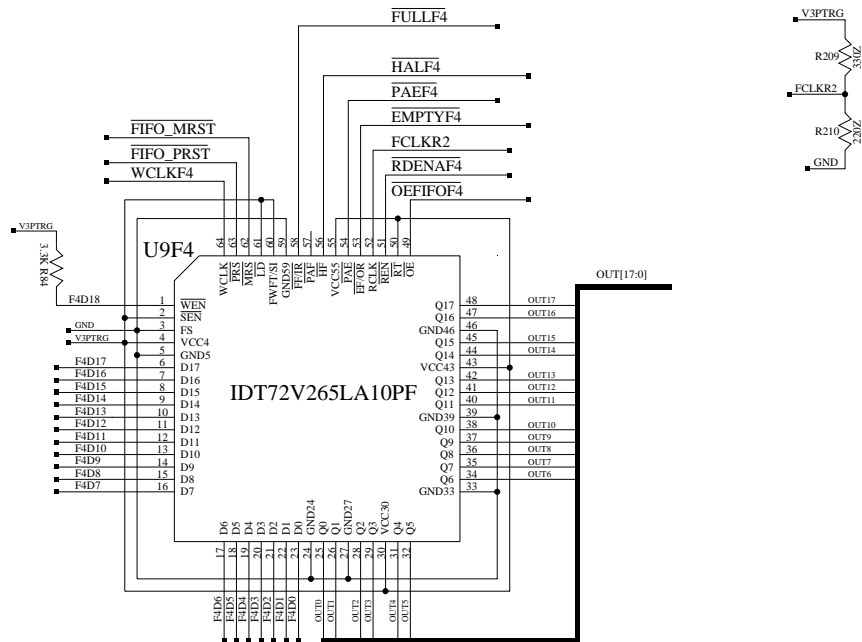
Fifo F2



Fifo F3



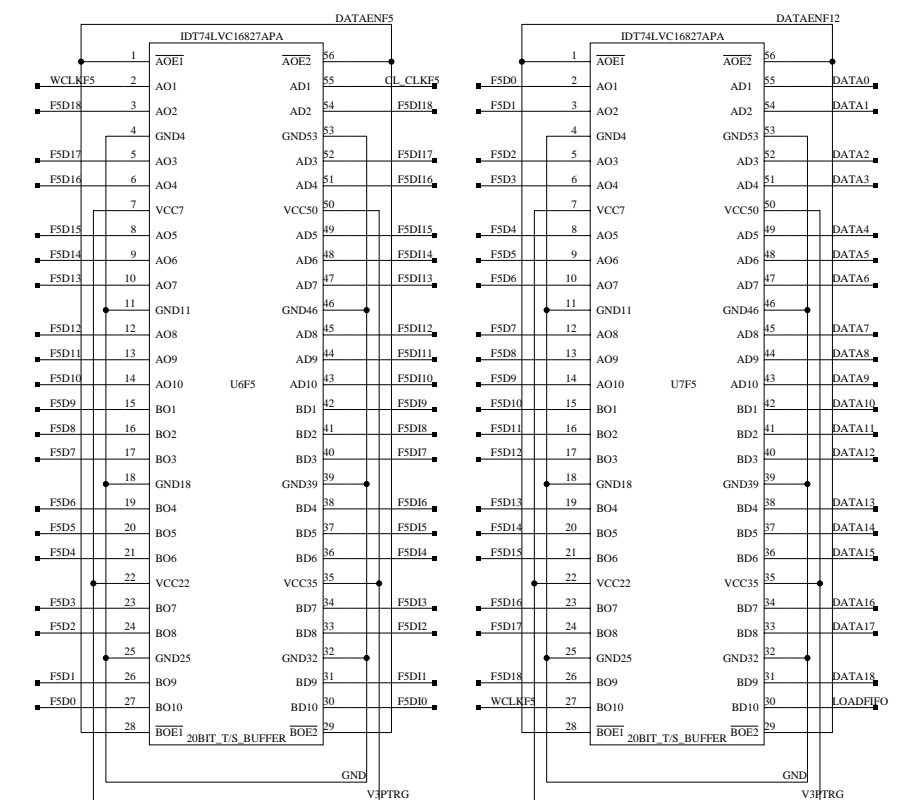
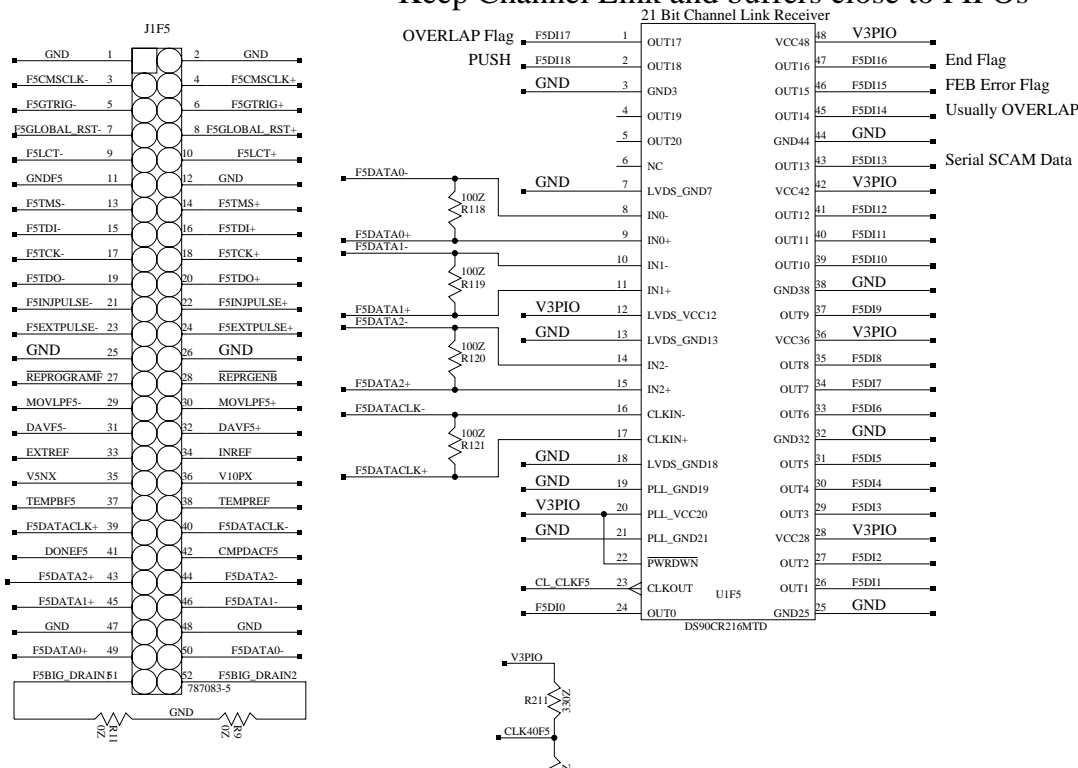
Keep Channel Link and buffers close to FIFOs

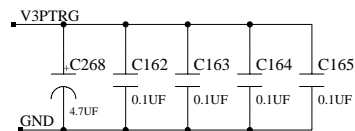
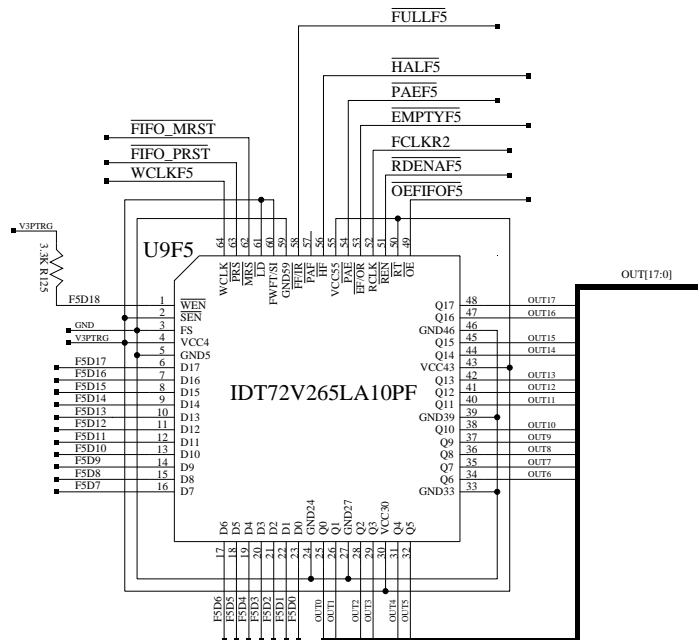


Fifo F4

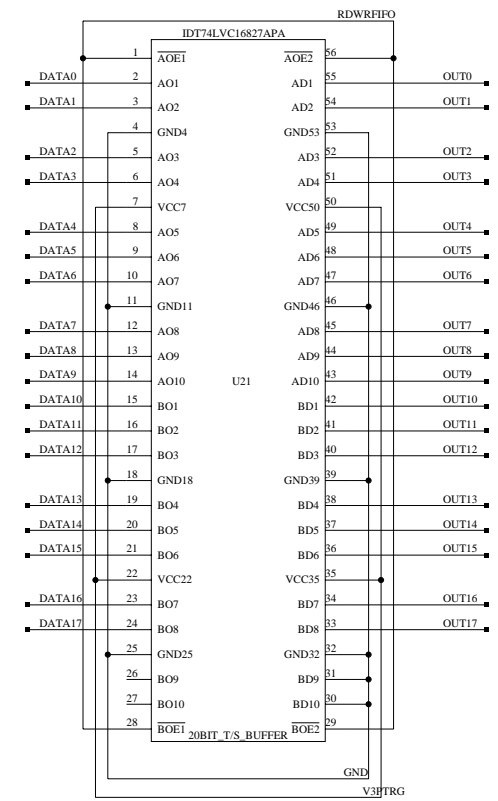
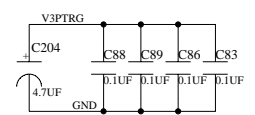
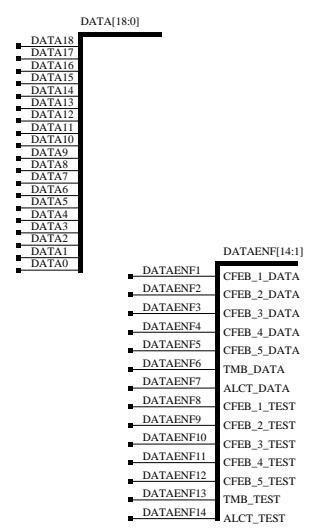
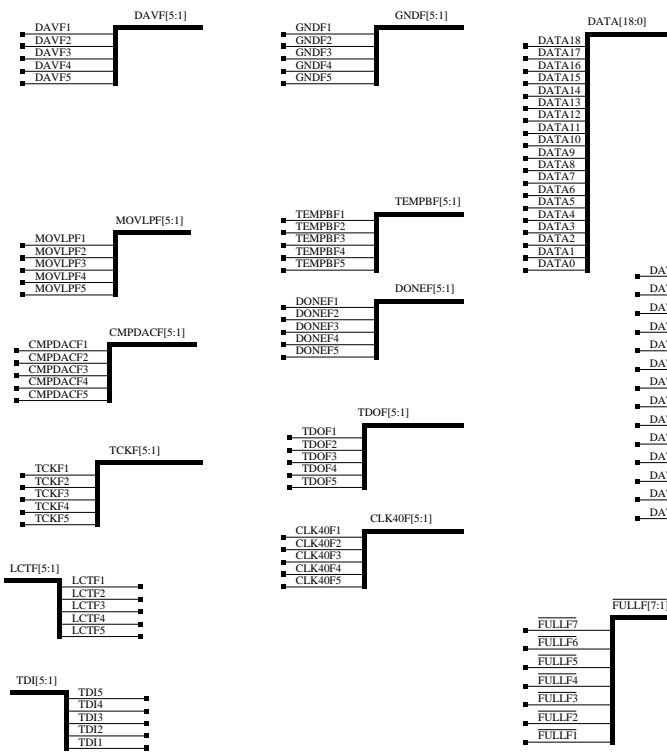
"CFEB_F5"

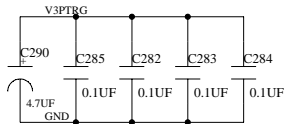
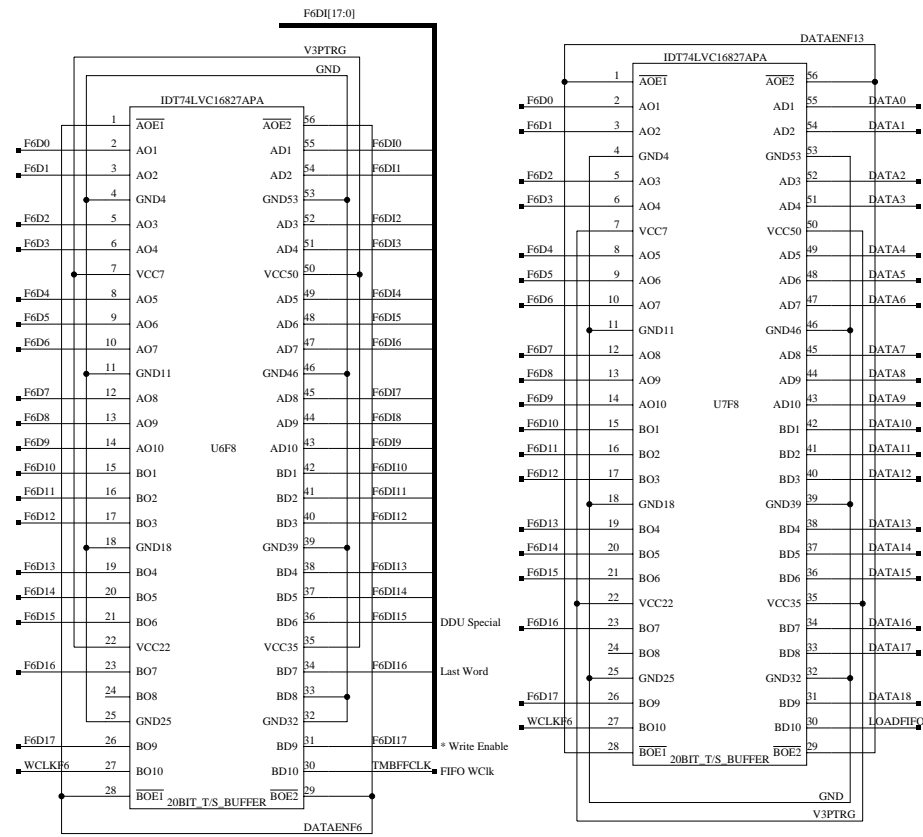
Keep Channel Link and buffers close to FIFOs



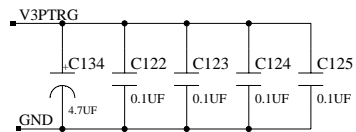
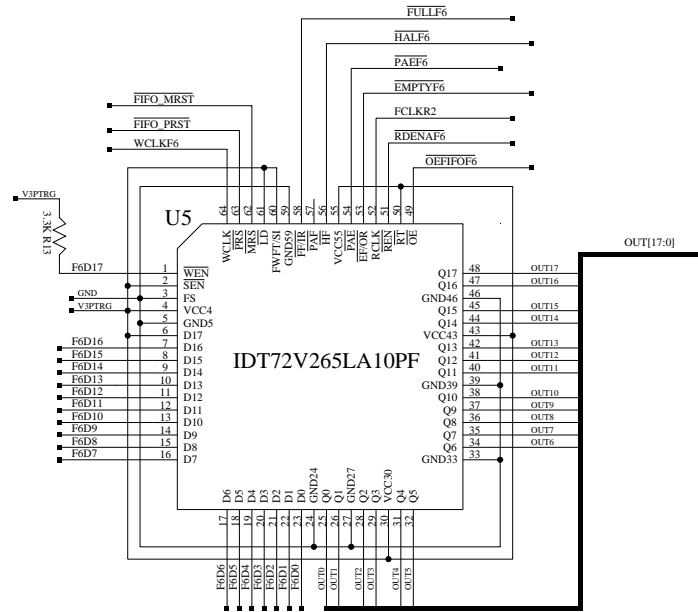


Fifo F5

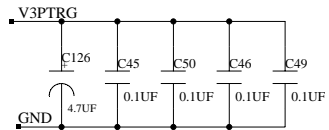




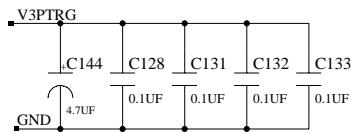
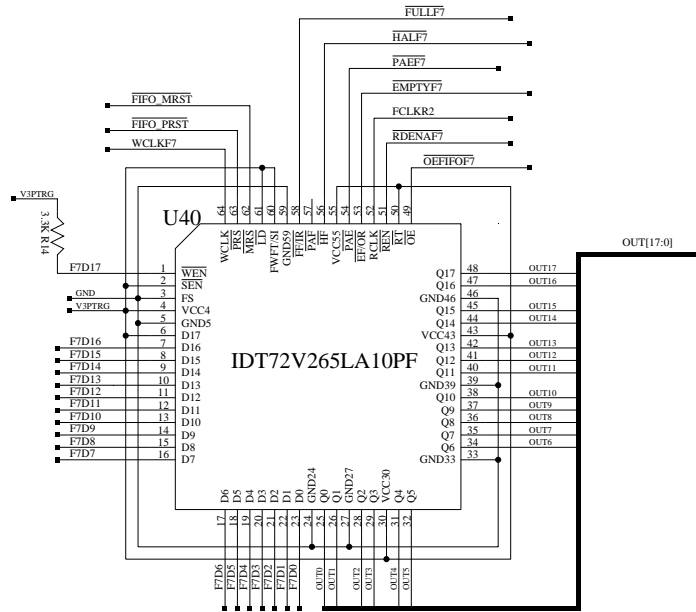
TMB Data Fifo



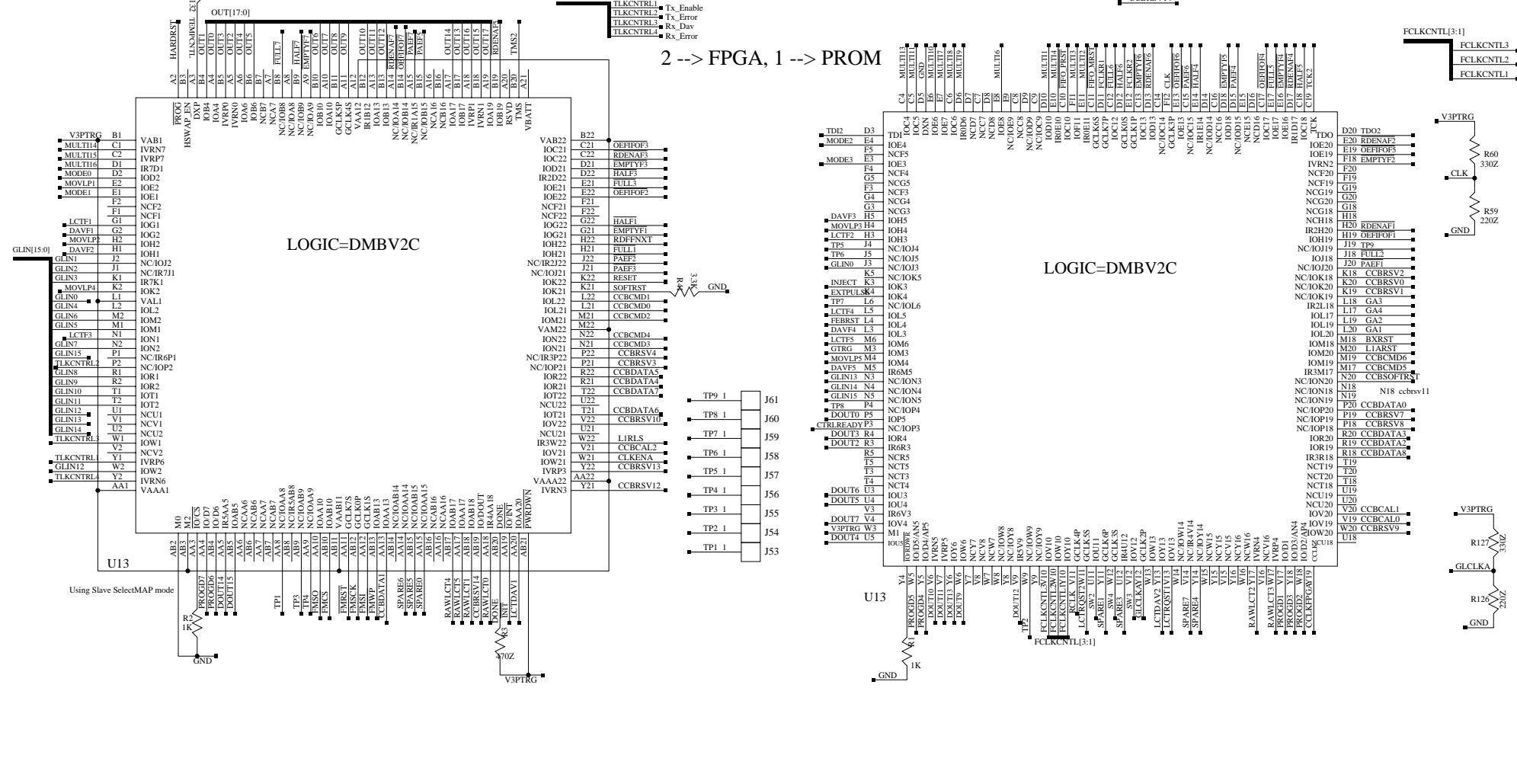
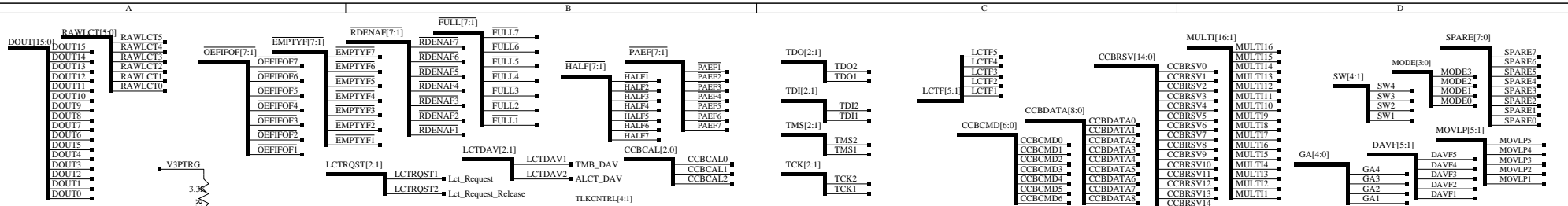
Fifo F6



ALCT Data Fifo



Fifo F7

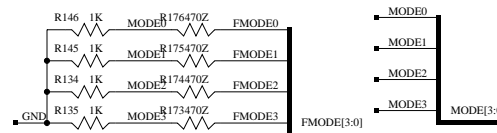
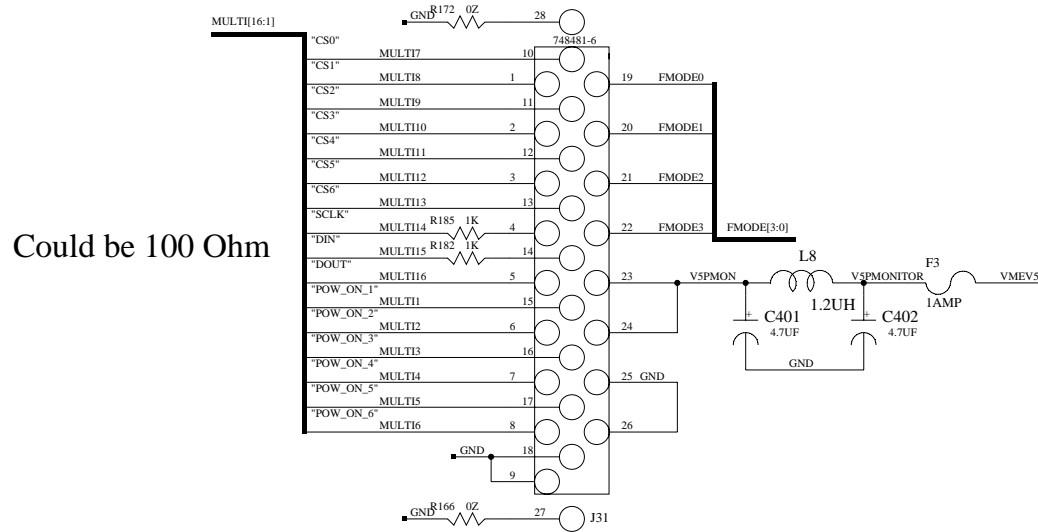


2 --> FPGA, 1 --> PROM

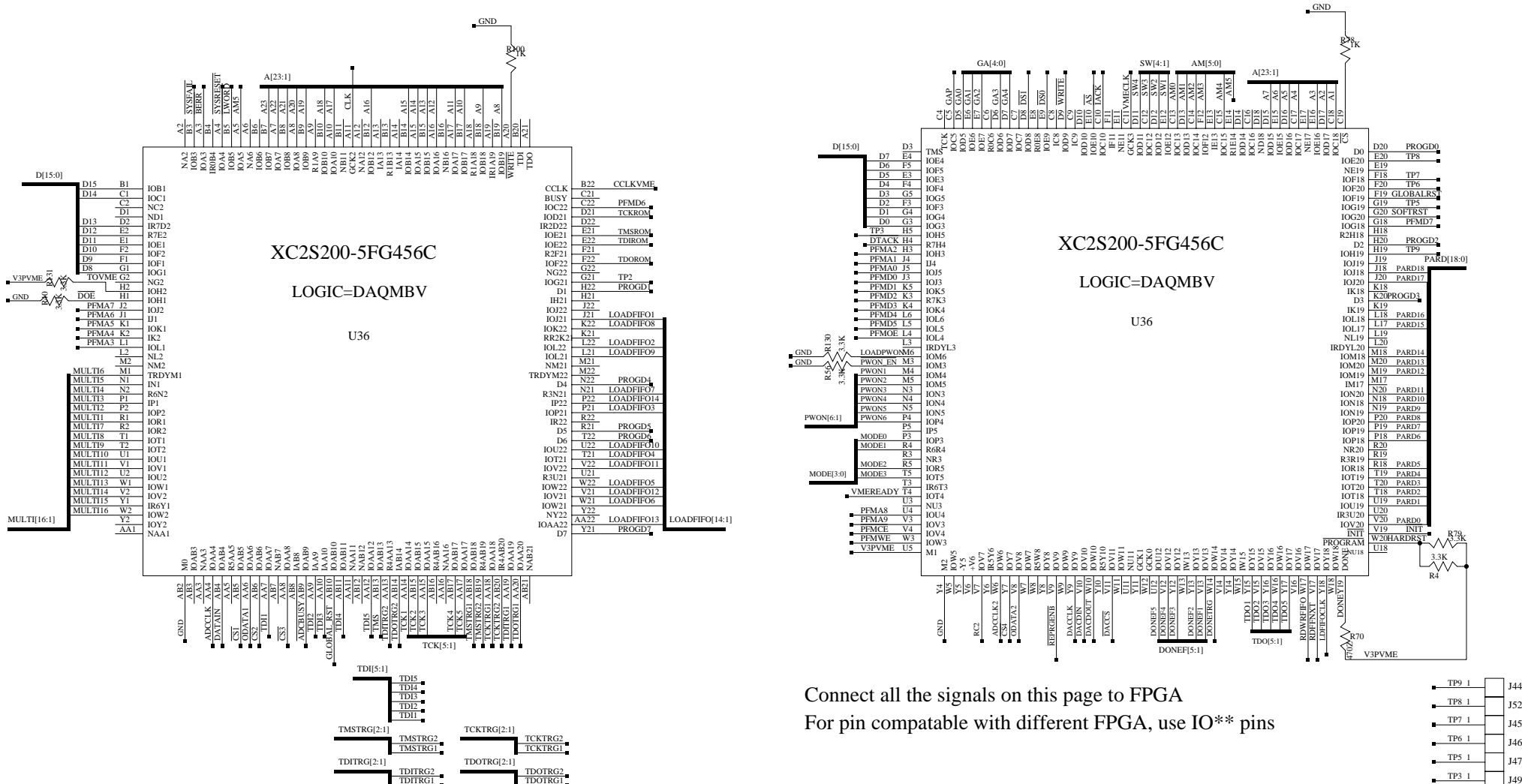
LOGIC=DMBV2C

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These are the functions if the LVDB monitor uses 6 ADC's.

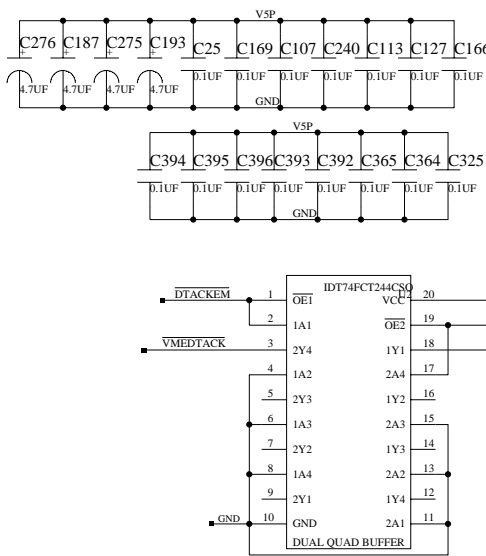
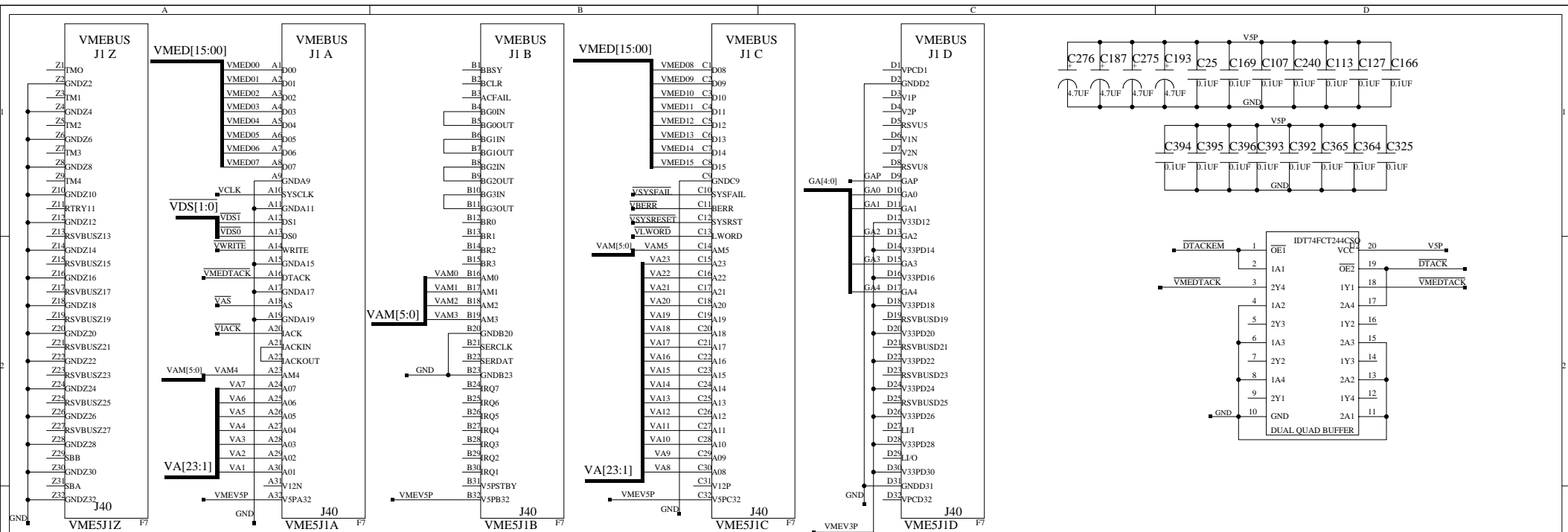


Default mode setting

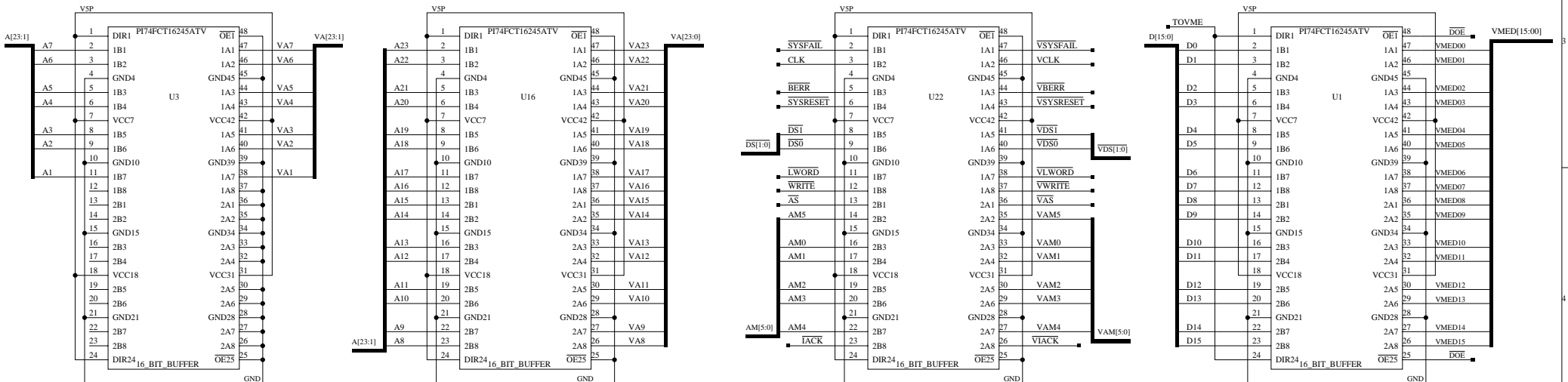


Connect all the signals on this page to FPGA
 For pin compatible with different FPGA, use IO** pins

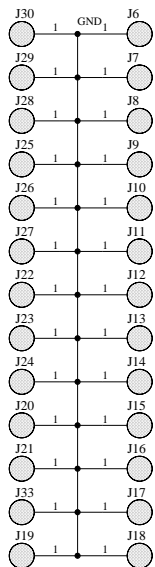
- TP9 1 J44
- TP8 1 J52
- TP7 1 J45
- TP6 1 J46
- TP5 1 J47
- TP3 1 J49
- TP2 1 J50



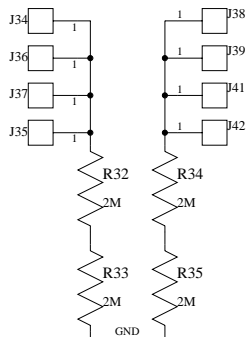
Harting PN# 02.01.160.2101



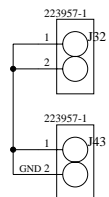
GROUND POINTS



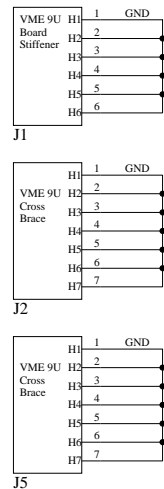
DISCHARGE UNIT



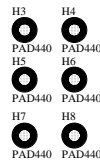
FEMALE GUIDES



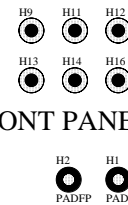
BOARD STIFFENER



MOUNTING POINTS

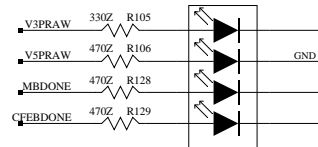


GLOBAL FIDUCIALS

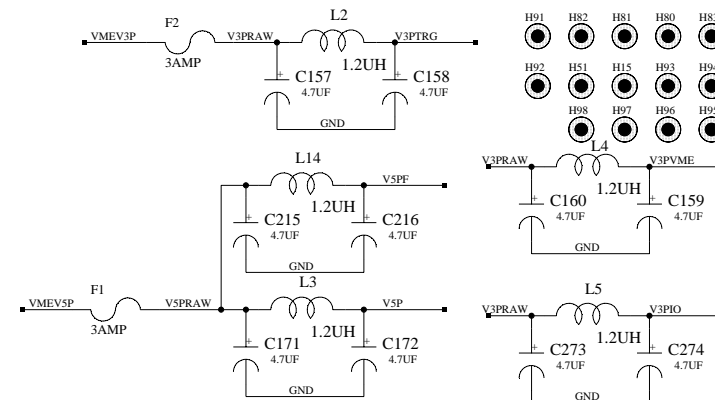
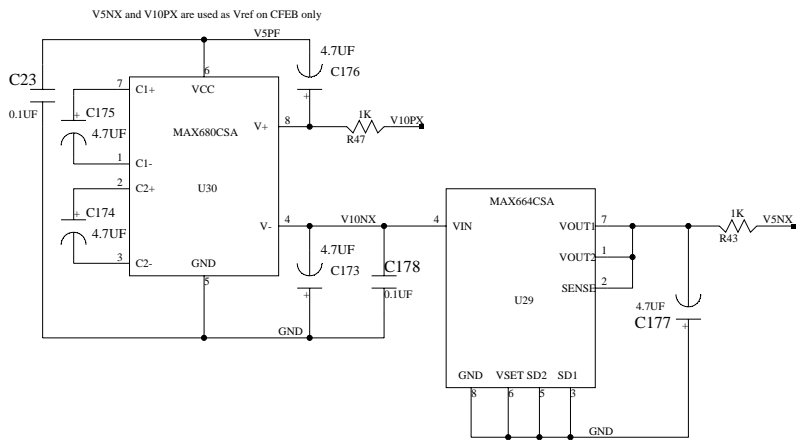
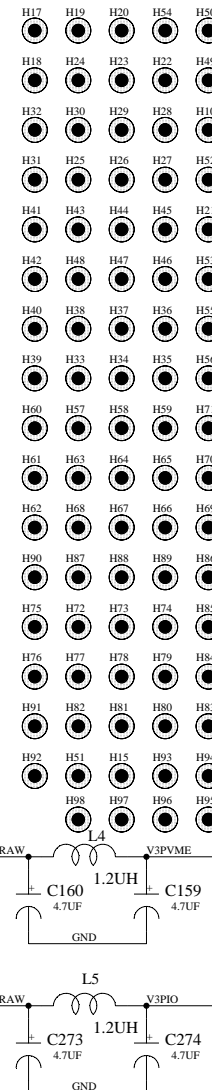


FRONT PANEL MOUNTS

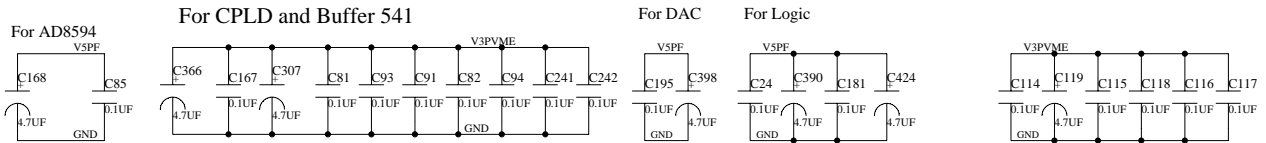
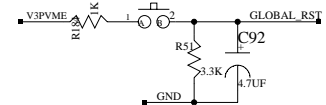
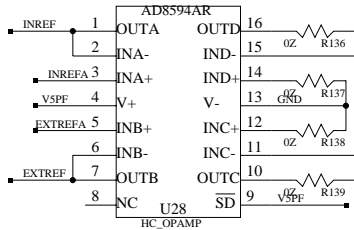
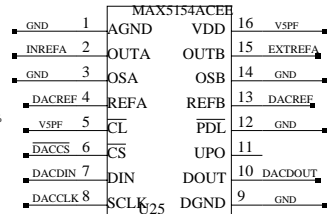
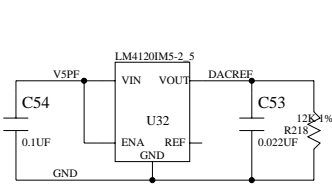
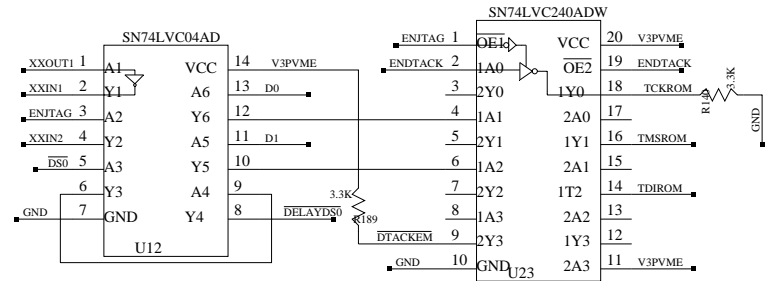
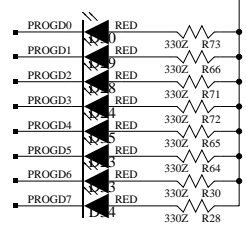
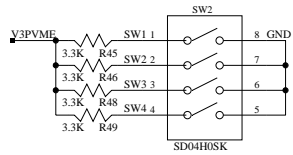
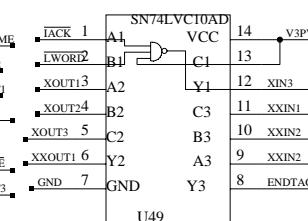
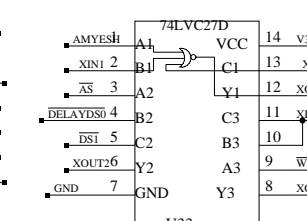
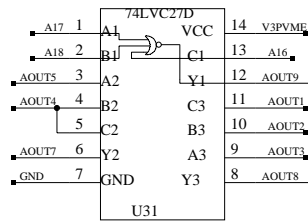
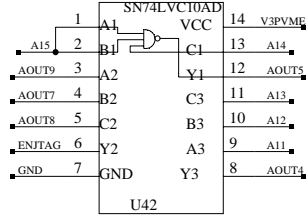
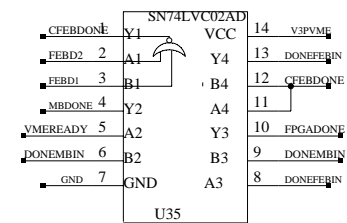
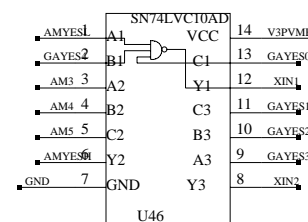
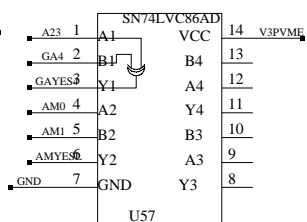
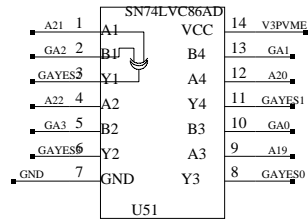
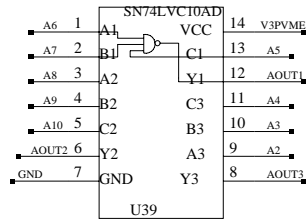
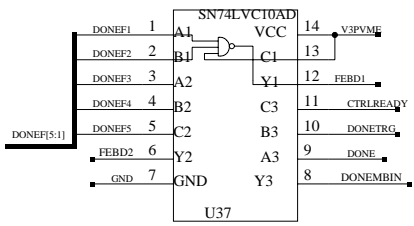
Power Monitor, Placed on front panel D10

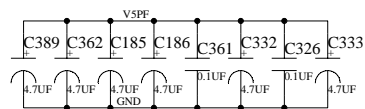
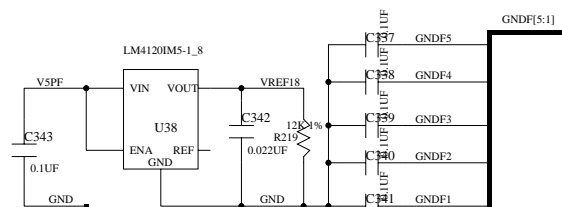
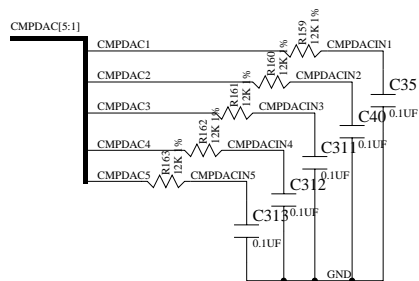
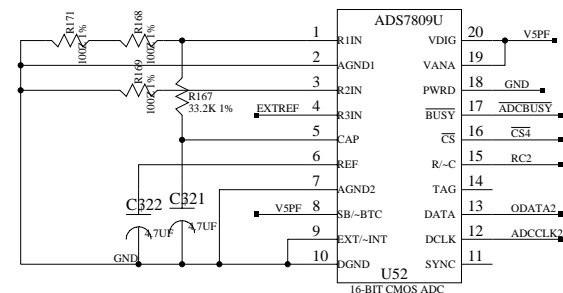
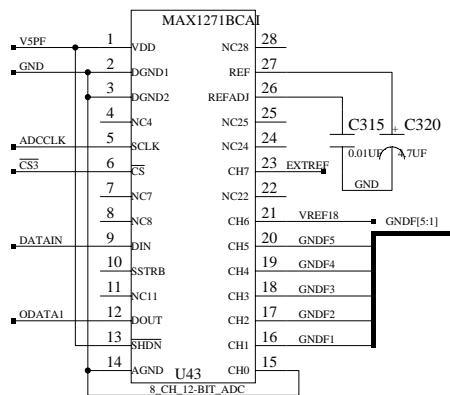
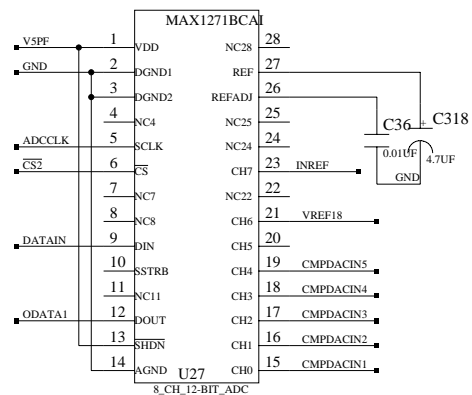
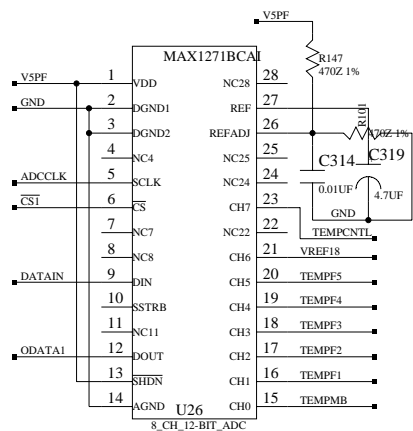
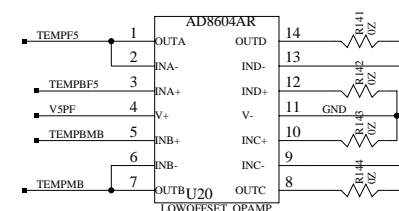
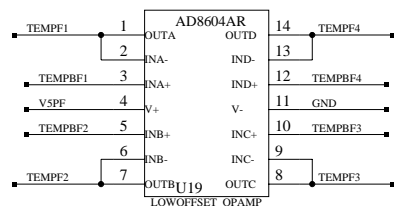
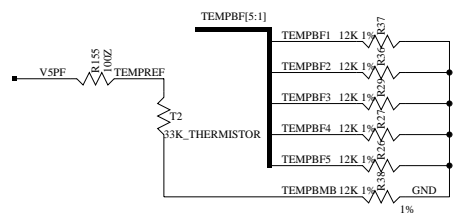


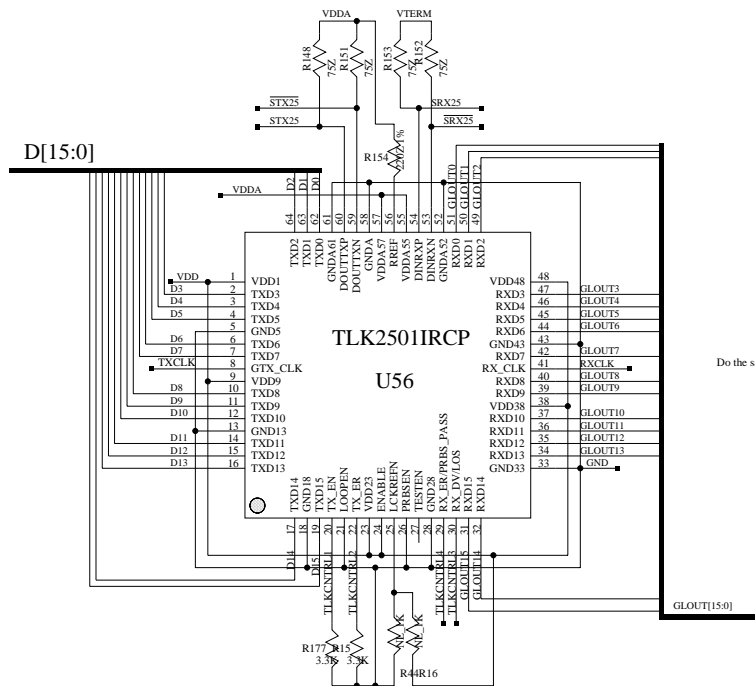
PART FIDUCIALS



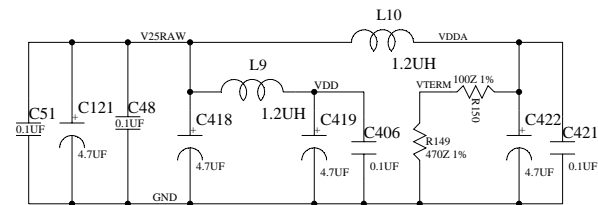
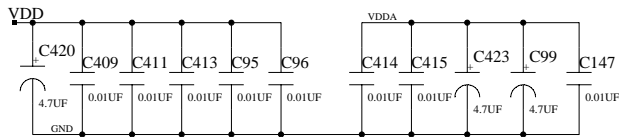
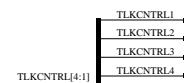
FPGA Done logic

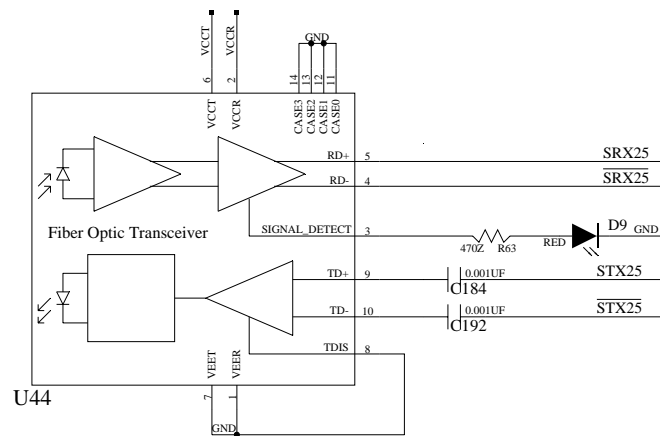
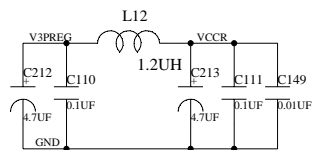
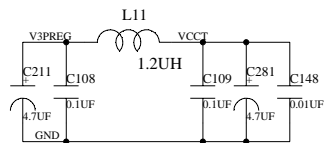
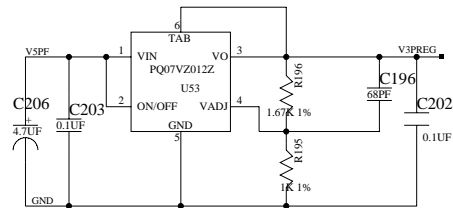




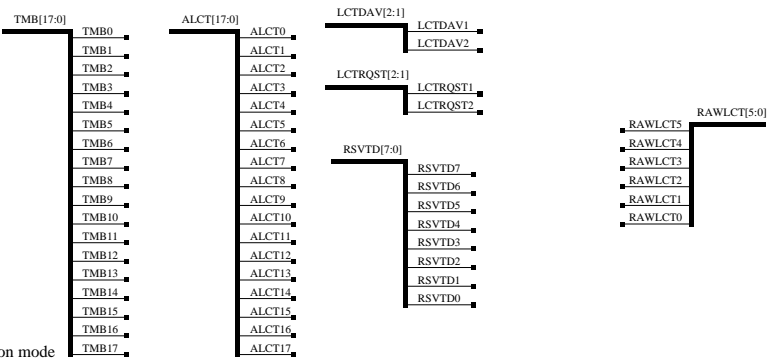
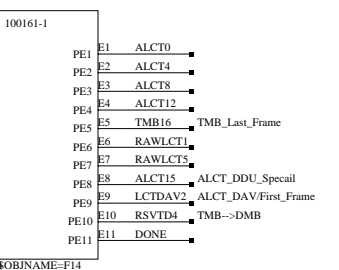
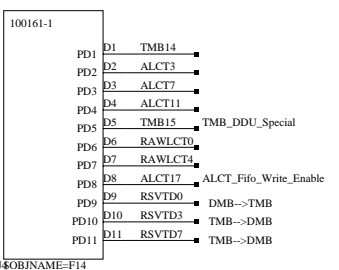
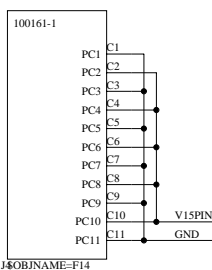
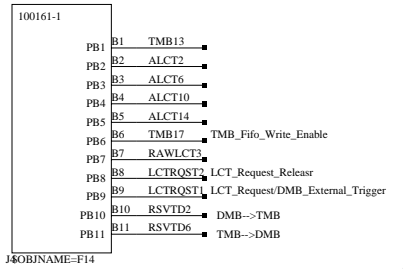
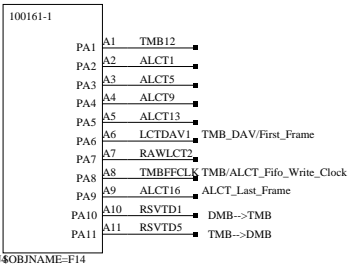
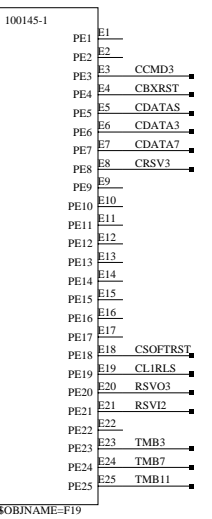
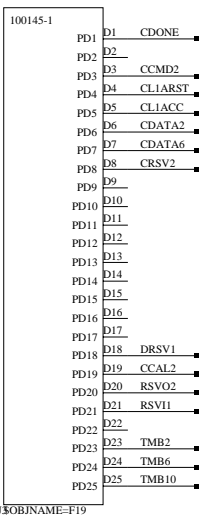
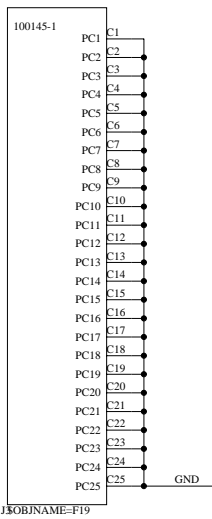
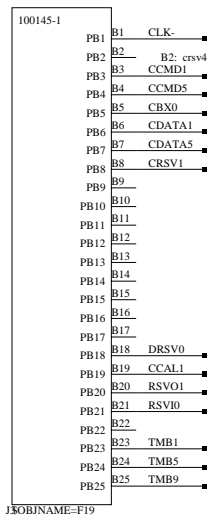
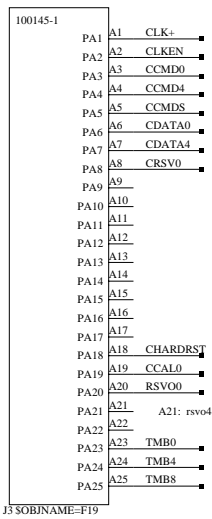


Do the same trick as before, so that one is enabled and the other is disabled.





NOTE: All high speed serial lines must be smooth, no right angles and no layer changes.



TMB[14:0]: CLCT/TMB data to 18-bit fifo
 TMB[29:15]: Additional CLCT/TMB data to 36-bit fifo
 TMB30: DDU special word flag
 TMB31: Last word flag bit
 TMB32: 40MHz clock to write to FIFO
 TMB33: Fifo write_enable inverted
 Spare[7:1]: Used to exchange infomation in CFEB calibration mode

Dan: The two parallel 100z is used to replace one 50z

