

DAQMBP

CMS CSC DAQ Motherboard PCB Schematic

REV 4

MBRD_BLK

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

DAQMB, It check and concentrate the DATA (CFEB, CLCT/TMB/ALCT) from one chamber, and then send to DDU

Oct. 23, 2000: Modify the design based on m:\wv\d741t\rev3\, an intermediary design

Nov. 1, 2000: The new scheme is ready, need update the CCB link, and CLCT/TMB link, and possibly CLCT/TMB FIFO.

Nov. 2, 2000: Preliminary design is ready. Need feedback from Dan, and coordination with UCLA, Rice and FLorida for backplane

Dec. 6, 2000: Double checked the signals by feed backs from FPGA design

Jan. 18, 2001: Modify the ADC design, use three MAX1271, and one ADS7809/AD977

Jan. 22, 2001: Modify the Backplane interface design. For CCB, use GTLP/LVTTL transceiver, TMB, use FPGA GTLP property

Feb. 7, 2001: Modify according to backplane PCB design, Add Flash ram

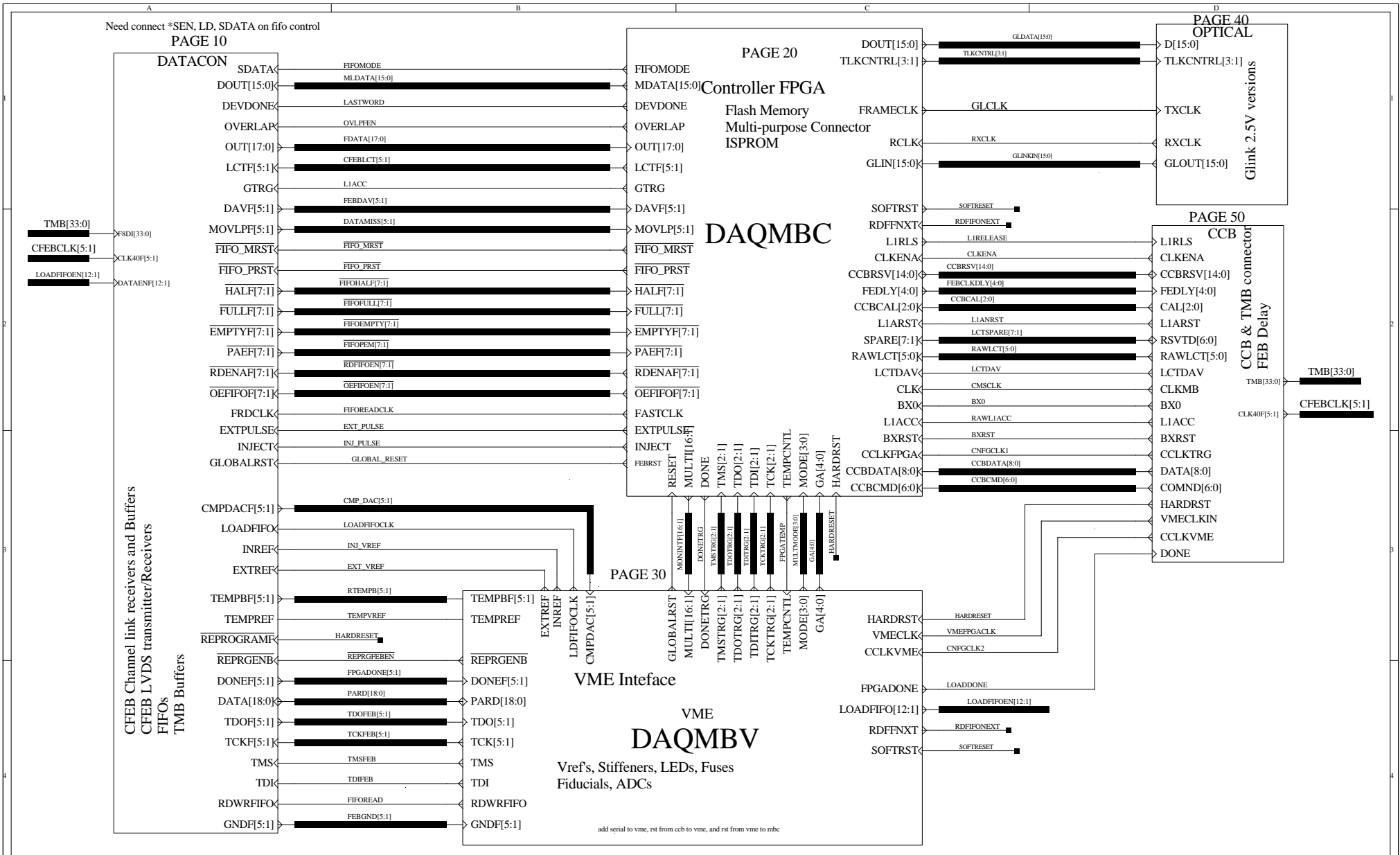
Feb. 14, 2001: Double check, and modify the VME interface and "emergency" handling

Feb. 26, 2001: Further check, Changed the DAC to MAX5154

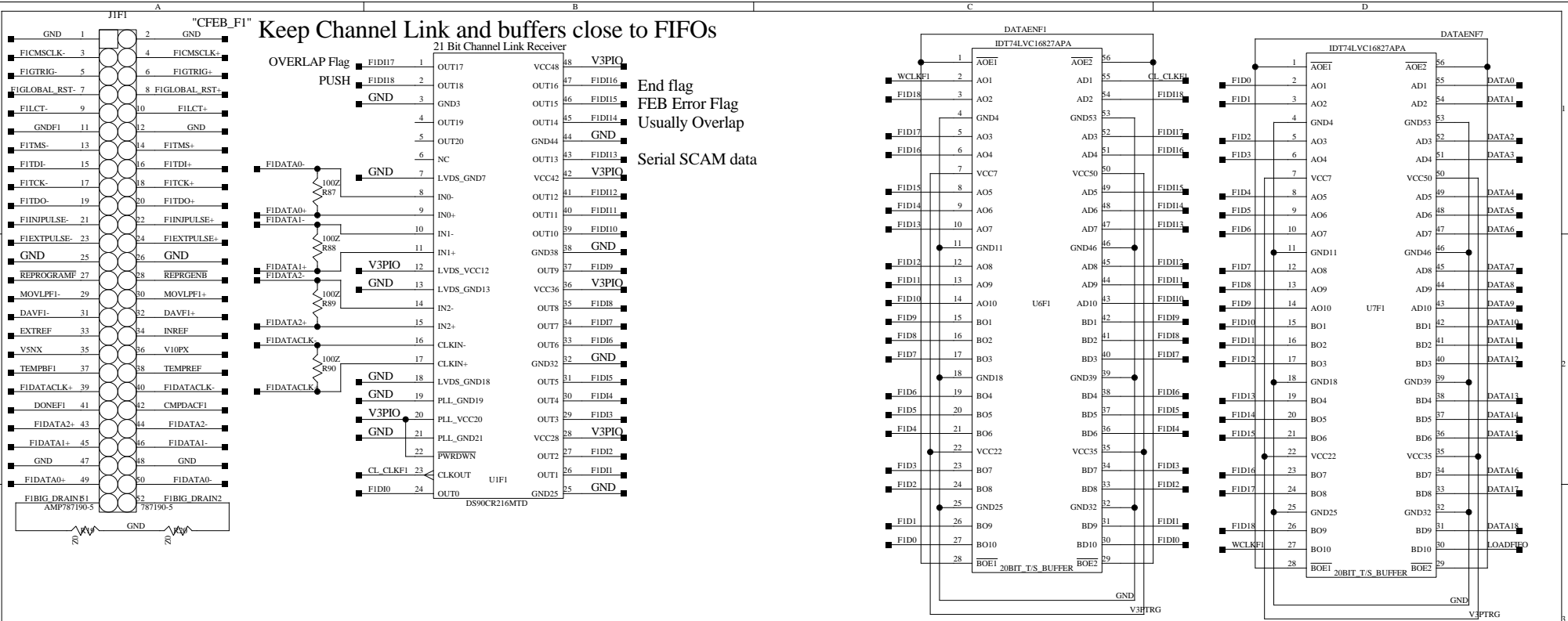
Mar. 5, 2001: Add TLK2501/1501 for GLINK, and Changed the Temprature ADC Refs

July 3, 2001: Modifications by the Rev3 PCB debug

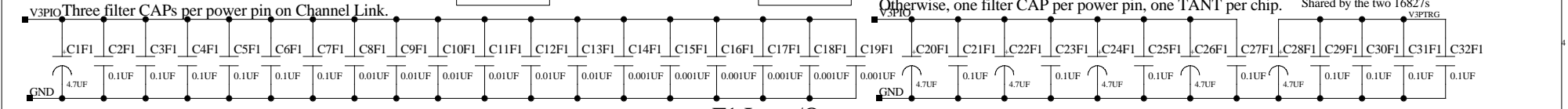
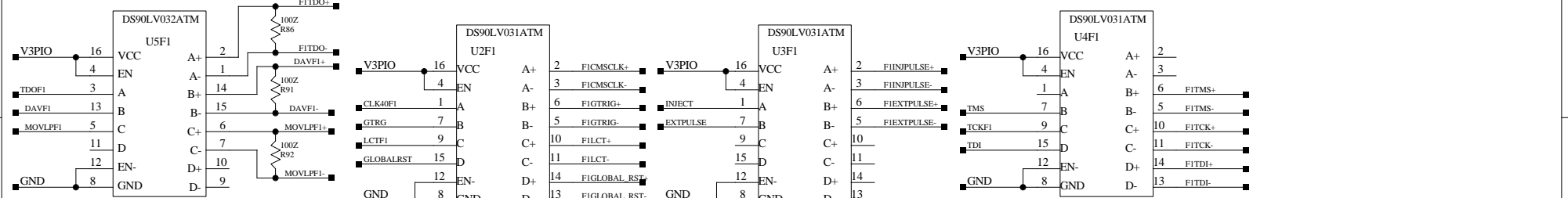
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"CFEB_F1" Keep Channel Link and buffers close to FIFOs



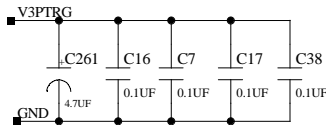
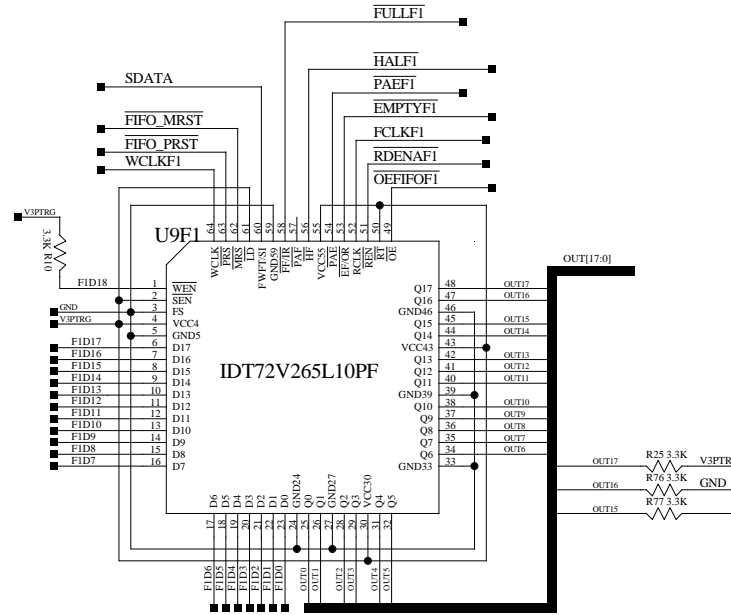
OVERLAP Flag
 PUSH
 End flag
 FEB Error Flag
 Usually Overlap
 Serial SCAM data



F1 Input/Output

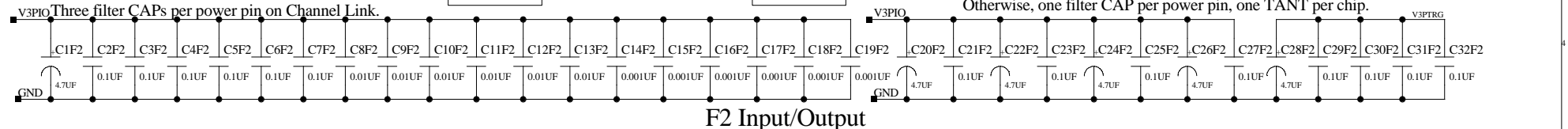
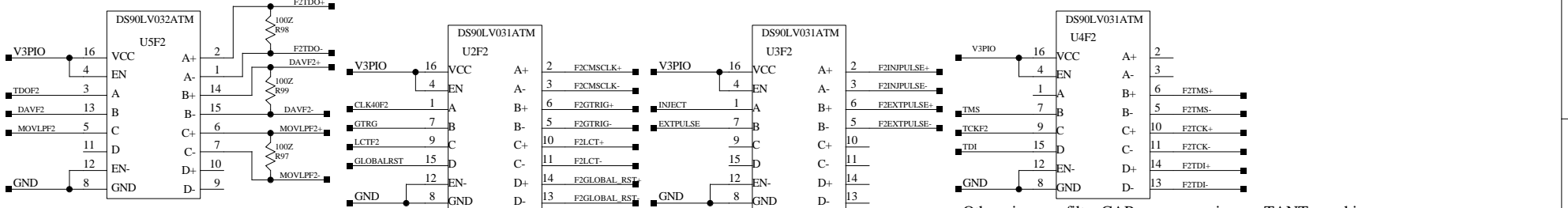
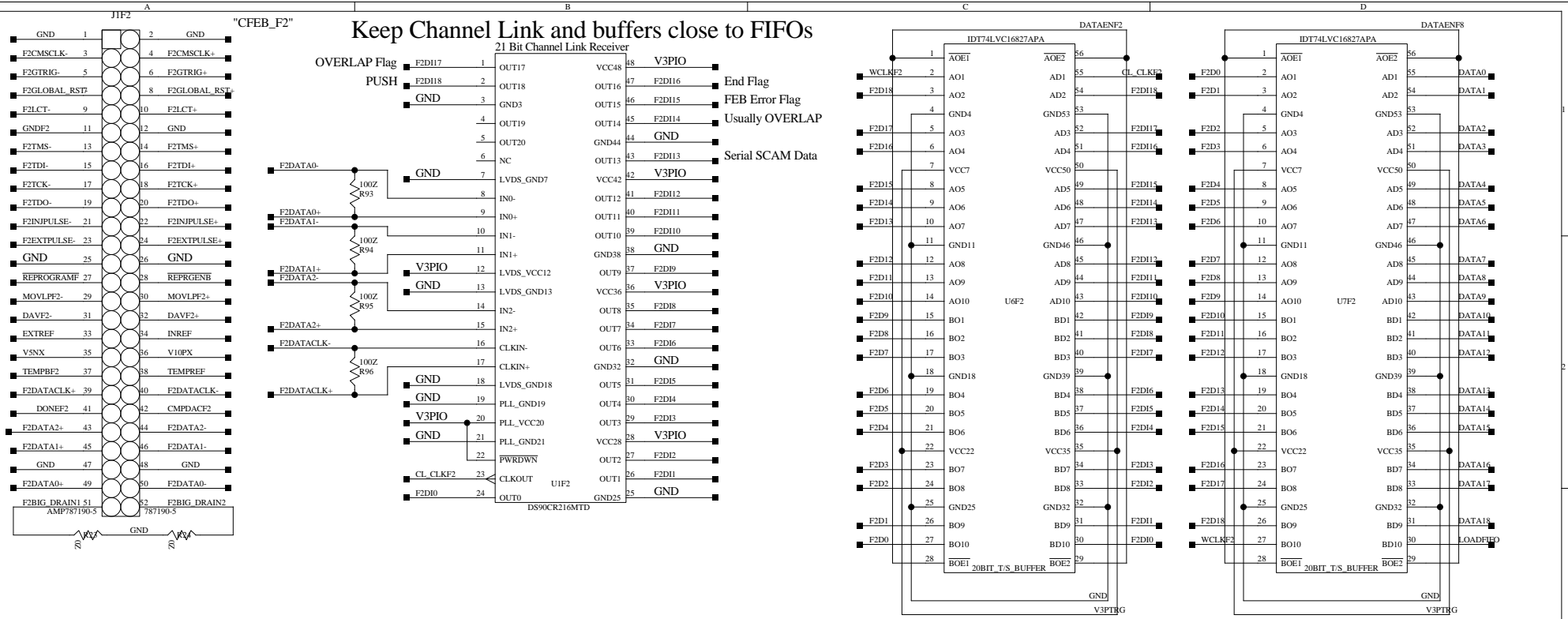
Disable all FIFOs for ~50ns during readout switching?
 Set FWFT mode: Sdata HIGH during falling edge of MRST.

Need PULL-DOWNS on:
 Lastword, Eflag, OEN, read_one
 Need PULL-UPS on:
 Overlap, rst, f_rst, kill_dav, dav, emptyf*

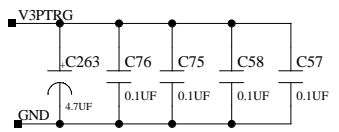
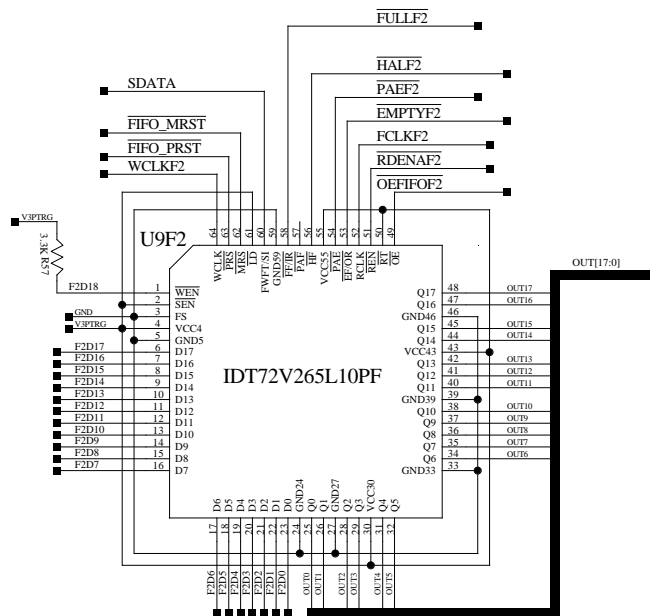


Fifo F1

Keep Channel Link and buffers close to FIFOs



F2 Input/Output



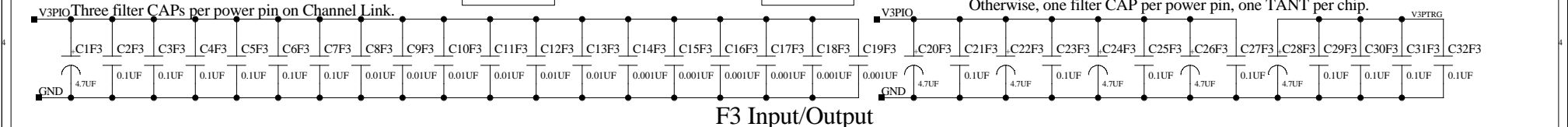
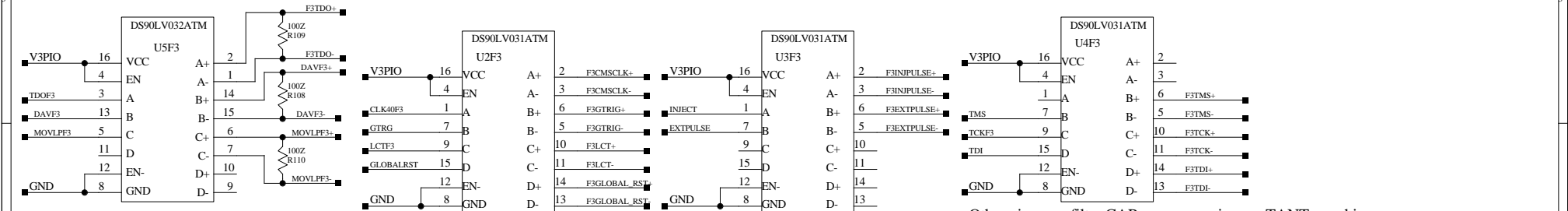
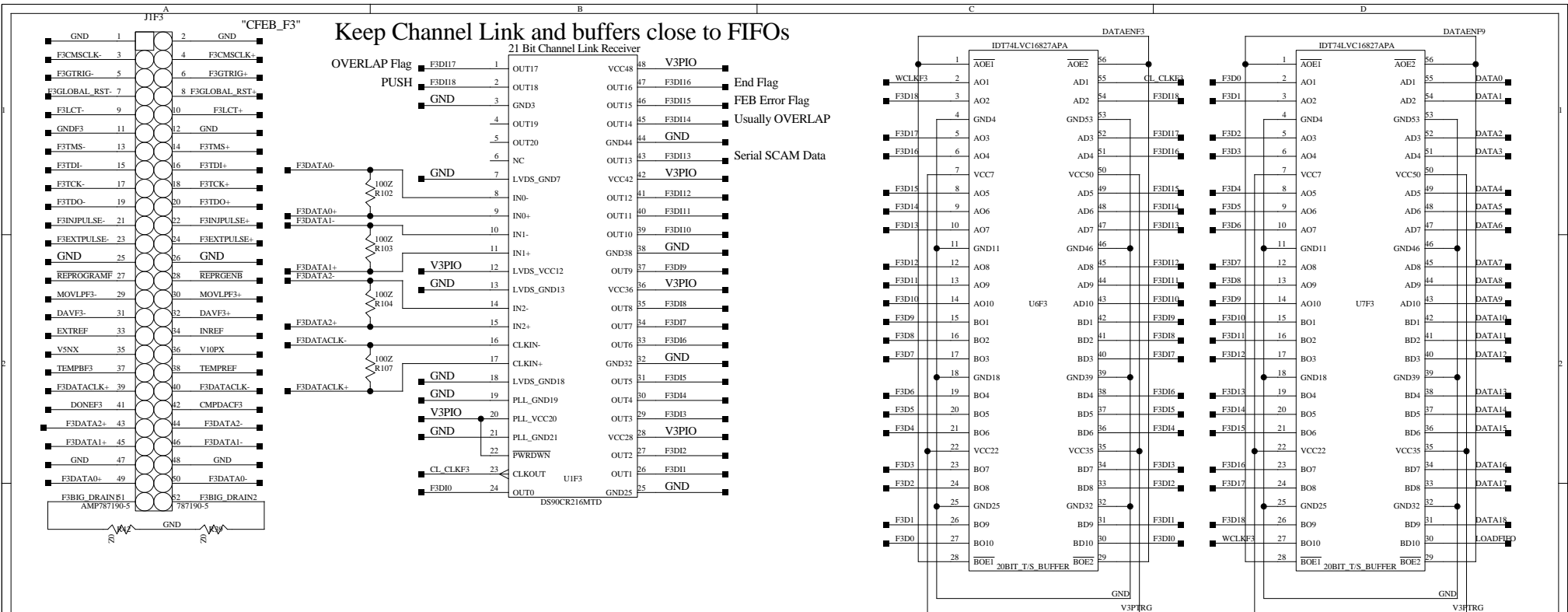
Fifo F2

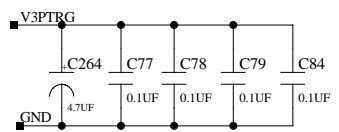
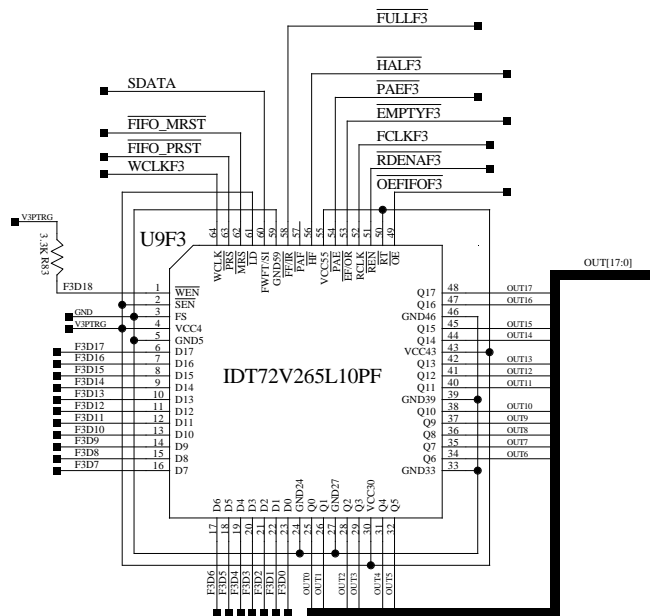
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TITLE FEB2 Fifo
 CMS CSC DAQ MOTHERBOARD
 CMS CSC ELECTRONICS

BY G PARENT PAGE 1
 DATE 7-3-2001_16:20

PROJECT DAQMBP
 FILE DATACON . 4 PAGE 10C





Fifo F3

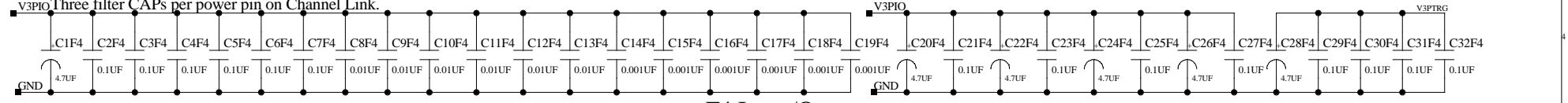
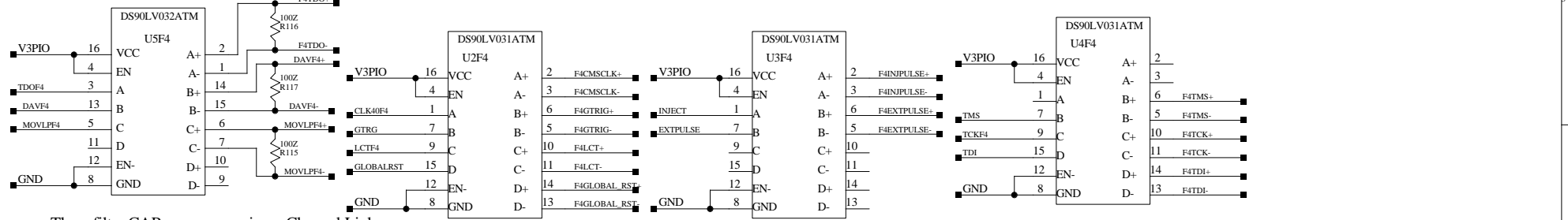
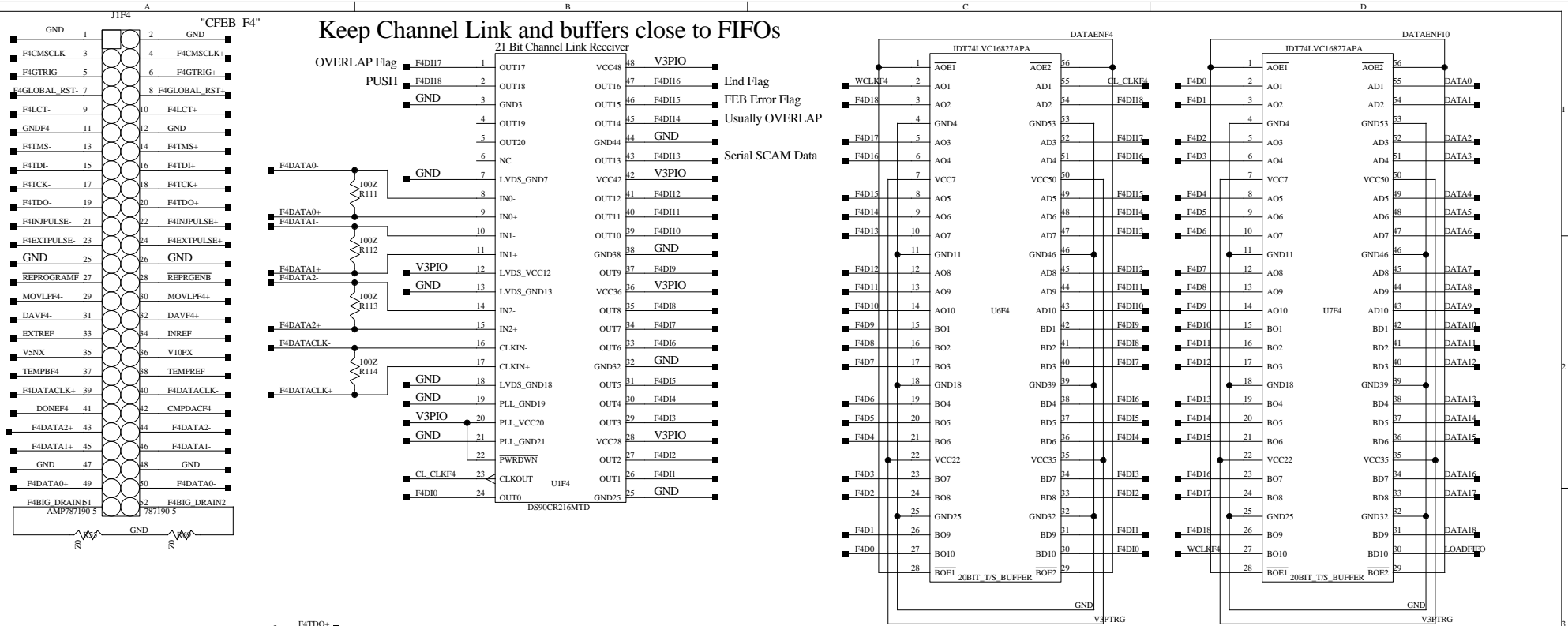
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TITLE FEB3 Fifo
 CMS CSC DAQ MOTHERBOARD
 CMS CSC ELECTRONICS

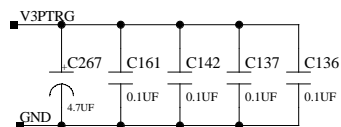
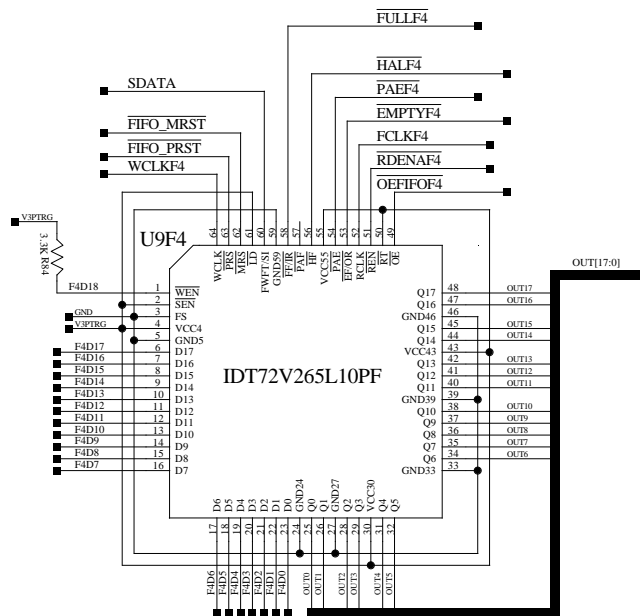
BY G PARENT PAGE 1
 DATE 7-3-2001_16:20

PROJECT DAQMBP
 FILE DATACON . 6 PAGE 10E

Keep Channel Link and buffers close to FIFOs



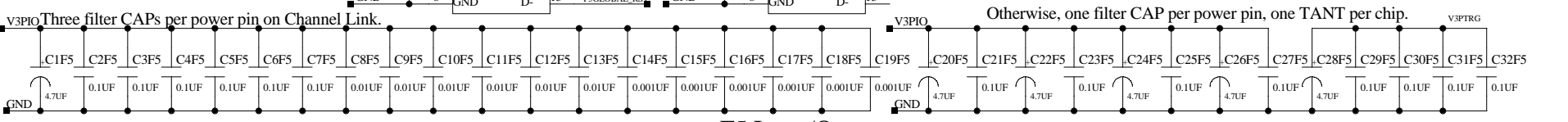
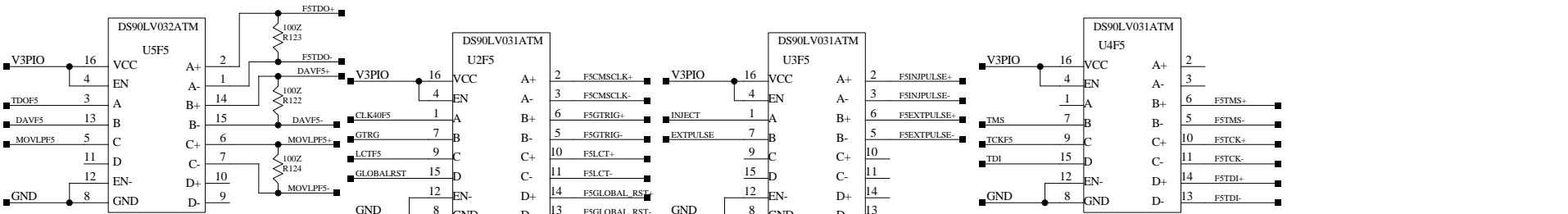
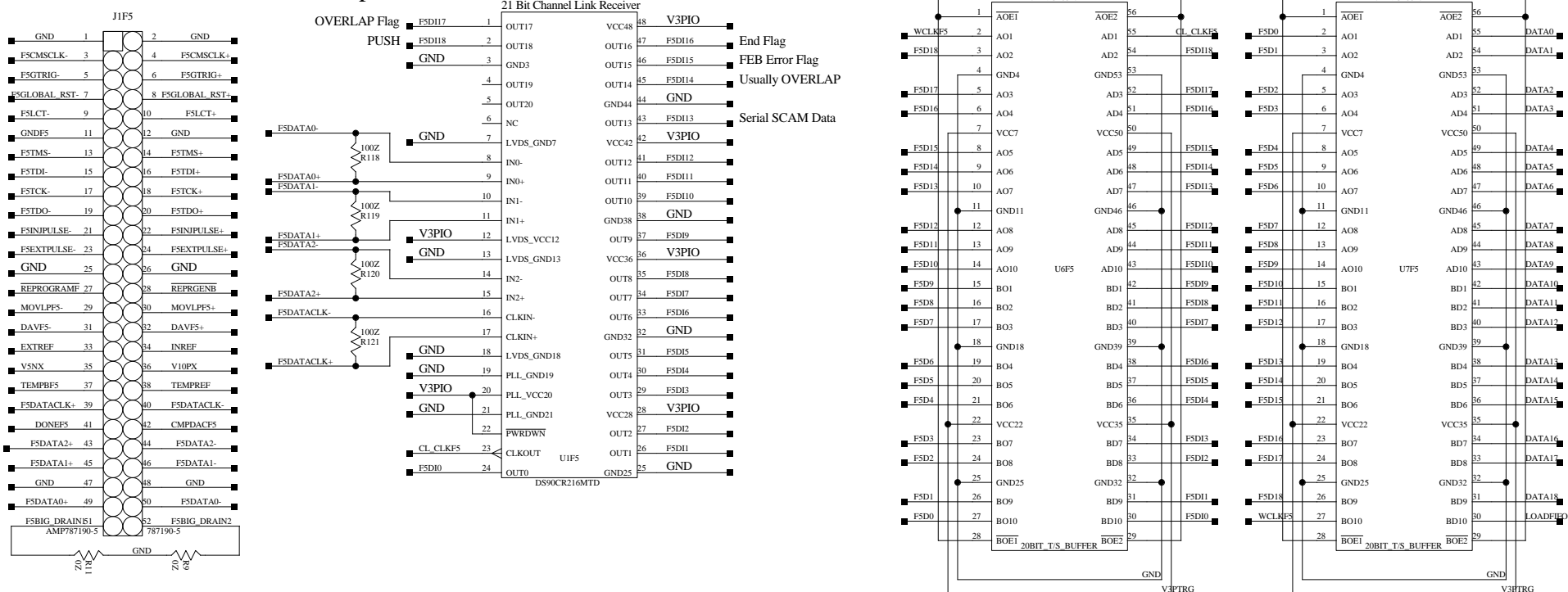
F4 Input/Output



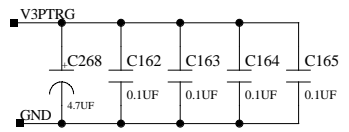
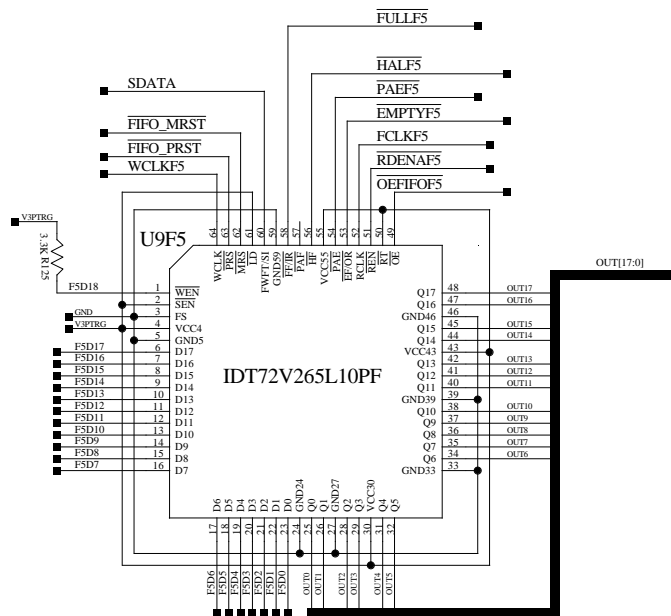
Fifo F4

"CFEB_F5"

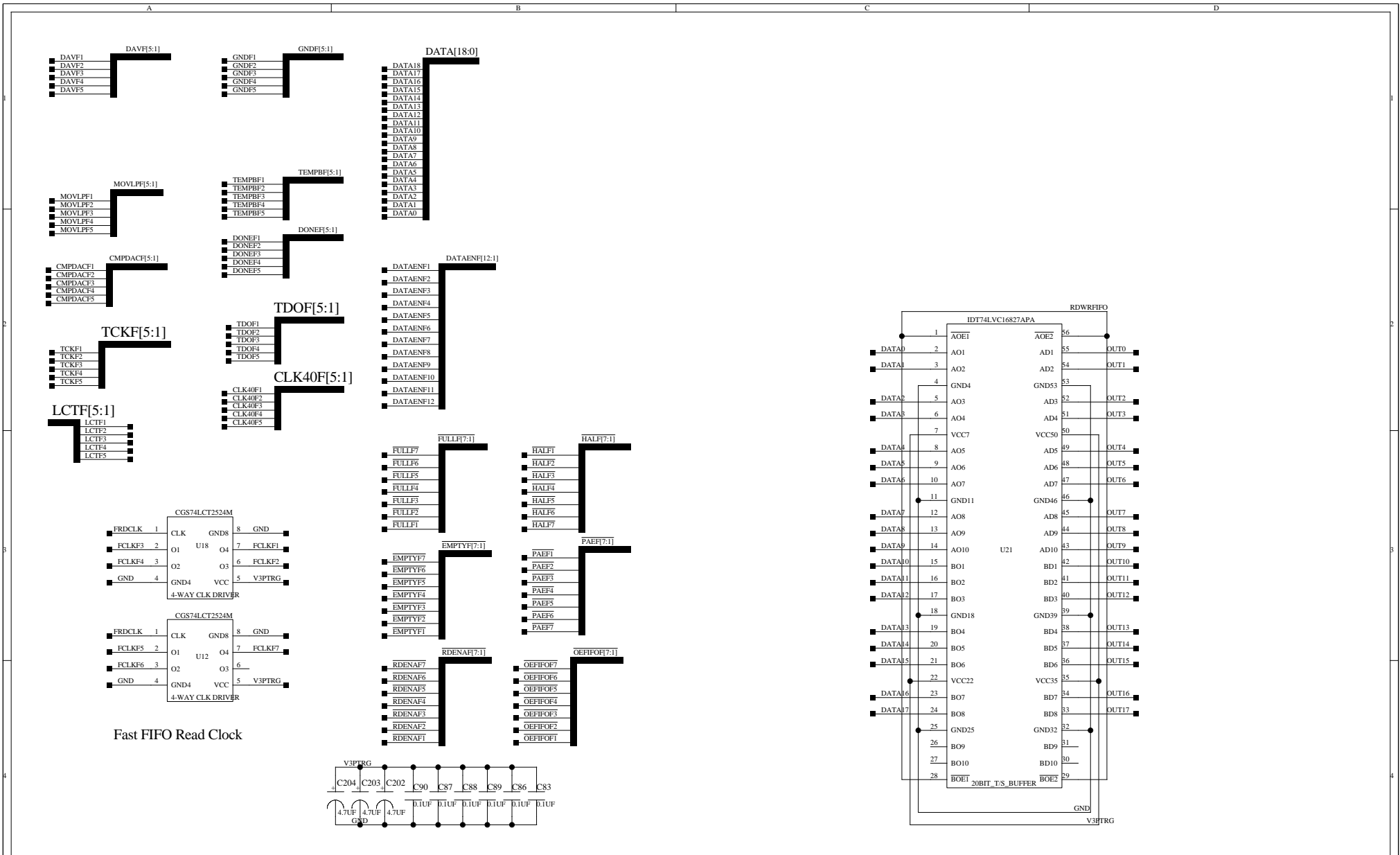
Keep Channel Link and buffers close to FIFOs



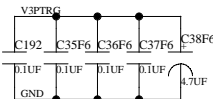
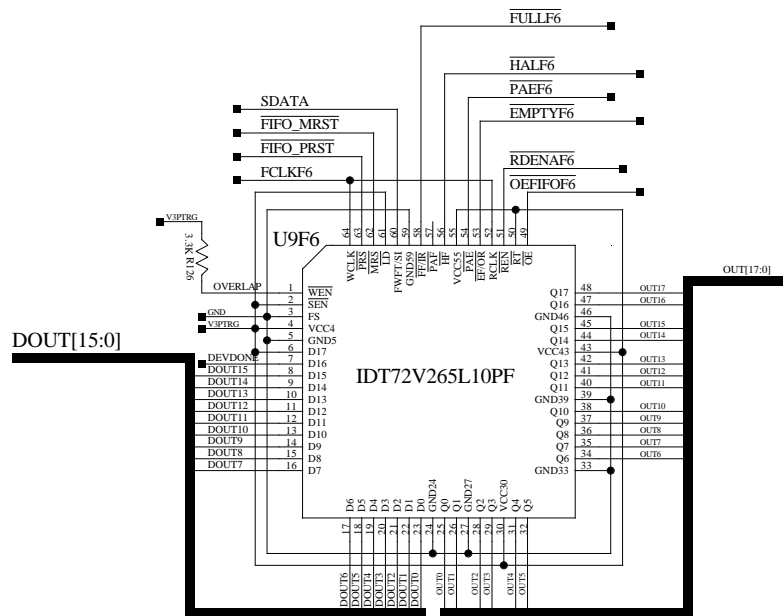
F5 Input/Output



Fifo F5



Fast FIFO Read Clock



Overlap Fifo F6

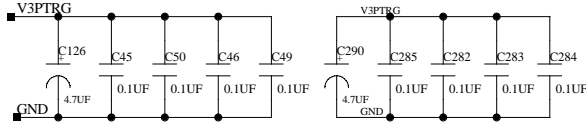
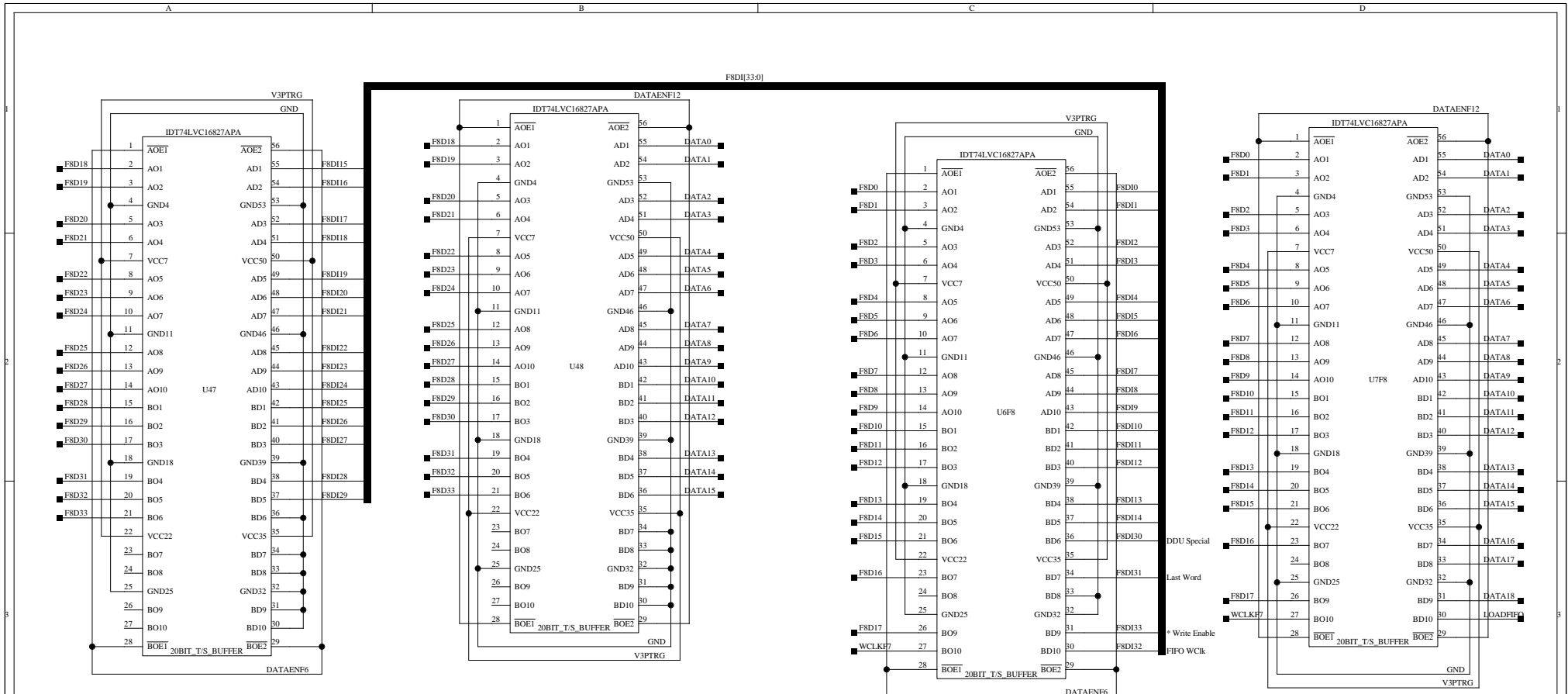
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TITLE OVERLAP Fifo
 CMS CSC DAQ MOTHERBOARD
 CMS CSC ELECTRONICS

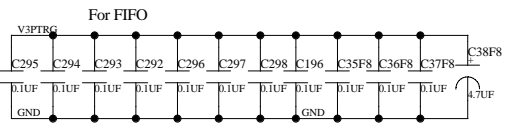
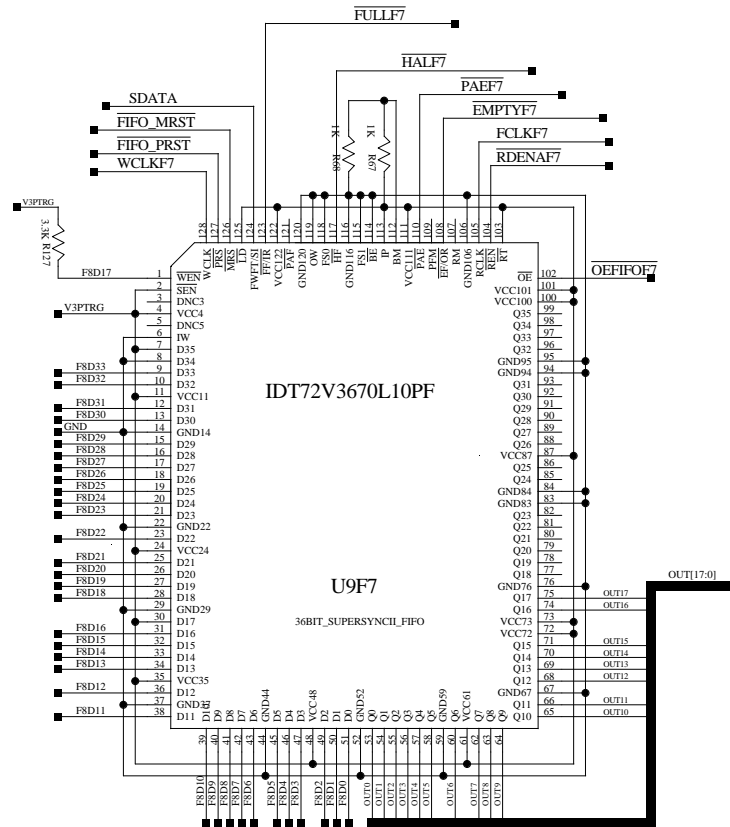
BY G
 DATE 7-3-2001_16:20

PARENT PAGE 1

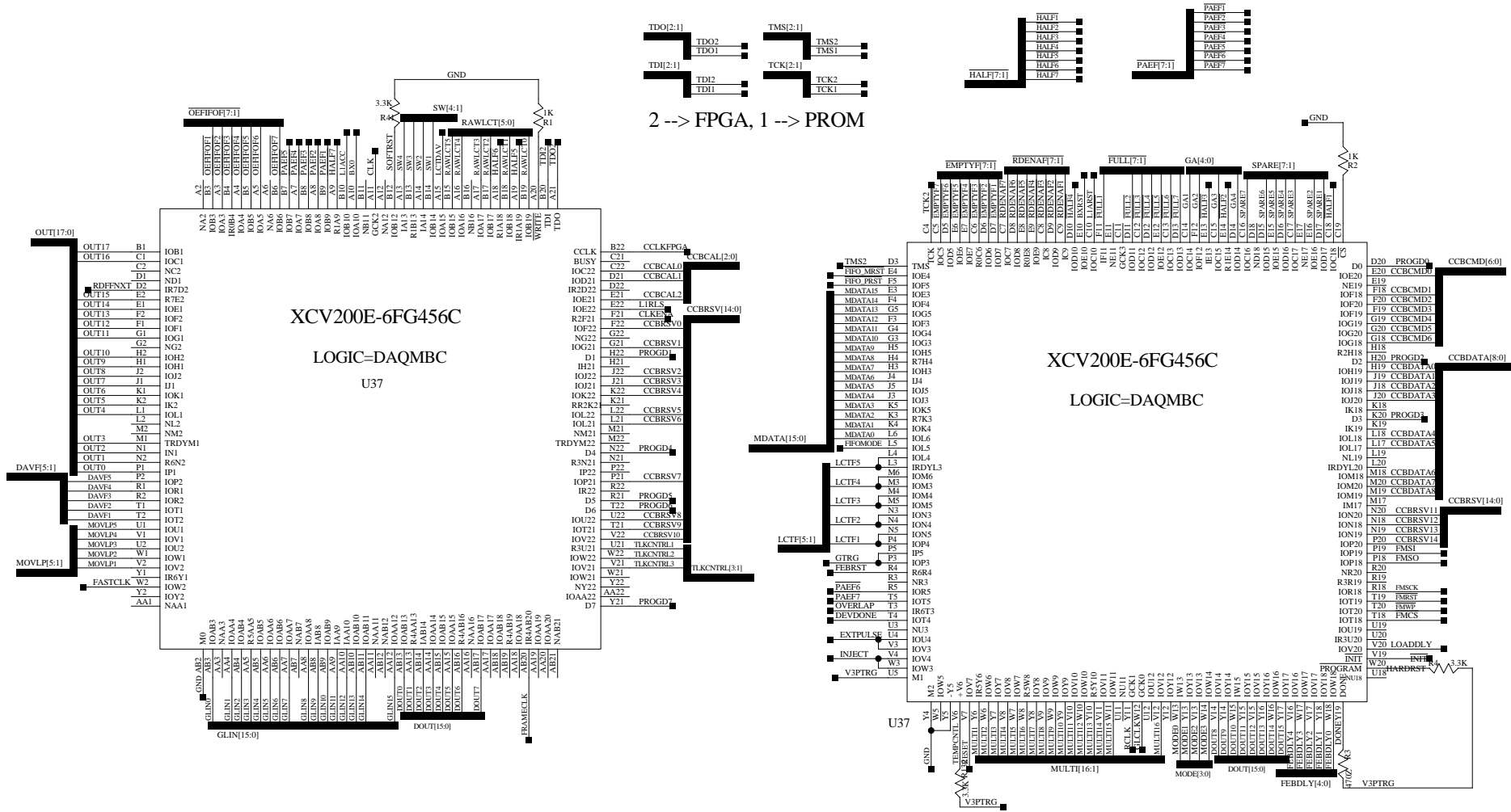
PROJECT DAQMBP
 FILE DATACON . 12
 PAGE 10K



Stuff either R67 or R68, but not both
 Load R68, BM low, 36 bit in and 36 bit out. (actually, only 18 low-order bits used)
 Load R67, BM high, 36 bit in and 18 bit out. The high-order 18-bit go out first, then low-order 18-bit

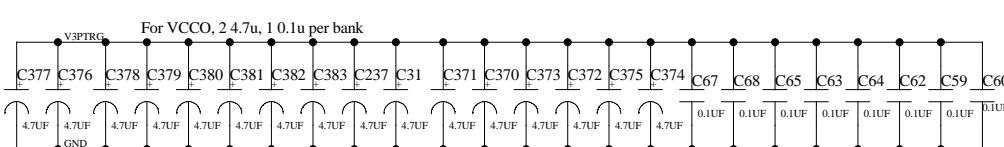
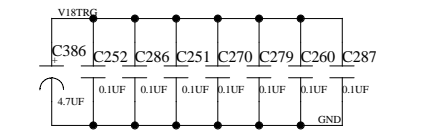
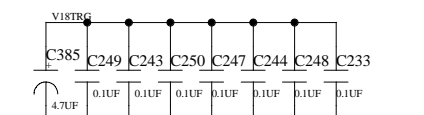
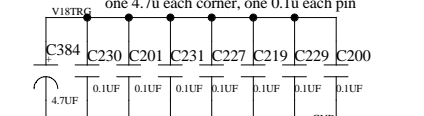
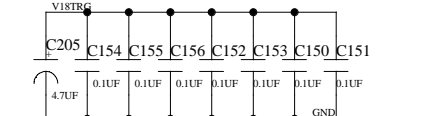
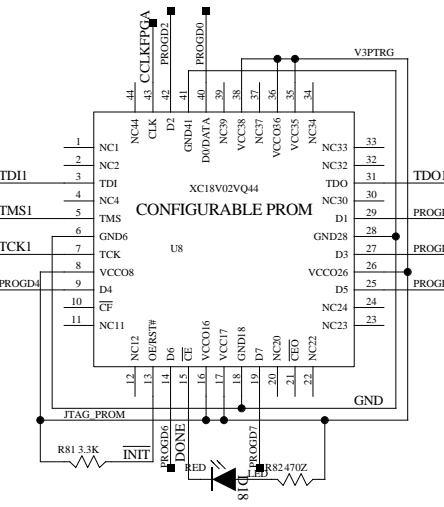
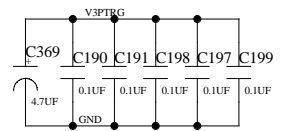
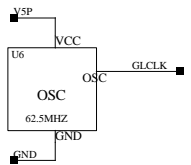
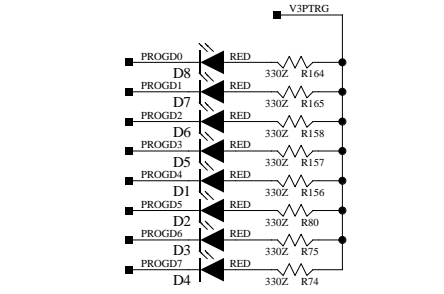
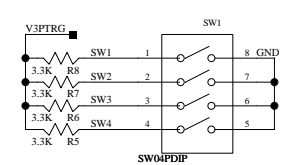
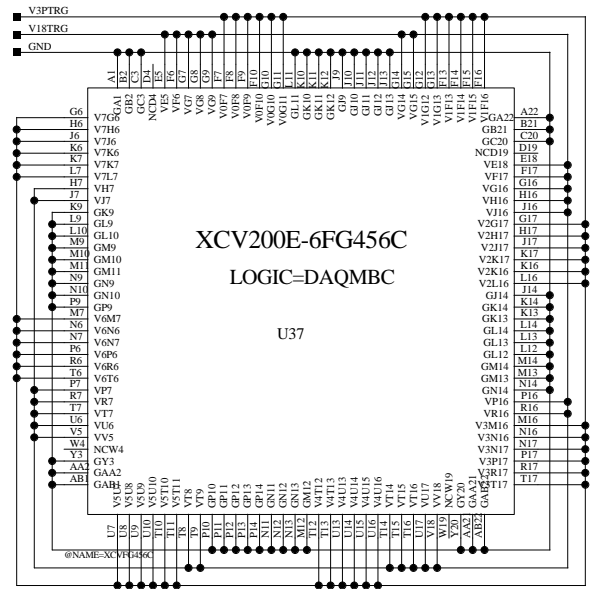
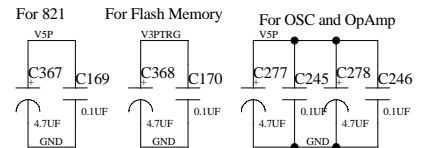
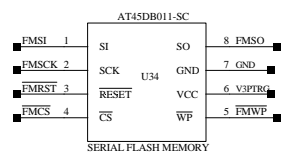
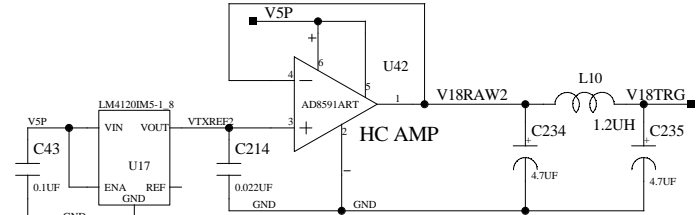
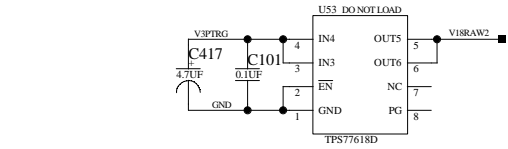
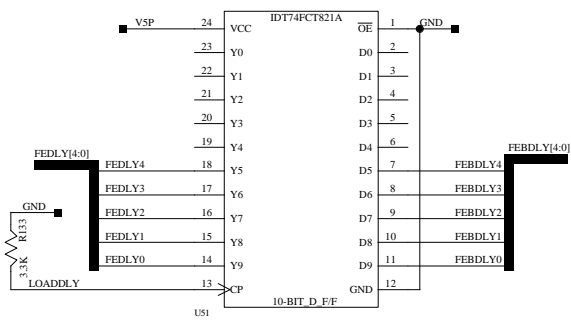


Fifo F8

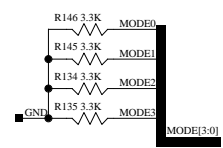
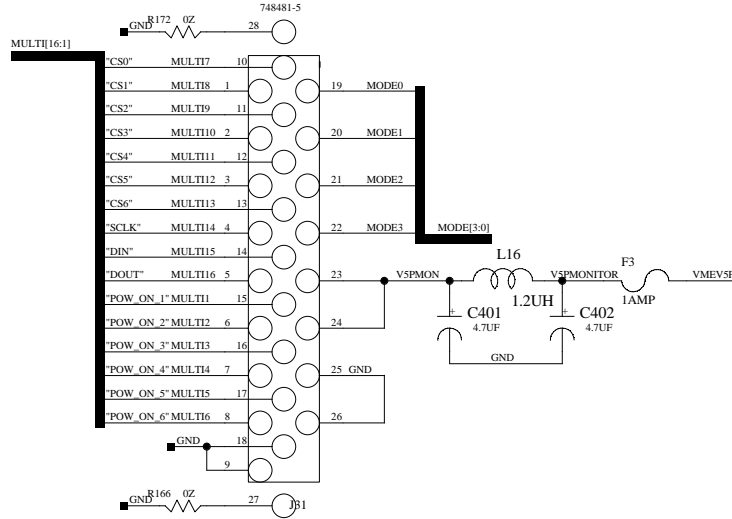


Connect all the signals on this page to FPGA
 Connect two I/O pins for EXTPULSE, INJECT, LCTF1, LCTF2, LCTF3, LCTF4, LCTF5 and GTRG
 For pin compatible with different FPGA, use IO** pins
 Put SPARE[7:1] in one I/O bank

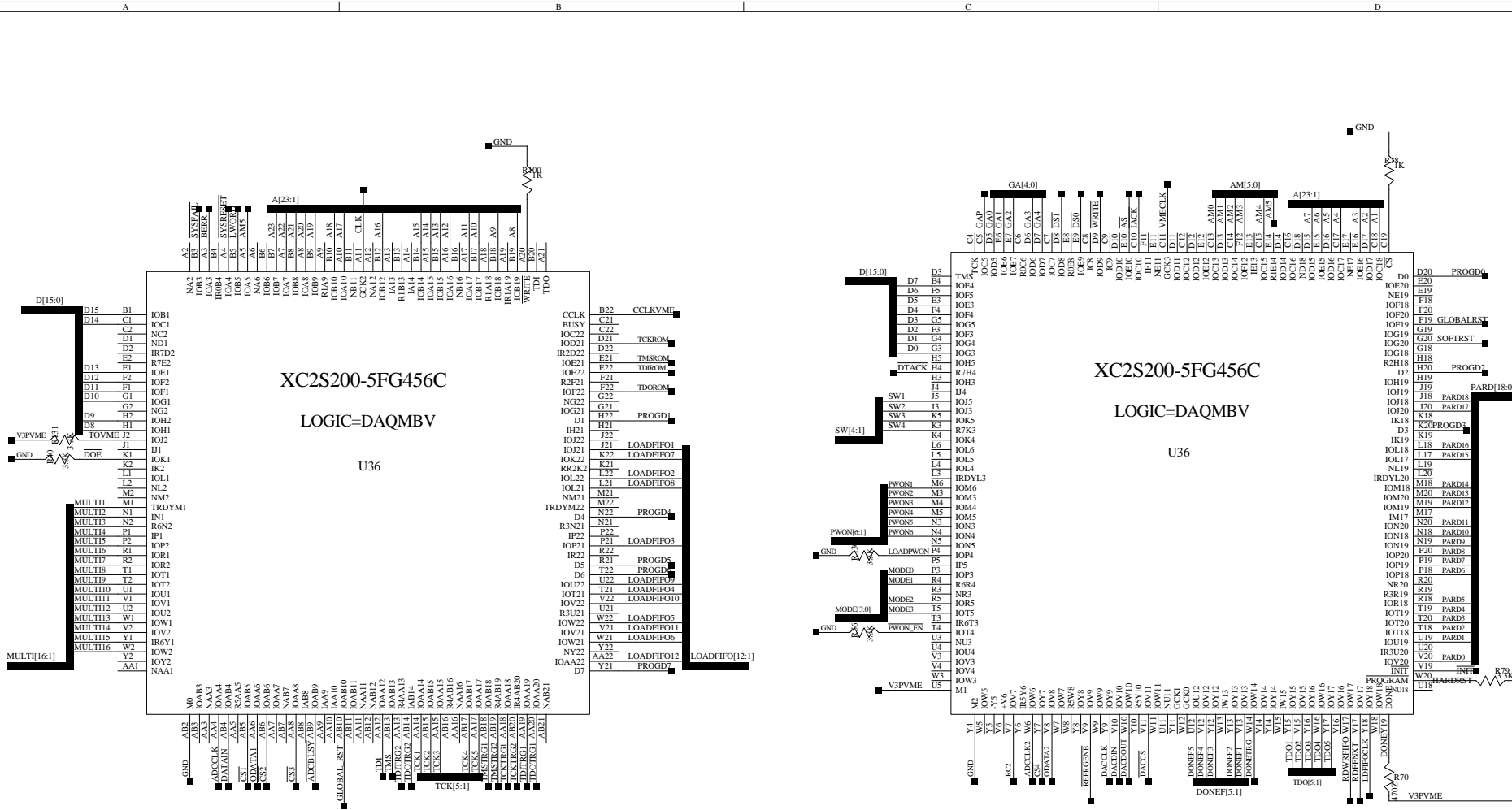
CONFIGURE DELAYS



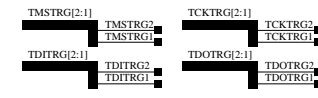
These are the functions if the LVDB monitor uses 6 ADC's.

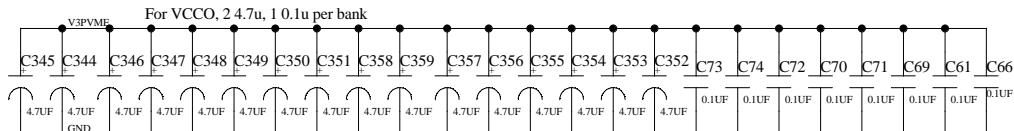
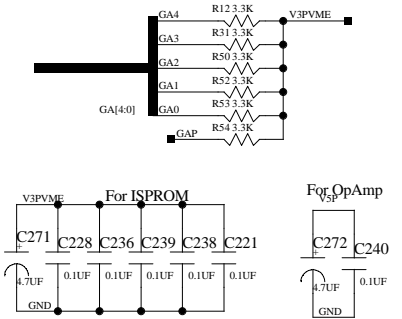
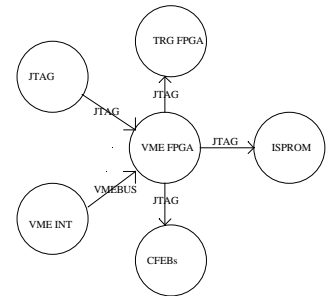
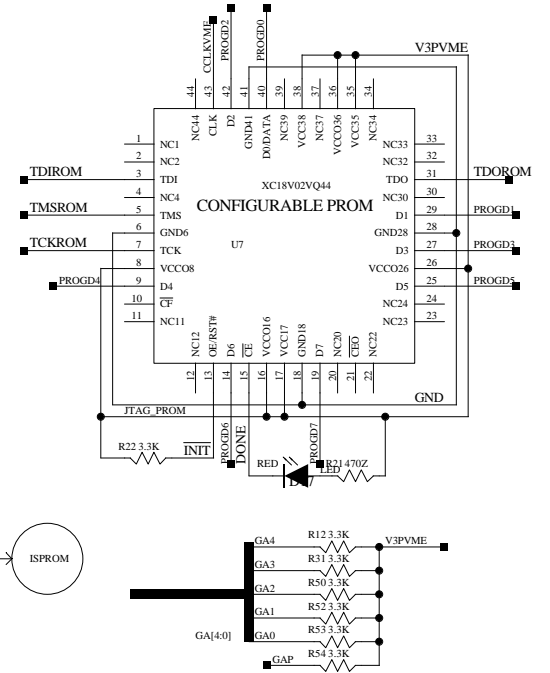
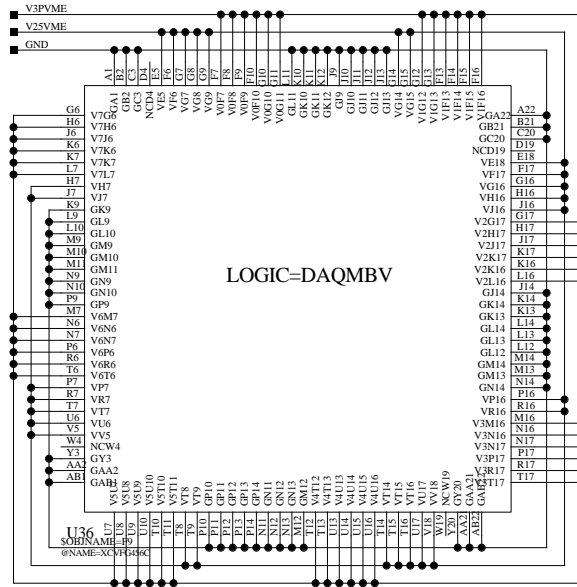
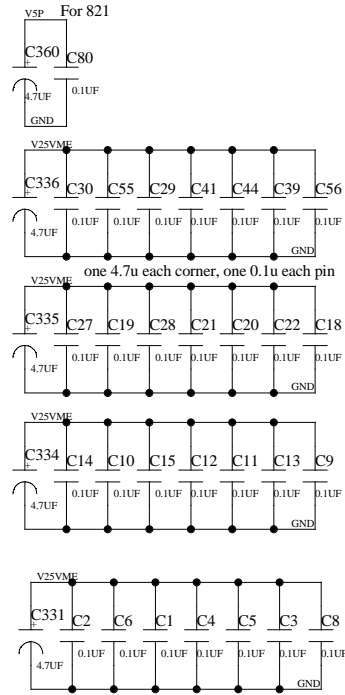
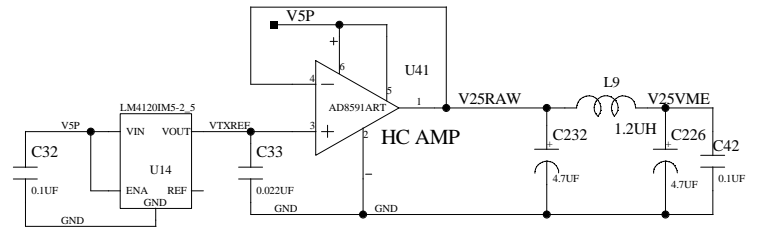
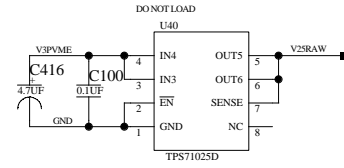
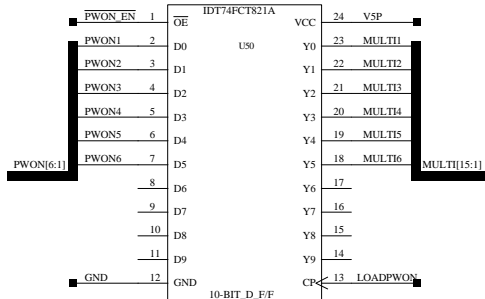


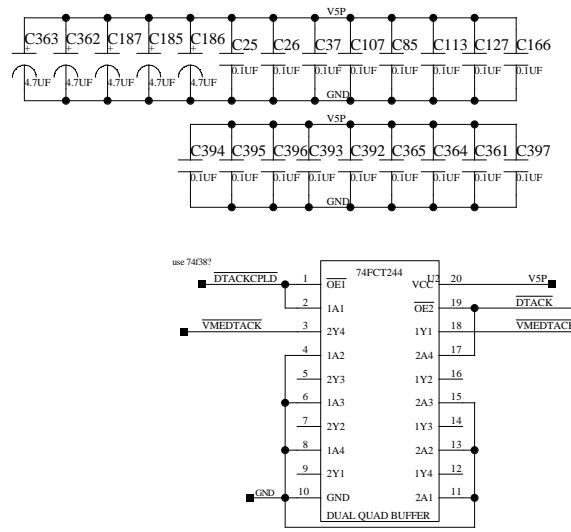
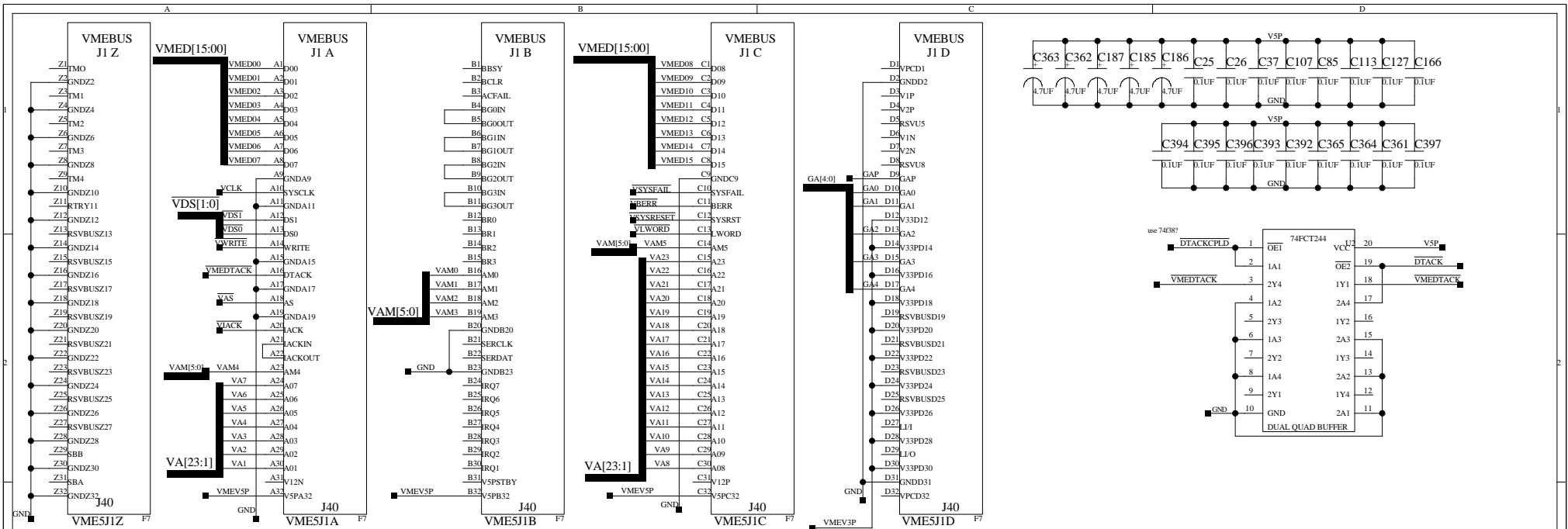
Default mode setting



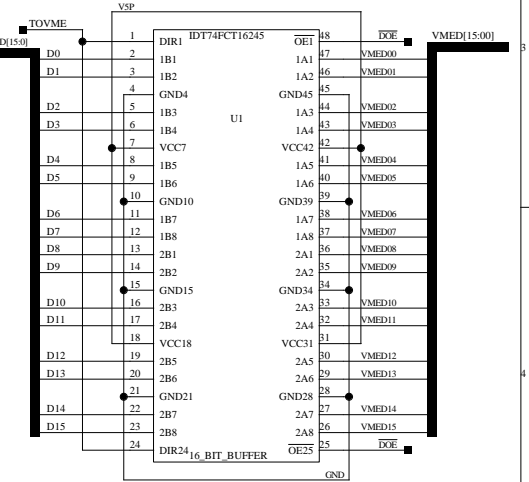
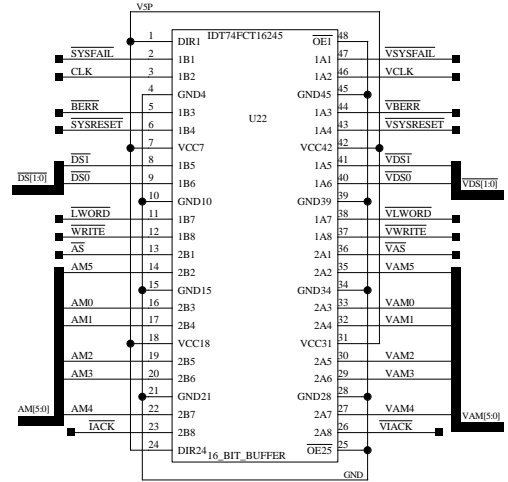
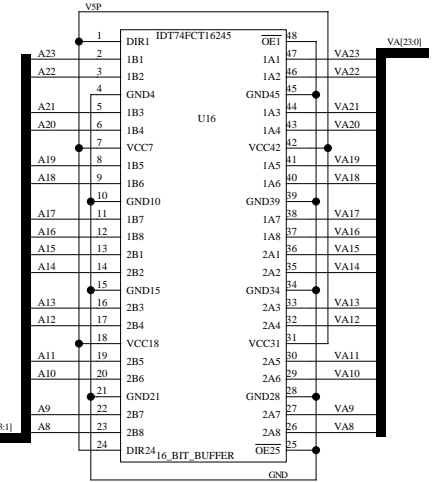
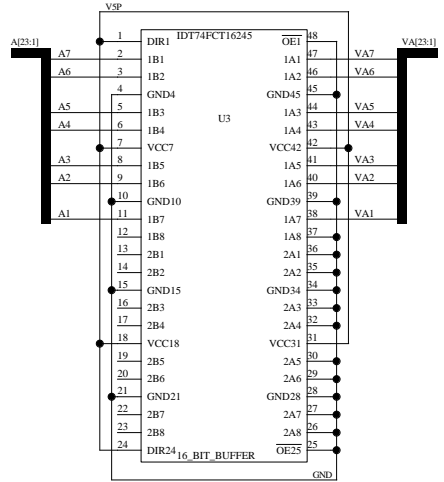
Connect all the signals on this page to FPGA
 For pin compatible with different FPGA, use IO** pins



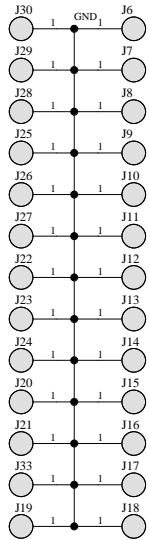




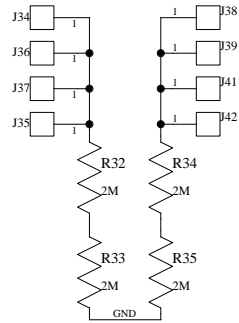
Harting PN# 02.01.160.2101



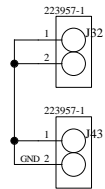
GROUND POINTS



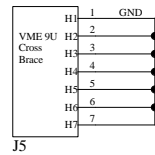
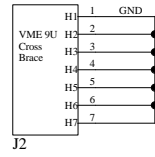
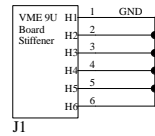
DISCHARGE UNIT



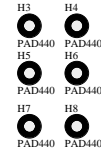
FEMALE GUIDES



BOARD STIFFENER



MOUNTING POINTS



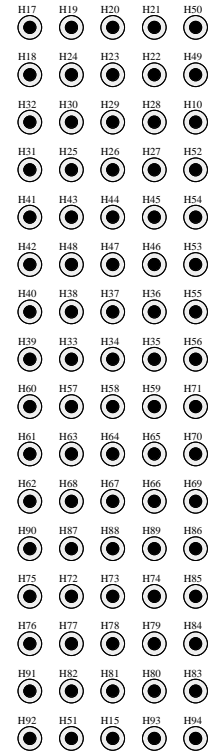
GLOBAL FIDUCIALS



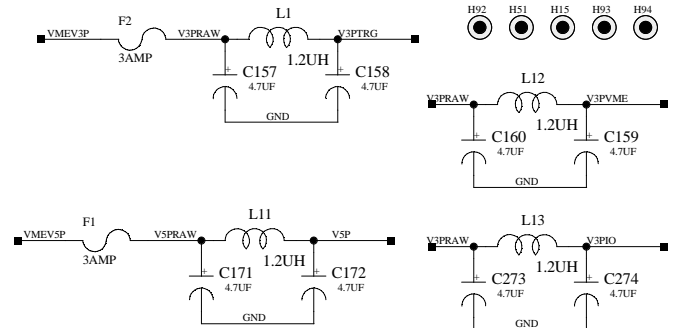
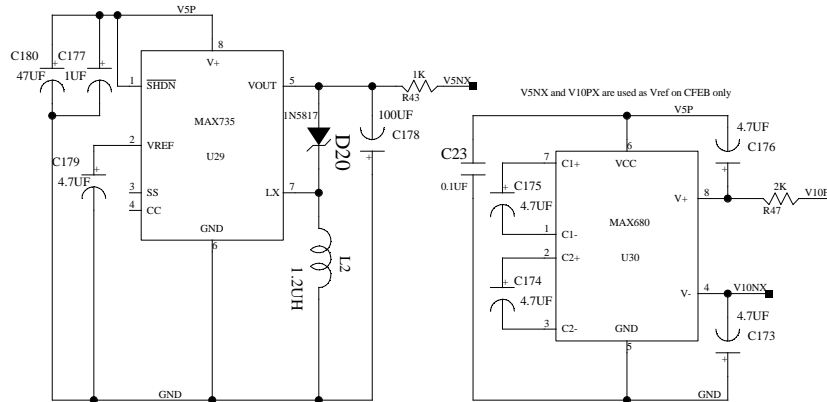
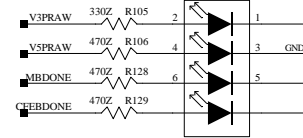
FRONT PANEL MOUNTS

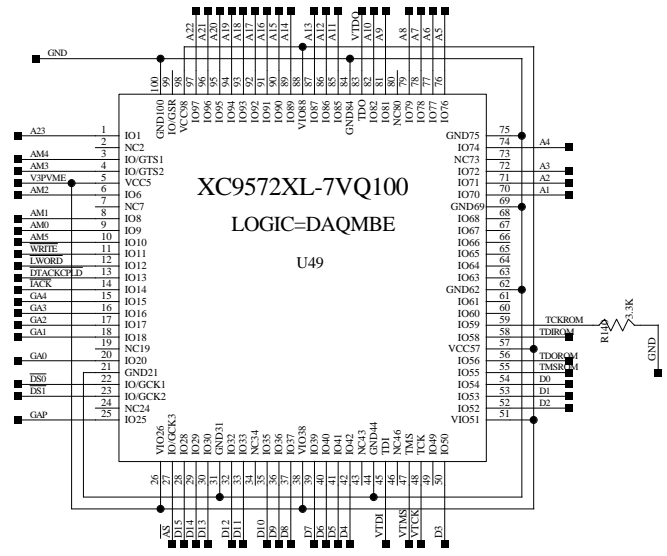
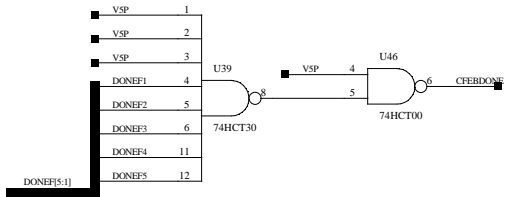
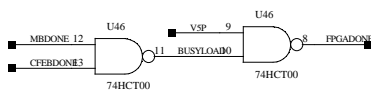
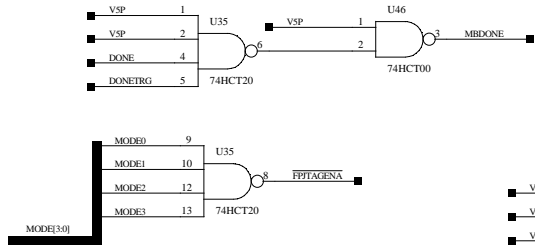


PART FIDUCIALS

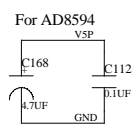
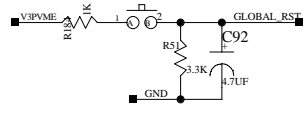
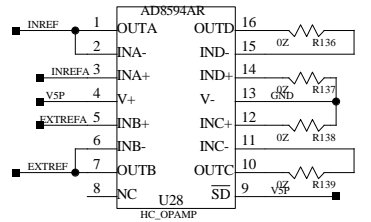
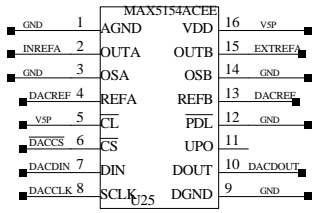
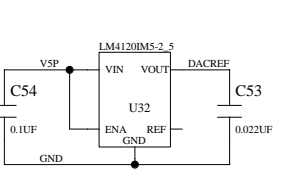
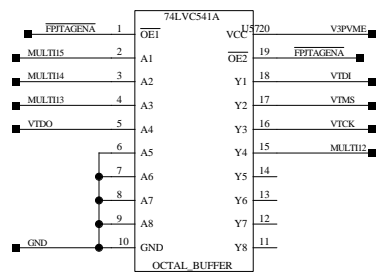
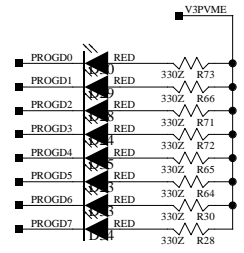
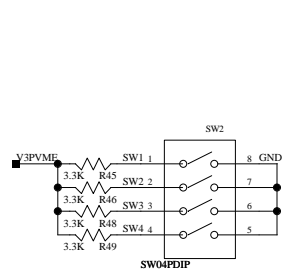


Power Monitor, Placed on front panel D10

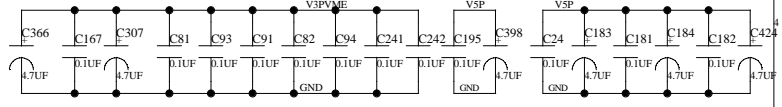


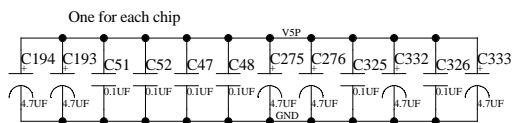
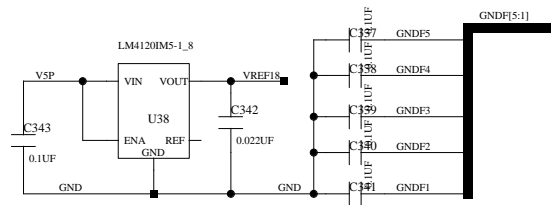
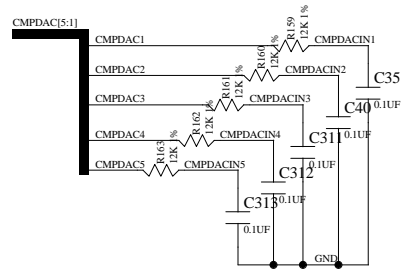
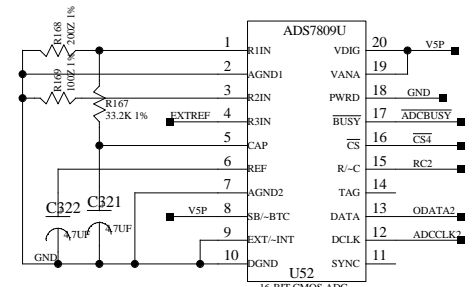
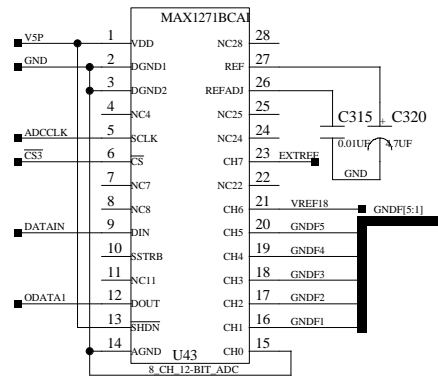
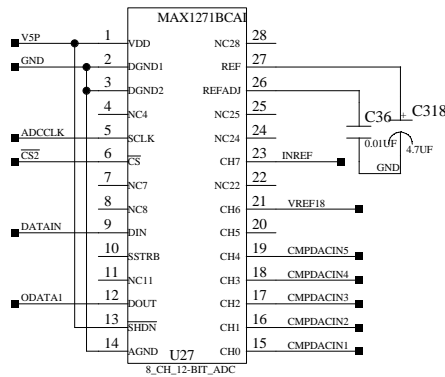
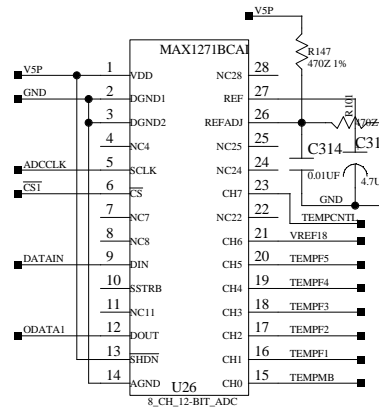
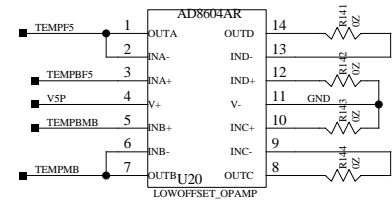
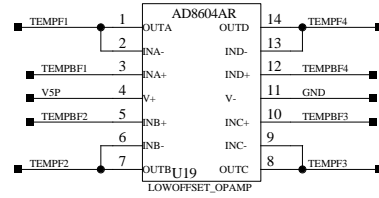
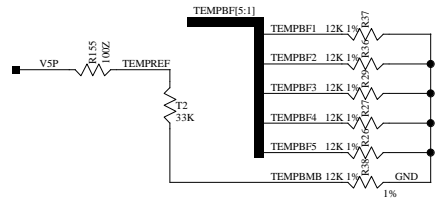


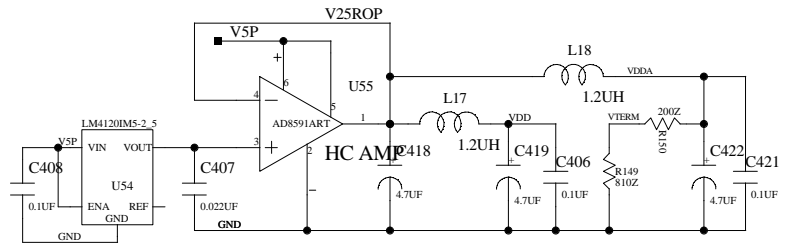
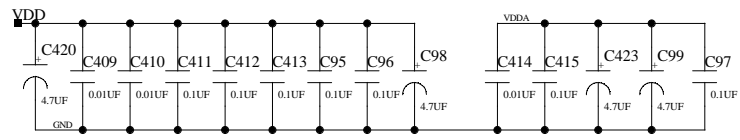
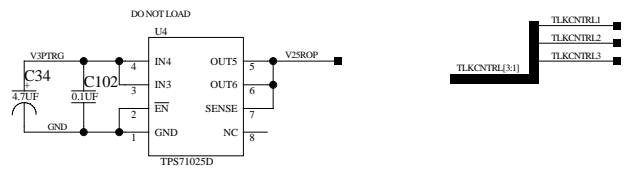
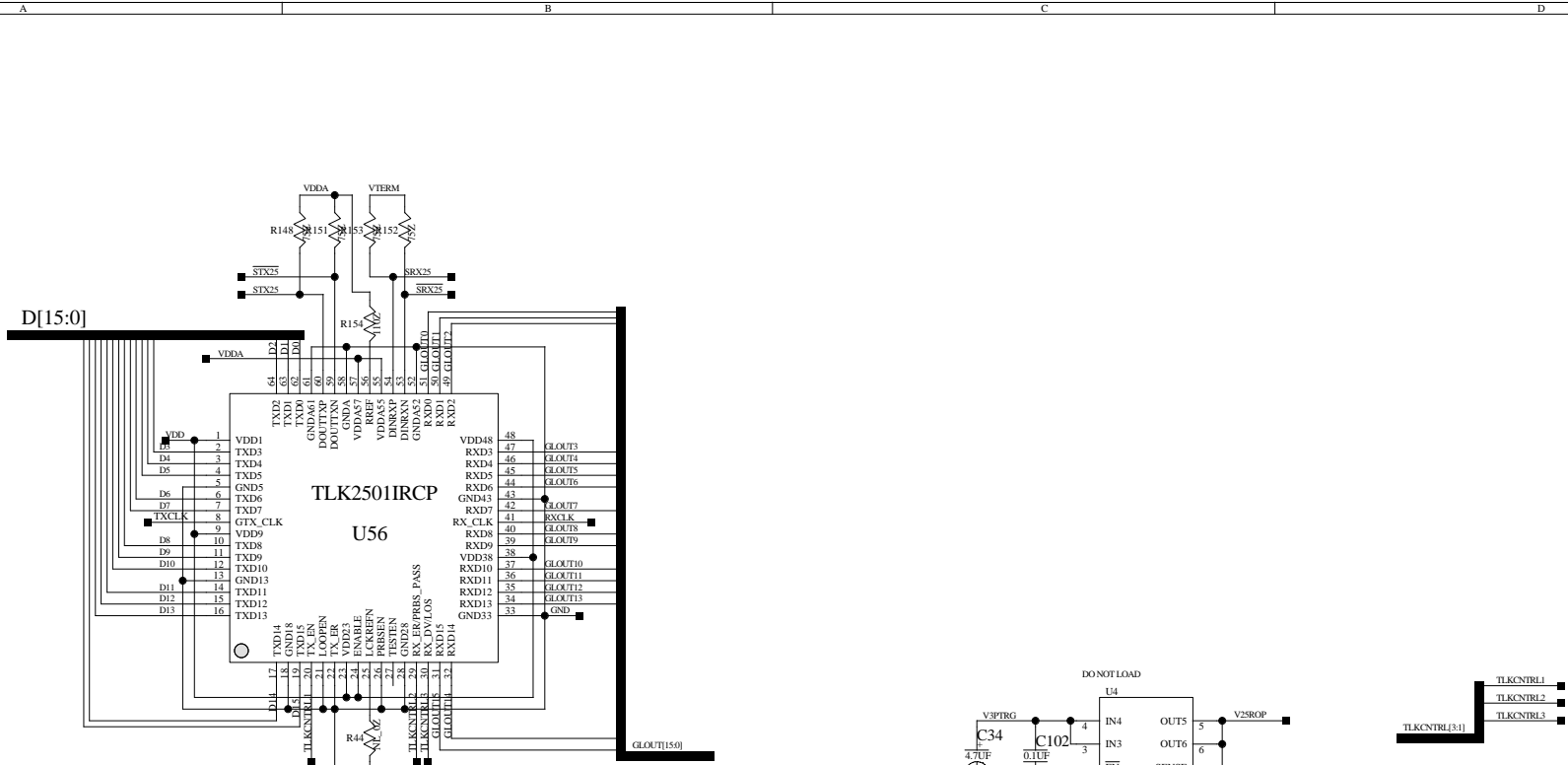
Emergency Case: PROMs, FPGAs not programmed

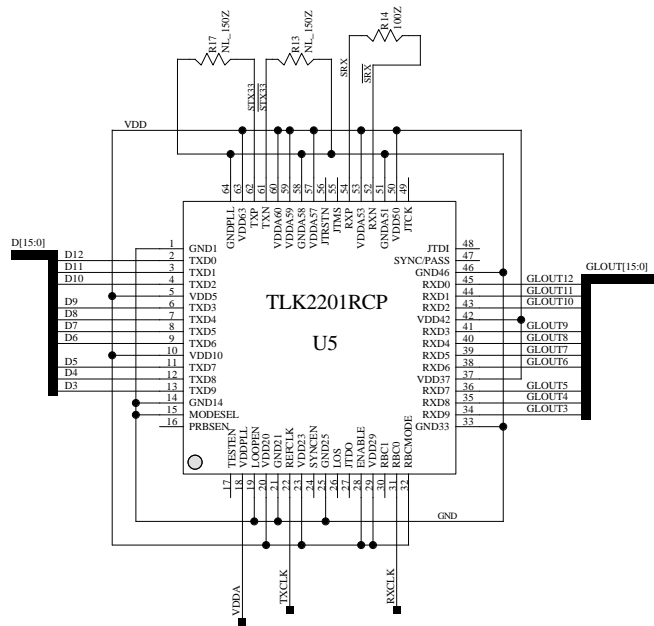


For CPLD and Buffer 541

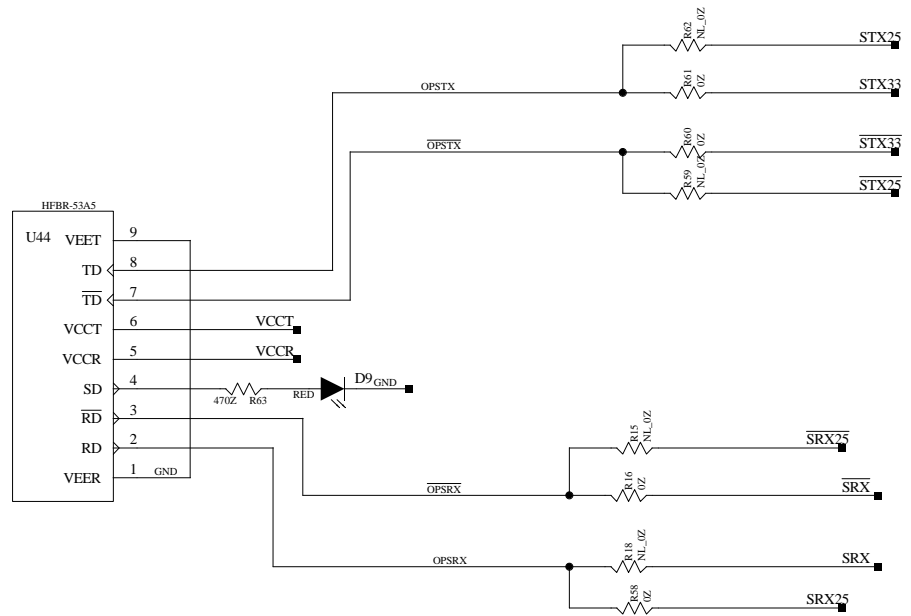
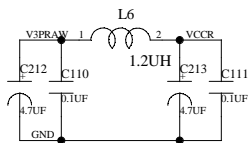
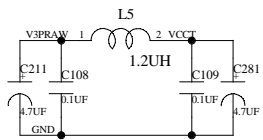




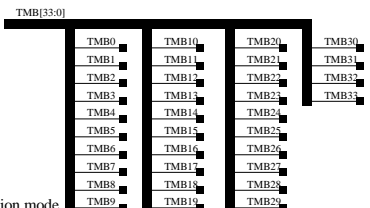
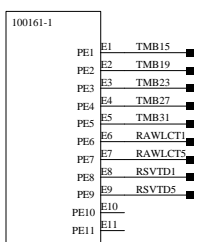
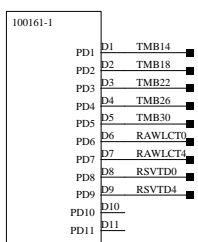
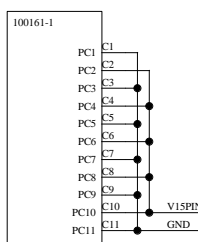
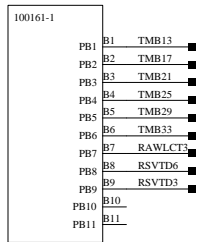
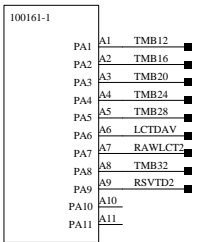
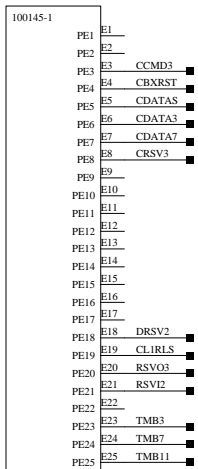
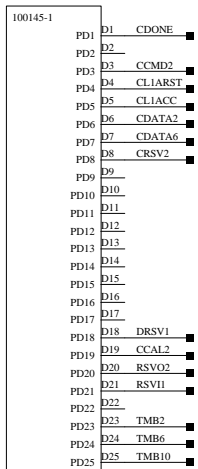
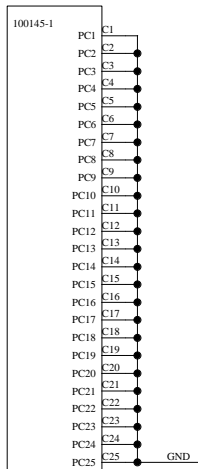
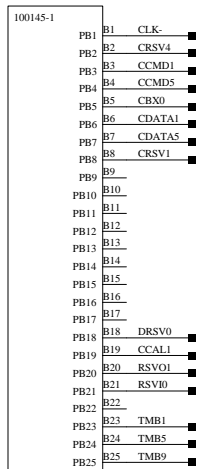
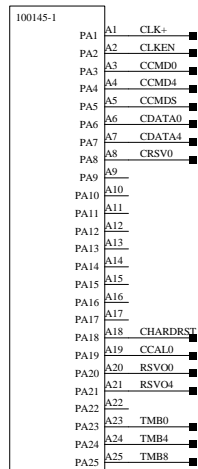




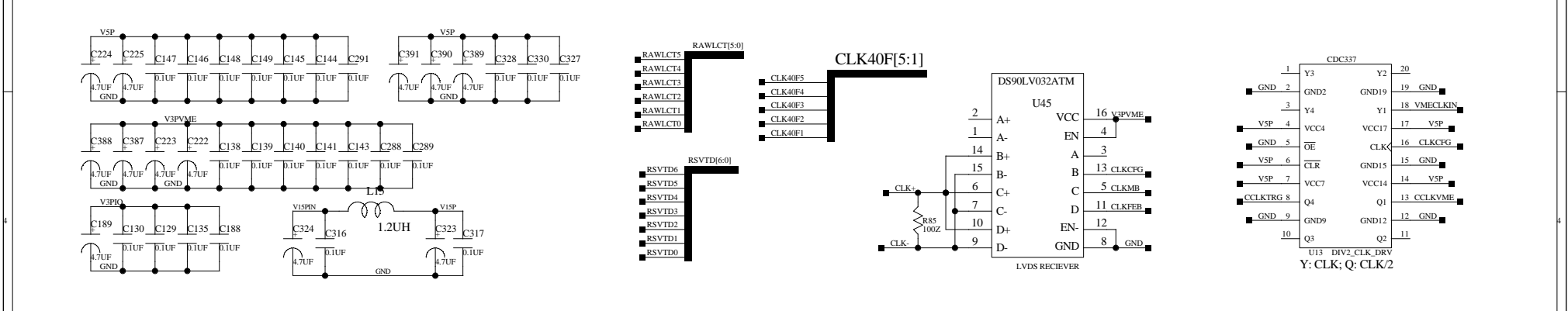
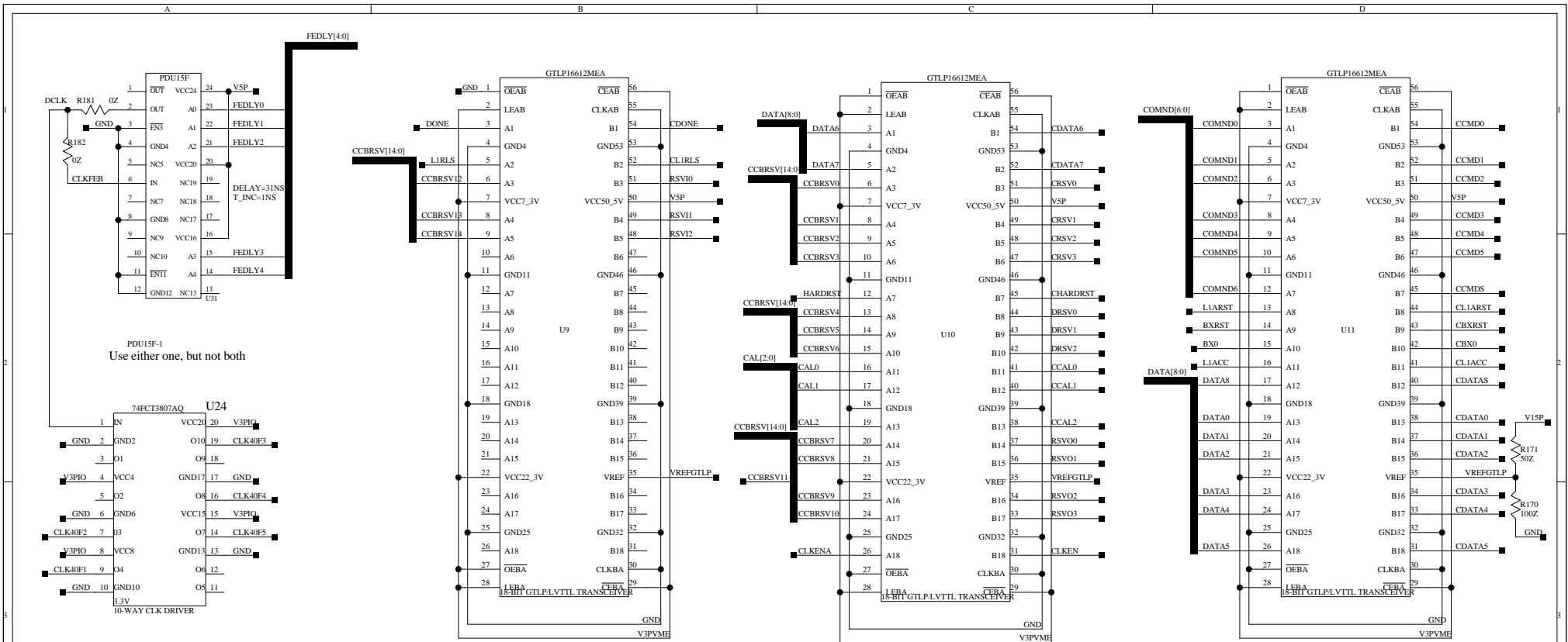
125MHz to match with Gigabit ethernet



NOTE: All high speed serial lines must be smooth, no right angles and no layer changes.



TMB[14:0]: CLCT/TMB data to 18-bit fifo
 TMB[29:15]: Additional CLCT/TMB data to 36-bit fifo
 TMB30: DDU special word flag
 TMB31: Last word flag bit
 TMB32: 40MHz clock to write to FIFO
 TMB33: Fifo write_enable inverted
 Spare[7:1]: Used to exchange information in CFEB calibration mode



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE GTLP receiver and CLOCK distribution CMS CSC DAQ MOTHERBOARD CMS CSC ELECTRONICS	BY GU PARENT PAGE 1 DATE 8-10-2001_14:05	PROJECT DAQMBP FILE CCB . 2 PAGE 50A
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