CMS EMU
DMB/CFEB Programmers Manual

Version 2.5

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VME address space organization and FPGA instruction descriptions.

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Device Selection Space Declaration

[A18…A12]

Address in Hex	Device
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VME Interface FPGA

Address in Hex	R/W/Ex	Description
00000	Ex	NOOP
00004	R	Read Status
00008		
0000C		
00010		
00014		
00018		
0001C		
00020		
00024		
00028		
0002C		
00030		
00034		
00038		
0003C		
00040		
00044		
00048		
. . .		
00FF8		
00FFC		

CFEB's (JTAG Port)

A11…A8	A7…A2
Shift Bit Count	Instruction

Note: A11 thru A8 contain the number of bits to be shifted minus 1, if applicable.
For example: when shifting 8 bits then Y in the table below should be 7.

In the table below, Y represents the bit count.

Address in Hex	R/W/Ex	Description
01Y00	W	Shift Data; no TMS header; no TMS tailer
01Y04	W	Shift Data with TMS header only
01Y08	W	Shift Data with TMS tailer only
01Y0C	W	Shift Data with TMS header & TMS tailer
01Y10		
01Y14	R	Read TDO register
01Y18	Ex	Reset JTAG State Machine
01Y1C	W	Shift Instruction Register
01Y20	W	Write Select Register
01Y24	R	Read Select Register
01Y28		
01Y2C		
01Y30	W	Shift Inst; no TMS header; no TMS tailer
01Y34	W	Shift Instruction with TMS header only
01Y38	W	Shift Instruction with TMS tailer only
01Y3C	W	Shift Inst. with TMS header & TMS tailer
01Y40		
01Y44		
01Y48	W	Shift with Special TMS trailer only (instr-to-data)
01Y4C	W	Shift with TMS header and Special TMS trailer (instr-to-data)
. . .		

DMB Controller FPGA (JTAG Port)

A11…A8	A7…A2
Shift Bit Count	Instruction

Note: A11 thru A8 contain the number of bits to be shifted minus 1, if applicable.
For example: when shifting 8 bits then Y in the table below should be 7.

In the table below, Y represents the bit count.

Address in Hex	R/W/Ex	Description
02Y00	W	Shift Data; no TMS header; no TMS tailer
02Y04	W	Shift Data with TMS header only
02Y08	W	Shift Data with TMS tailer only
02Y0C	W	Shift Data with TMS header & TMS tailer
02Y10		
02Y14	R	Read TDO register
02Y18	Ex	Reset JTAG State Machine
02Y1C	W	Shift Instruction Register
02Y20		
02Y24		
02Y28		
02Y2C		
02Y30	W	Shift Inst; no TMS header; no TMS tailer
02Y34	W	Shift Instruction with TMS header only
02Y38	W	Shift Instruction with TMS tailer only
02Y3C	W	Shift Inst. with TMS header & TMS tailer
02Y40		
02Y44		
02Y48	W	Shift with Special TMS trailer only (instr-to-data)
02Y4C	W	Shift with TMS header and Special TMS trailer (instr-to-data)
. . .		

DMB Controller PROM (JTAG Port)

A11…A8	A7…A2
Shift Bit Count	Instruction

Note: A11 thru A8 contain the number of bits to be shifted minus 1, if applicable.
For example: when shifting 8 bits then Y in the table below should be 7.

In the table below, Y represents the bit count.

Address in Hex	R/W/Ex	Description
03Y00	W	Shift Data; no TMS header; no TMS tailer
03Y04	W	Shift Data with TMS header only
03Y08	W	Shift Data with TMS tailer only
03Y0C	W	Shift Data with TMS header & TMS tailer
03Y10		
03Y14	R	Read TDO register
03Y18	Ex	Reset JTAG State Machine
03Y1C	W	Shift Instruction Register
03Y20		
03Y24		
03Y28		
03Y2C		
03Y30	W	Shift Inst; no TMS header; no TMS tailer
03Y34	W	Shift Instruction with TMS header only
03Y38	W	Shift Instruction with TMS tailer only
03Y3C	W	Shift Inst. with TMS header & TMS tailer
03Y40		
03Y44		
03Y48	W	Shift with Special TMS trailer only (instr-to-data)
03Y4C	W	Shift with TMS header and Special TMS trailer (instr-to-data)
. . .		

VME Interface PROM (JTAG Port)

A11…A8	A7…A2
Shift Bit Count	Instruction

Note: A11 thru A8 contain the number of bits to be shifted minus 1, if applicable.
For example: when shifting 8 bits then Y in the table below should be 7.

In the table below, Y represents the bit count.

Address in Hex	R/W/Ex	Description
04Y00	W	Shift Data; no TMS header; no TMS tailer
04Y04	W	Shift Data with TMS header only
04Y08	W	Shift Data with TMS tailer only
04Y0C	W	Shift Data with TMS header & TMS tailer
04Y10		
04Y14	R	Read TDO register
04Y18	Ex	Reset JTAG State Machine
04Y1C	W	Shift Instruction Register
04Y20		
04Y24		
04Y28		
04Y2C		
04Y30	W	Shift Inst; no TMS header; no TMS tailer
04Y34	W	Shift Instruction with TMS header only
04Y38	W	Shift Instruction with TMS tailer only
04Y3C	W	Shift Inst. with TMS header & TMS tailer
04Y40		
04Y44		
04Y48	W	Shift with Special TMS trailer only (instr-to-data)
04Y4C	W	Shift with TMS header and Special TMS trailer (instr-to-data)
. . .		

Dual DAC (MAX5154)

Address in Hex	R/W/Ex	Description
05000	W	Set Calibration DAC
05004		
05008		
0500C		
. . .		

Serial Data Format

MSB……..…….……..LSB			
← 16 Bits of Serial Data →			
Address Bit	Control Bit	MSB……..Data Bits……..LSB	Sub bit
A0	C1,C0	D11……..……D0	S0
1 Address Bit/2 Control Bits		← 12 Data Bits →	0

A0	DAC Port Function
0	Internal charge injection voltage setting (trigger test pulses).
1	External capacitor charge injection voltage setting (precision calibration).

16 Bit Serial Word			**Function**
A0 C1 C0	**D11……D0 MSB LSB**	**S0**	
0 0 1	12 bits of DAC data	0	Load input register A; DAC register is unchanged.
1 0 1	12 bits of DAC data	0	Load input register B; DAC register is unchanged.
0 1 0	**12 bits of DAC data**	**0**	**Load input register A; all DAC registers are updated.**
1 1 0	**12 bits of DAC data**	**0**	**Load input register B; all DAC registers are updated.**
0 1 1	12 bits of DAC data	0	Load all DAC registers from the shift register (start up both DACs with new data).
1 0 0	xxxxxxxxxxxx	0	Update both DAC registers from their respective input registers (start up both DACs with data previously stored in the input registers).
1 1 1	xxxxxxxxxxxx	0	Shut down both DACs if PDL =1.
0 0 0	0 0 1 x xxxxxxxx	0	Update DAC register A from input register A (start up DAC A with data previously stored in inpu register A).
0 0 0	1 0 1 x xxxxxxxx	0	Update DAC register B from input register A (start up DAC B with data previously stored in inpu register B).
0 0 0	1 1 0 x xxxxxxxx	0	Shut down DAC A when PDL =1.
0 0 0	1 1 1 x xxxxxxxx	0	Shut down DAC B when PDL =1.
0 0 0	0 1 0 x xxxxxxxx	0	UPO goes low (default).
0 0 0	0 1 1 x xxxxxxxx	0	UPO goes high.
0 0 0	1 0 0 1 xxxxxxxx	0	Mode 1, DOUT clocked out on SCLK's rising edge.
0 0 0	1 0 0 0 xxxxxxxx	0	Mode 0, DOUT clocked out on SCLK's falling edge.
0 0 0	0 0 0 x xxxxxxxx	0	No operation (NOOP).

FIFO's

Address in Hex	R/W/Ex	Description
06000	W	Write data; (no lastword, no overlap)
06004	W	Write data; (lastword, no overlap)
06008	W	Write data; (no lastword, overlap)
0600C	W	Write data; (lastword, overlap)
06010	R	Read low order 16 bits; does not Incr. FIFO
06014	R	Read low order 16 bits; Incr. FIFO
06018	R	Read high order 2 bits; does not Incr. FIFO
0601C	R	Read high order 2 bits; Incr. FIFO
06020	W	Write Select Register (more than 1 FIFO can be enabled)
06024	R	Read Select Register (for verification)
06028		
0602C	Ex	Increment FIFO read counter
. . .		

Normal Procedure for Writing/Reading FIFO's

Writing to FIFO's

1. Select which FIFO(s) to write to (address 6020) in order to output enable the correct buffer(s).
2. Load data in VME interface FPGA by writing to address 6000, 4, 8, or C. This will present the data to the FIFO(s) and produces a write enable signal as well as the write clock.
3. Repeat step 2 until all data is written or the FIFO(s) is (are) full.
4. Restore normal operation by writing zero to the select register disabling the buffers and enabling the channel link path.

Reading From FIFO's

1. Select which FIFO to read back by sending JTAG instructions to the controller FPGA. Use JTAG instruction XXXX along with data for the read enable register.
2. If 18 bits are to be read, read the high order 2 bits first (address 6018). Then read the low order 16 bits with an increment (address 6010).
3. Repeat step 2 until all data has been read from that FIFO.
4. Repeat step 1-3 until all FIFO's have been read.

DMB ADC's

Address in Hex	R/W/Ex	Description
07000	W	Write Control Byte to MAX1271's
07004	R	Read Data Back from 1271 Register
07008		
0700C	R	Read Data Back from Burr Brown Reg.
07010		
07014		
07018		
0701C		
07020	W	Write Select Register
07024	R	Read Select Register
07028		
0702C		
07030		
07034		
07038		
0703C		
07040		
07044		
07048		
0704C		
07050		
07054		
07058		
0705C		
07060		
07064		
07068		
0706C		
. . .		

Control Byte Format Specific To DMB ADC's (MAX1271)

Vref = internal reference = 4.096 V
Normal operation (always on)
External Clock Mode

Control-Byte Format

Bit 7 (MSB)	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**
Start	SEL2	SEL1	SEL0	RNG	BIP	PD1	PD0

Measurement	Select Reg.	Chan	Range	Conversion	Control Byte Binary	Control Byte Hex
DMB Temp	1	0	0-4.096	ADC*4.096/4096	10001001	89
CFEB1 Temp	1	1	0-4.096	ADC*4.096/4096	10011001	99
CFEB2 Temp	1	2	0-4.096	ADC*4.096/4096	10101001	A9
CFEB3 Temp	1	3	0-4.096	ADC*4.096/4096	10111001	B9
CFEB4 Temp	1	4	0-4.096	ADC*4.096/4096	11001001	C9
CFEB5 Temp	1	5	0-4.096	ADC*4.096/4096	11011001	D9
1.8V Ref.	1	6	0-4.096	ADC*4.096/4096	11101001	E9
Virtex Temp	1	7	0-4.096	ADC*4.096/4096	11111001	F9
Comp. DAC 1	2	0	0-4.096	ADC*4.096/4096	10001001	89
Comp. DAC 2	2	1	0-4.096	ADC*4.096/4096	10011001	99
Comp. DAC 3	2	2	0-4.096	ADC*4.096/4096	10101001	A9
Comp. DAC 4	2	3	0-4.096	ADC*4.096/4096	10111001	B9
Comp. DAC 5	2	4	0-4.096	ADC*4.096/4096	11001001	C9
N/C	2	5	0-4.096	ADC*4.096/4096	11011001	D9
1.8V Ref.	2	6	0-4.096	ADC*4.096/4096	11101001	E9
Int. Cal. DAC	2	7	0-4.096	ADC*4.096/4096	11111001	F9
DMB GND	3	0	+/-2.048	ADC*2*2.048/4096	10000101	85
CFEB1 GND	3	1	+/-2.048	ADC*2*2.048/4096	10010101	95
CFEB2 GND	3	2	+/-2.048	ADC*2*2.048/4096	10100101	A5
CFEB3 GND	3	3	+/-2.048	ADC*2*2.048/4096	10110101	B5
CFEB4 GND	3	4	+/-2.048	ADC*2*2.048/4096	11000101	C5
CFEB5 GND	3	5	+/-2.048	ADC*2*2.048/4096	11010101	D5
1.8V Ref.	3	6	+/-2.048	ADC*2*2.048/4096	11100101	E5
Ext. Cal. DAC	3	7	+/-2.048	ADC*2*2.048/4096	11110101	F5

Low Voltage Monitoring

Address in Hex	R/W/Ex	Description
08000	W	Write Control Byte to MAX1270's
08004	R	Read Data Back
08008		
0800C		
08010	W	Write Low Voltage Power Register
08014	R	Read Low Voltage Power Register
08018		
0801C		
08020	W	Write ADC Chip Select Register
08024	R	Read ADC Chip Select Register
08028		
0802C		
08030		
08034		
08038		
0803C		
08040		
08044		
08048		
0804C		
08050		
08054		
08058		
0805C		
08060		
08064		
08068		
0806C		
. . .		

Control Byte Format Specific To LV Monitor ADC's (MAX1270)

Vref = internal reference = 4.096 V
Normal operation (always on)
External Clock Mode

Control-Byte Format

Bit 7 (MSB)	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**
Start	SEL2	SEL1	SEL0	RNG	BIP	PD1	PD0

Measurement	Select Reg.	Chan	Range	Conversion	Control Byte Binary	Control Byte Hex
CFEB1 OCM 3	1	0	0-10 V	ADC*10/4096	10001001	89
CFEB1 OCM 5	1	1	0-10 V	ADC*10/4096	10011001	99
CFEB1 OCM 6	1	2	0-10 V	ADC*10/4096	10101001	A9
CFEB2 OCM 3	1	3	0-10 V	ADC*10/4096	10111001	B9
CFEB2 OCM 5	1	4	0-10 V	ADC*10/4096	11001001	C9
CFEB2 OCM 6	1	5	0-10 V	ADC*10/4096	11011001	D9
CFEB3 OCM 3	1	6	0-10 V	ADC*10/4096	11101001	E9
CFEB3 OCM 5	1	7	0-10 V	ADC*10/4096	11111001	F9
CFEB3 OCM 6	2	0	0-10 V	ADC*10/4096	10001001	89
CFEB4 OCM 3	2	1	0-10 V	ADC*10/4096	10011001	99
CFEB4 OCM 5	2	2	0-10 V	ADC*10/4096	10101001	A9
CFEB4 OCM 6	2	3	0-10 V	ADC*10/4096	10111001	B9
CFEB5 OCM 3	2	4	0-10 V	ADC*10/4096	11001001	C9
CFEB5 OCM 5	2	5	0-10 V	ADC*10/4096	11011001	D9
CFEB5 OCM 6	2	6	0-10 V	ADC*10/4096	11101001	E9
ALCT OCM 3.3	2	7	0-10 V	ADC*10/4096	11111001	F9
ALCT OCM 1.8	3	0	0-10 V	ADC*10/4096	10001001	89
ALCT OCM 5B	3	1	0-10 V	ADC*10/4096	10011001	99
ALCT OCM 5A	3	2	0-10 V	ADC*10/4096	10101001	A9

Control Byte Format Specific To LV Monitor ADC's (MAX1270) Continued

Vref = internal reference = 4.096 V
Normal operation (always on)
External Clock Mode

Control-Byte Format

Bit 7 (MSB)	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**
Start	SEL2	SEL1	SEL0	RNG	BIP	PD1	PD0

Measurement	Select Reg.	Chan	Range	Conversion	Control Byte Binary	Control Byte Hex
CFEB1 3.3V	3	3	0-5 V	ADC*5/4096	10110001	B1
CFEB1 5V	3	4	0-10 V	ADC*10/4096	11001001	C9
CFEB1 6V	3	5	0-10 V	ADC*10/4096	11011001	D9
CFEB2 3.3V	3	6	0-5 V	ADC*5/4096	11100001	E1
CFEB2 5V	3	7	0-10 V	ADC*10/4096	11111001	F9
CFEB2 6V	4	0	0-10 V	ADC*10/4096	10001001	89
CFEB3 3.3V	4	1	0-5 V	ADC*5/4096	10010001	91
CFEB3 5V	4	2	0-10 V	ADC*10/4096	10101001	A9
CFEB3 6V	4	3	0-10 V	ADC*10/4096	10111001	B9
CFEB4 3.3V	4	4	0-5 V	ADC*5/4096	11000001	C1
CFEB4 5V	4	5	0-10 V	ADC*10/4096	11011001	D9
CFEB4 6V	4	6	0-10 V	ADC*10/4096	11101001	E9
CFEB5 3.3V	4	7	0-5 V	ADC*5/4096	11110001	F1
CFEB5 5V	5	0	0-10 V	ADC*10/4096	10001001	89
CFEB5 6V	5	1	0-10 V	ADC*10/4096	10011001	99
ALCT 3.3V	5	2	0-5 V	ADC*5/4096	10100001	A1
ALCT 1.8V	5	3	0-5 V	ADC*5/4096	10110001	B1
ALCT 5.5V B	5	4	0-10 V	ADC*10/4096	11001001	C9
ALCT 5.5V A	5	5	0-10 V	ADC*10/4096	11011001	D9
Analog Feed	5	6	0-10 V	ADC*10/4096	11101001	E9
Digital Feed	5	7	0-10 V	ADC*10/4096	11111001	F9

Control Byte Format for MAX1270/1271

(Taken from data sheet)

Control-Byte Format

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Start	SEL2	SEL1	SEL0	RNG	BIP	PD1	PD0

Table 2. Channel Selection

SEL2	SEL1	SEL0	Channel
0	0	0	Ch0
0	0	1	Ch1
0	1	0	Ch2
0	1	1	Ch3
1	0	0	Ch4
1	0	1	Ch5
1	1	0	Ch6
1	1	1	Ch7

Table 4. Power Down and Clock Selection

PD1	PD0	MODE
0	0	Normal Operation (always on), Internal Clock Mode
0	1	Normal Operation (always on), External Clock Mode
1	0	Standby Power-Down Mode (STBYPD), Clock Mode Unaffected
1	1	Full Power-Down Mode (FULLPD), Clock Mode Unaffected

Table 3. Range and Polarity Selection for MAX1270/MAX1271

MAX1270					
Input Range	**RNG**	**BIP**	**Negative Full Scale**	**Zero Scale (V)**	**Full Scale**
0 to 5 V	0	0	-	0	Vref * 1.2207
0 to 10 V	1	0	-	0	Vref * 2.4414
+/- 5 V	0	1	-Vref*1.2207	0	Vref * 1.2207
+/- 10 V	1	1	-Vref*2.4414	0	Vref * 2.4414
MAX1271					
Input Range	**RNG**	**BIP**	**Negative Full Scale**	**Zero Scale (V)**	**Full Scale**
0 to Vref/2	0	0	-	0	Vref/2
0 to Vref	1	0	-	0	Vref
+/- Vref/2	0	1	-Vref/2	0	Vref/2
+/- Vref	1	1	-Vref	0	Vref

Flash Memory for Buckeye Shifting

Address in Hex	R/W/Ex	Description
09000	Ex	Initialize the Programming Process
09004	W	Load Buckeye Pattern into FPGA Reg.
09008	Ex	Program Flash with Data in Register
0900C	R	Readback FPGA Register
09010	Ex	Write Buckeye's with Flash Content
09014	Ex	Erase Flash Memory
09018		
0901C		
09020		
09024		
09028		
0902C		
09030		
09034		
09038		
0903C		
09040		
09044		
09048		
0904C		
09050		
09054		
09058		
0905C		
09060		
09064		
09068		
0906C		
. . .		