DAQMBV

CMS CSC DAQ Motherboard VME interface FPGA

VME interface and Slow control

MBVME

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

12-3-2001_15:55

mojo

DAQMB VME interface FPGA Design

This FPGA do the slow control for CFEB and DAQMB by VME --> JTAG, or direct VME command

Modification history:

Nov. 27, 2000: Modification based on Dan's D741Z design, which convert VME to JTAG, add DAQMB specific functions

Nov. 29, 2000: Base structure of the Design is ready; Dec. 5, 2000: preliminary design passed APR

Feb. 2, 2001: Totally new scheme design on m:\wv\cmsdaqmb\daqmbv\ and Spartan-II

Feb. 28, 2001: Modify to be consistent with new COMMAND scheme

Apr. 9, 2001: Finished Modification, and pin Allocation according to DAQMB PCB Layout

Apr. 13, 2001: Ready for DAQMB debugging, 178 IOBs are used

July 24, 2001: Optimization based on the version1 design.

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174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Comment and Revision Information
DAQMB Controller
CMS CSC Electronics

BY: GU

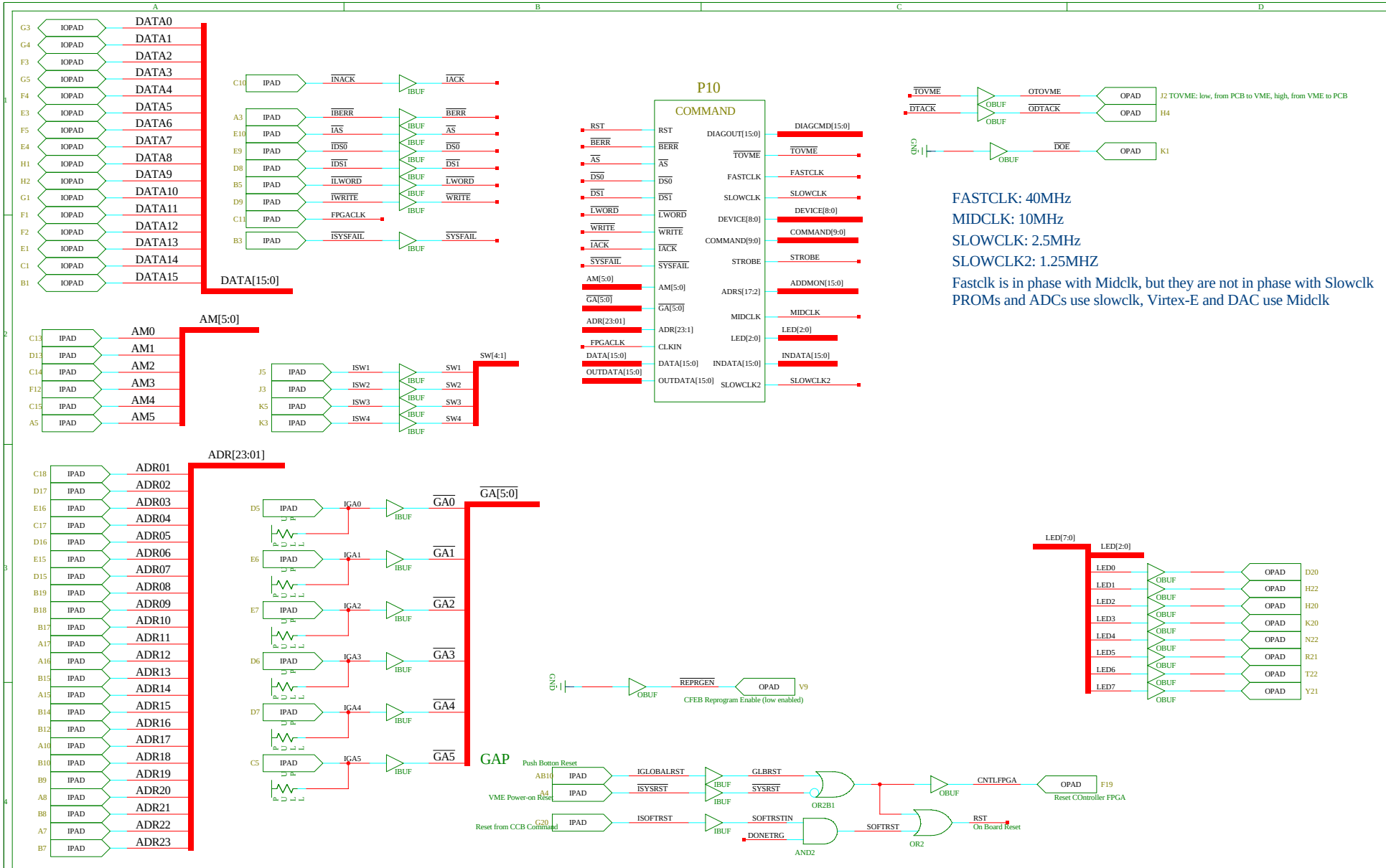
PARENT PAGE:

PROJECT: daqmbv

DATE: 7-24-2001_9:11

FILE: DAQMBV . 2

PAGE: 1A

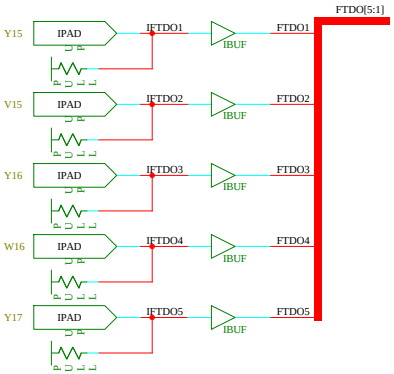


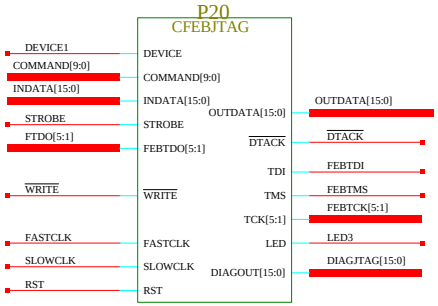
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Command Decoder DAQMB VME Interface CMS CSC Electronics	BY: GU PARENT PAGE: 1 DATE: 12-3-2001_15:55	PROJECT: DAQMBV FILE: MBVME . 1 PAGE: 2

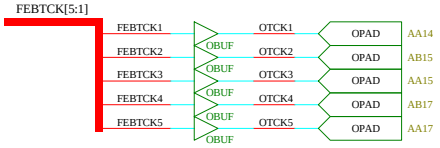
CFEB JTAG Clock: 1.25MHz, which is conrolled by ENABLE.

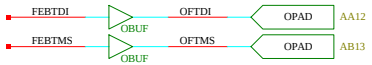
The DAC can work at 10MHz, FPGA can work at 33MHz, PROM can work at 10MHz, but it can only be Re-programmed at about 1.25MHz

The guess number for BUCKEYE is 5MHz



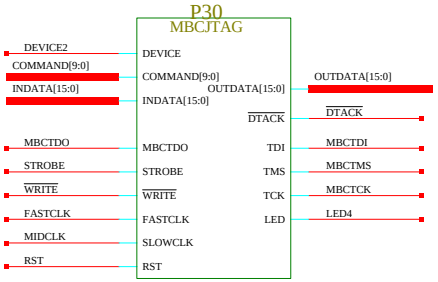


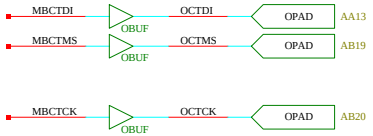




THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CFEB JTAG DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 1	PROJECT: DAQMBV
		DATE: 9-11-2001_12:56	FILE: MBVME . 2	PAGE: 2A

DAQMB Controller FPGA JTAG Clock: 10MHz, which is synchronized with MIDCLK
The FPGA can work at 33MHz, the Serial Flash Memory can work at 20MHz





THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DAQMB Controller FPGA and PROM JTAG DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 1	PROJECT: DAQMBV
		DATE: 9-11-2001_12:56	FILE: MBVME . 3	PAGE: 2B

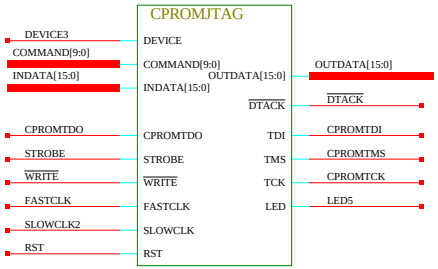
DAQMB ISPROMs' JTAG clock: 1.25MHz, half of SLOWCLK

The normal JTAG command can work at 10MHz, but for In_System_Programming, it must be slow, such as 1.25MHz

The ISP does not work at 2.5MHz or faster

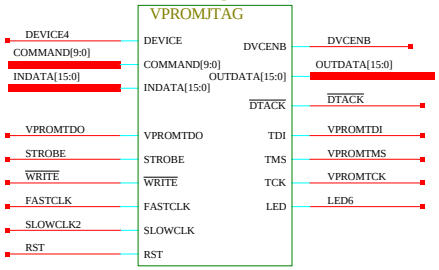
DAQMB Controller FPGA PROM

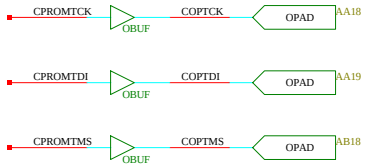
P40

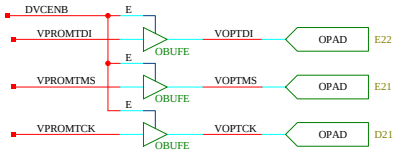


DAQMB VME Interface FPGA PROM

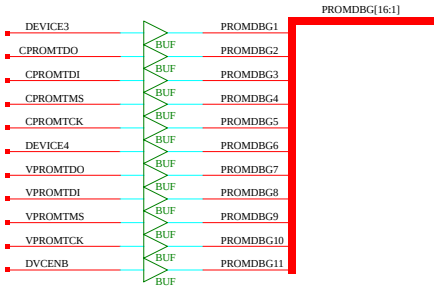
P45







Both FPGA and CPLD will drive VPROM's JTAG line, tri-state when not in use



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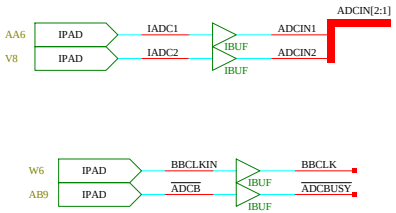
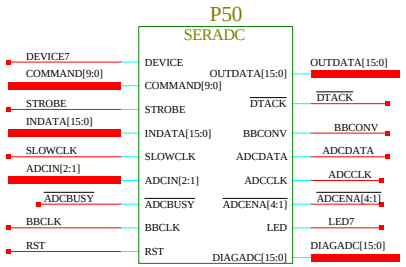
TITLE: DAQMB PROMs' JTAGs
DAQMB VME Interface
CMS CSC Electronics

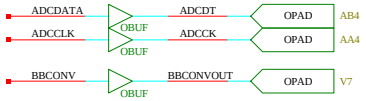
BY	PARENT PAGE	PROJECT
GU	1	DAQMBV
DATE	FILE	PAGE
10-12-2001_10:11	MBVME . 4	2C

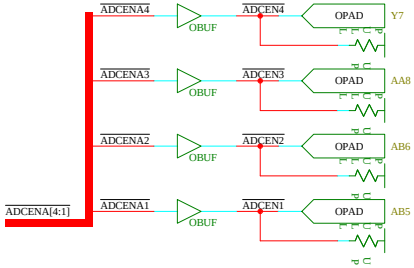
Serial ADC (MAX1270/1271) Interface clock: 1.25MHz, Divided SLOWCLOCK is used

The ADC1270/1271 can work at a frequency from 0.1MHz to 2.0MHz





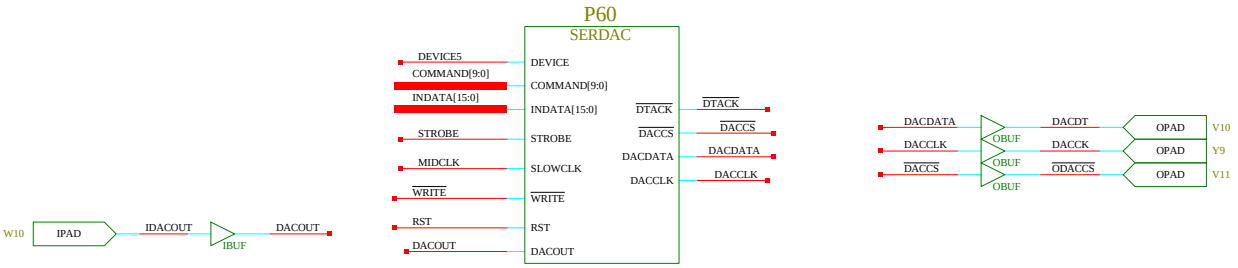




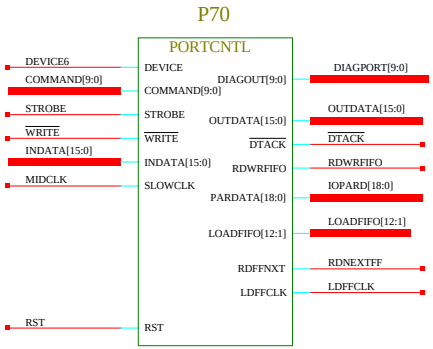
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Serial ADCs DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 1	PROJECT: DAQMBV
		DATE: 9-13-2001_7:56	FILE: MBVME . 5	PAGE: 2D

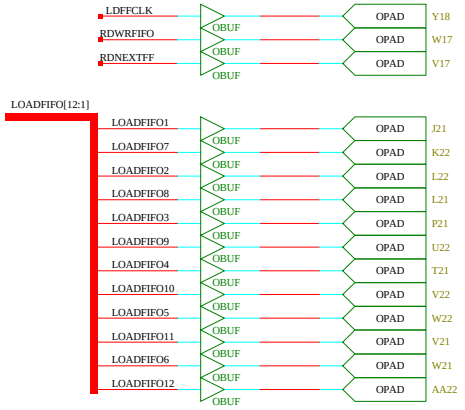
Serial DAC (MAX5154/5155) interface clock: 5MHz

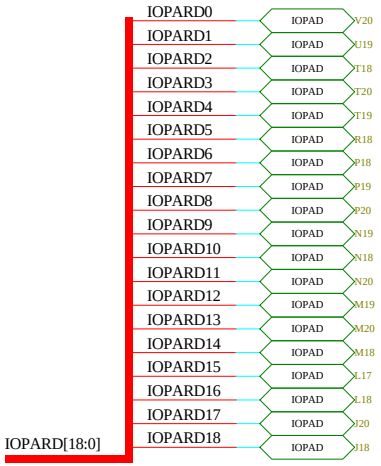
The MAX 5154/5155 requires the minimum clock period is 100ns.



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Serial DAC control DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 1	PROJECT: DAQMBV
		DATE: 9-11-2001_12:56	FILE: MBVME . 6	PAGE: 2E







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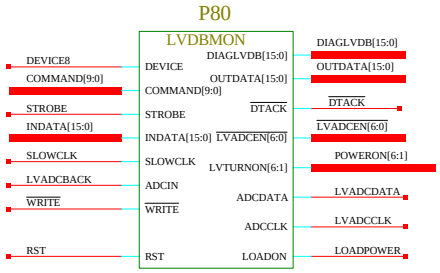
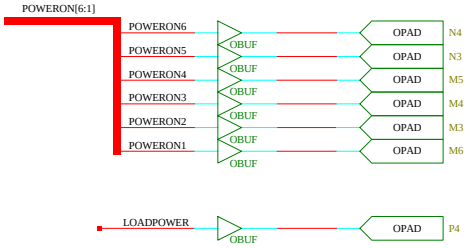
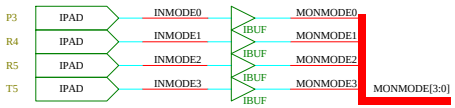
TITLE: Parallel Loading/Reading FIFO control
DAQMB VME Interface
CMS CSC Electronics

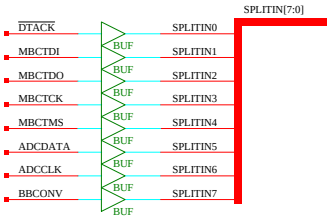
BY	PARENT PAGE	PROJECT	
GU	1	DAQMBV	
DATE		FILE	PAGE
9-13-2001_7:57		MBVME . 7	2F



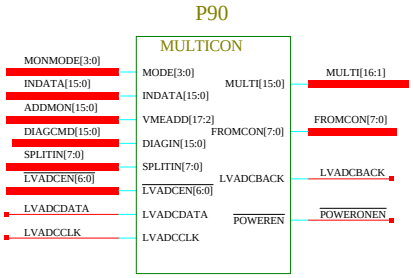


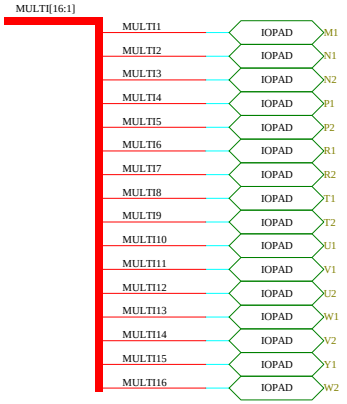
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Serial DAC DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 1	PROJECT: DAQMBV
		DATE: 9-11-2001_12:56	FILE: MBVME . 8	PAGE: 2G

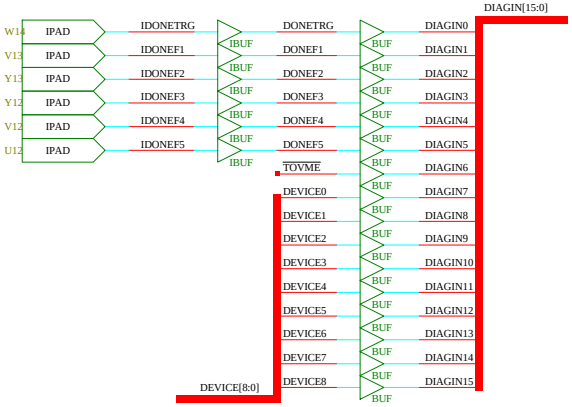


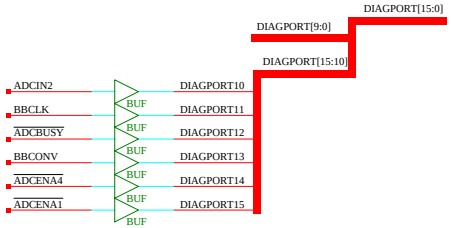


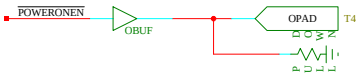
Multi-fuction Connector Control



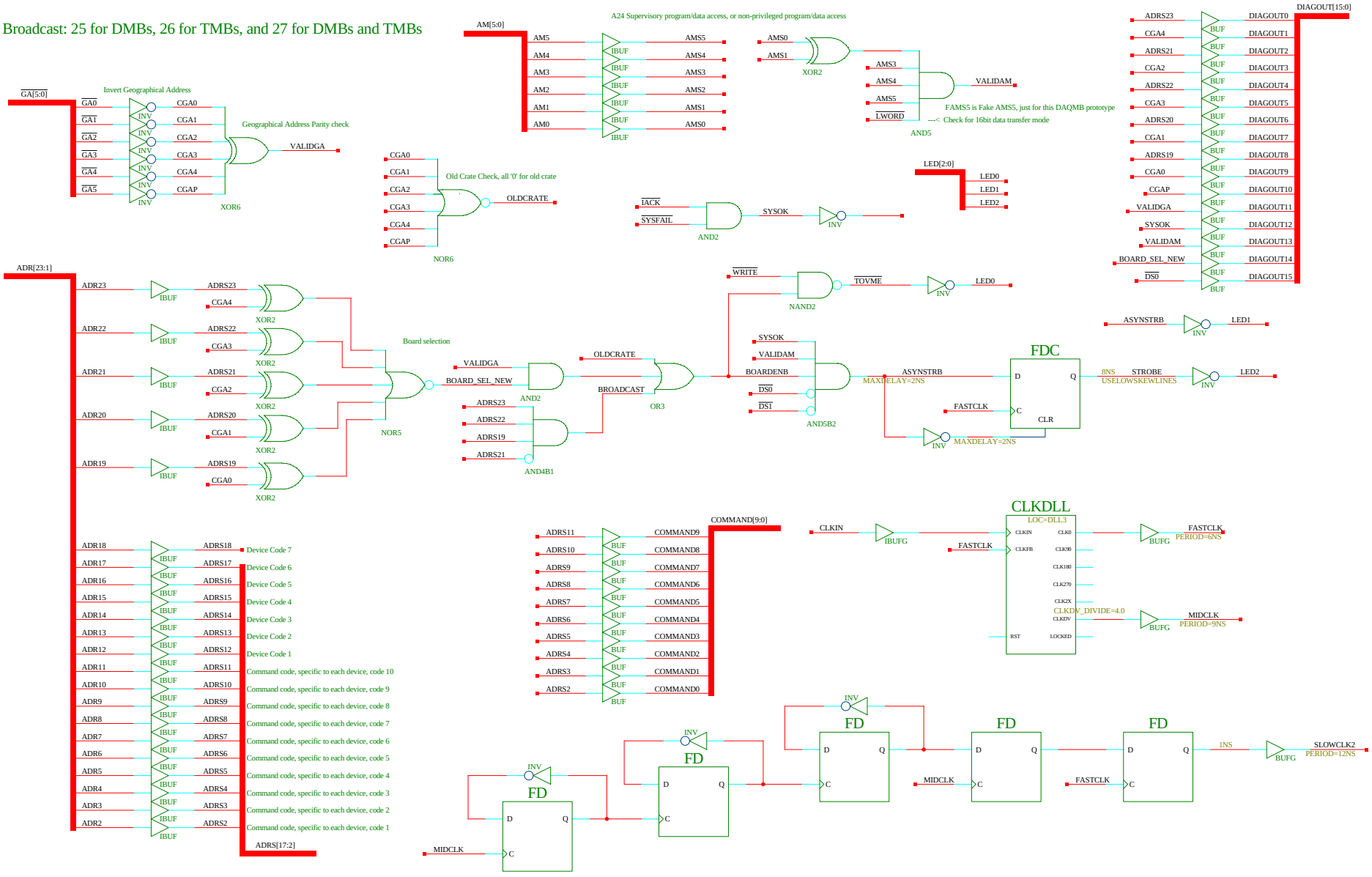






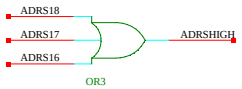


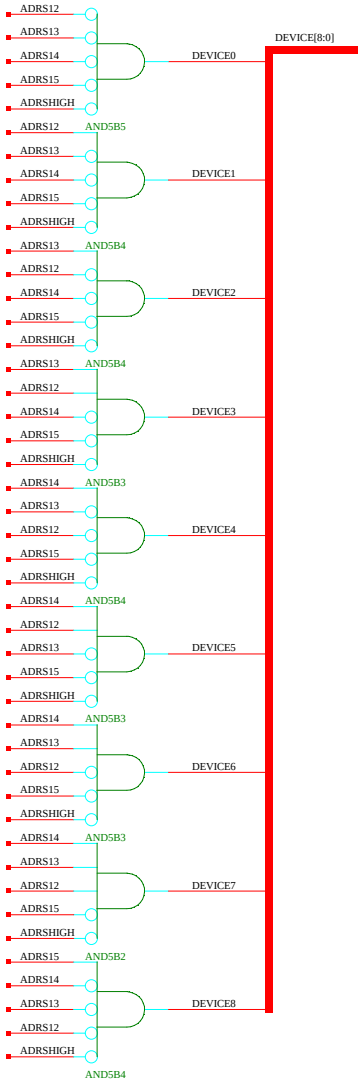
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Multi-function Connector interface DAQMB VME Interface CMS CSC Electronics	BY: GU PARENT PAGE: 1 PROJECT: DAQMBV DATE: 12-3-2001_15:55 FILE: MBVME . 9 PAGE: 2H	



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Address Decoder DAQMB VME Interface CMS CSC Electronics	BY: GU PARENT PAGE: 2 DATE: 3-1-2002_15:29	PROJECT: DAQMBV FILE: COMMAND . 1 PAGE: 10

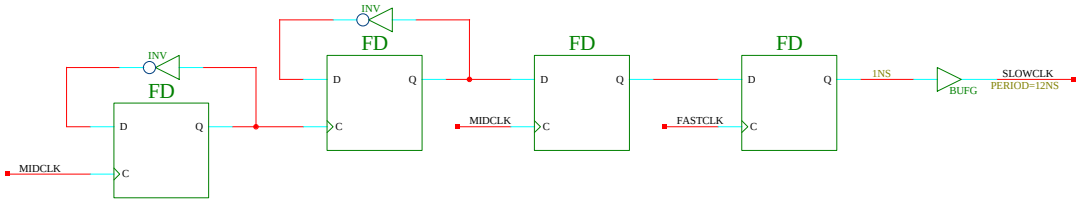
Device Selection





Device code:

00 || VME Interface FPGA
01 || CFEB JTAG
02 || DAQMB Controller FPGA JTAG
03 || DAQMB Controller PROM JTAG
04 || VME Interface PROM JTAG
05 || Dual DAC for Calibration
06 || FIFO Read/Write
07 || DAQMB ADC Interface
08 || Low Voltage Monitoring Interface
0F || Emergency PROM Programming, Reserved for Emergency CPLD



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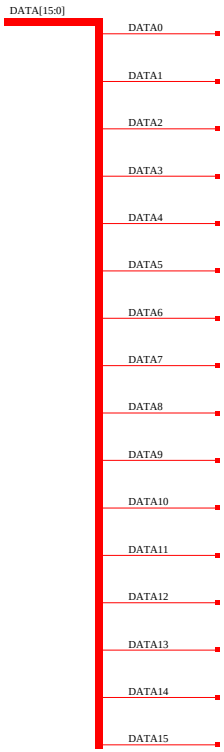
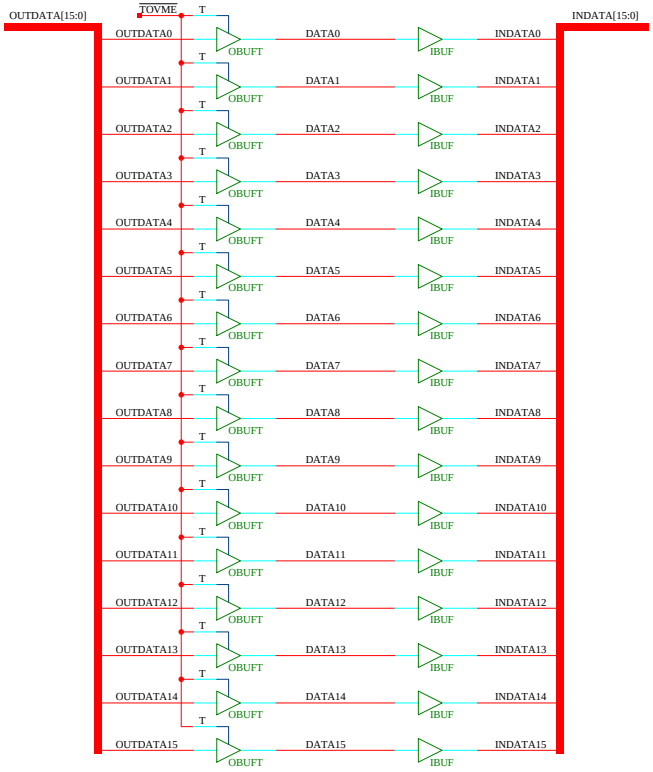
TITLE: Read Command Decoder
DAQMB VME Interface
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
GU	2	DAQMBV
DATE	FILE	PAGE
10-16-2001_12:02	COMMAND . 2	10A





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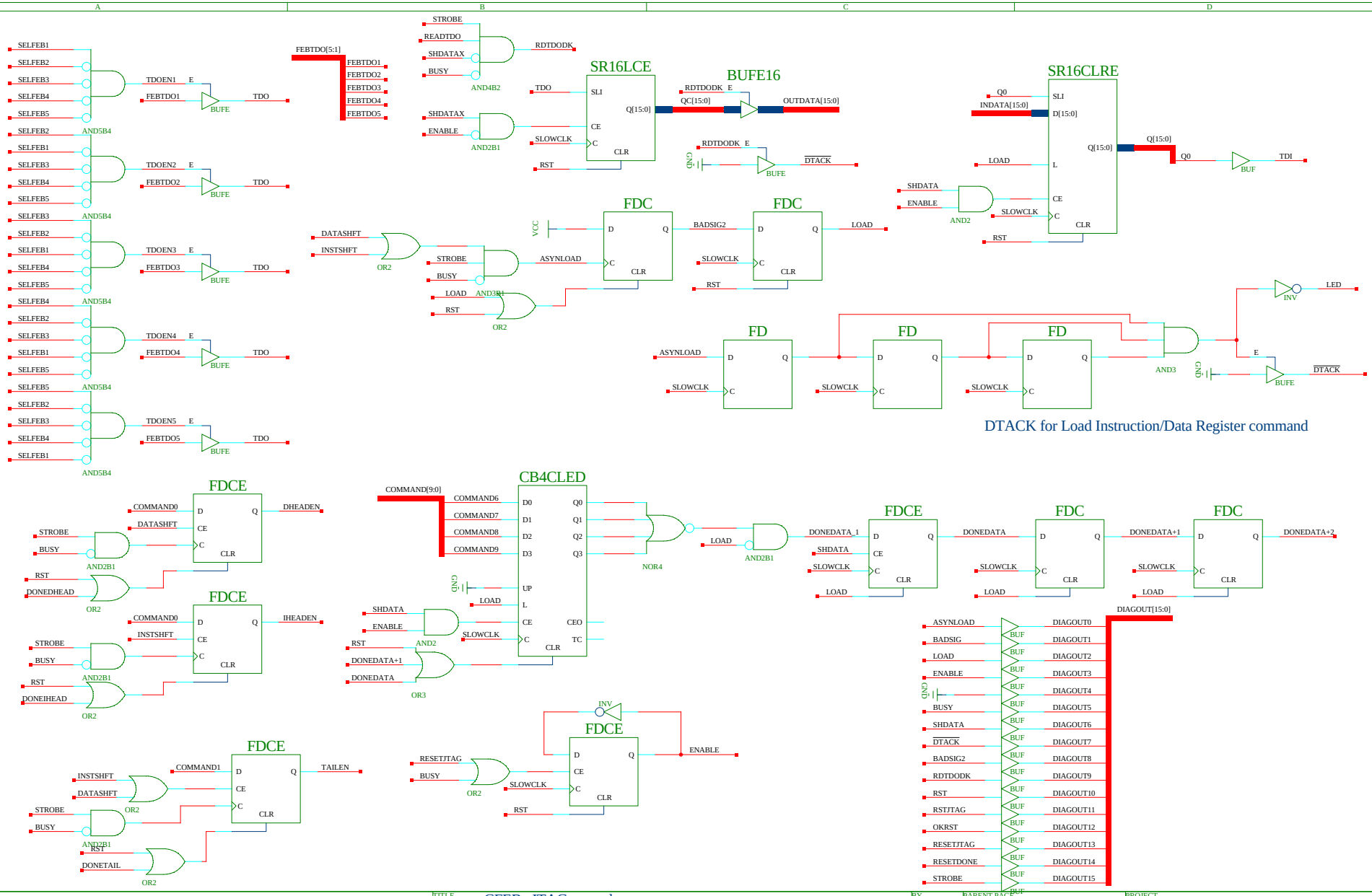
TITLE: Write Command Decoder
DAQMB VME Interface
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
GU	2	DAQMBV
DATE		FILE / PAGE
10-4-2001_14:11		COMMAND . 3 / 10B



DTACK for Load Instruction/Data Register command

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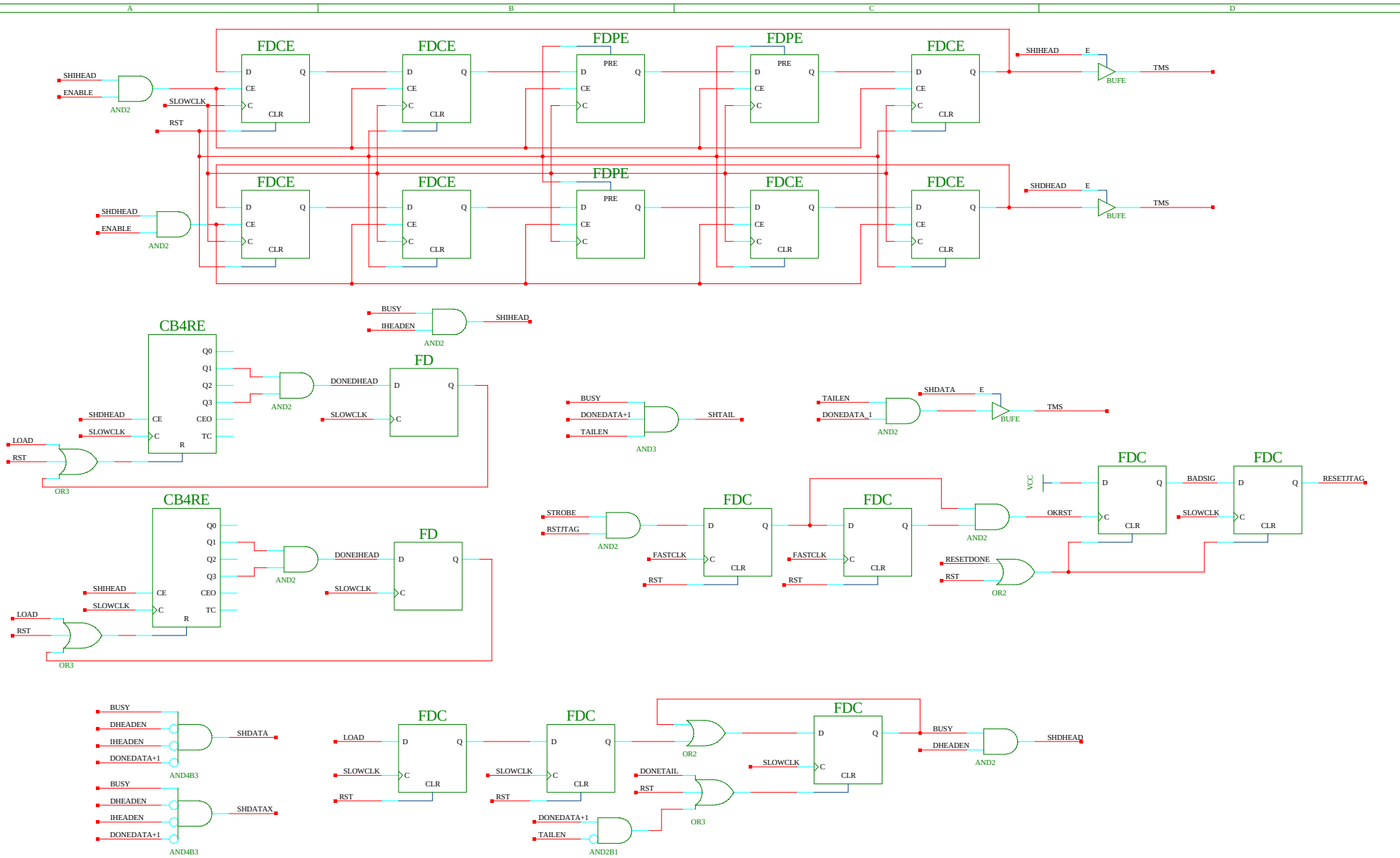
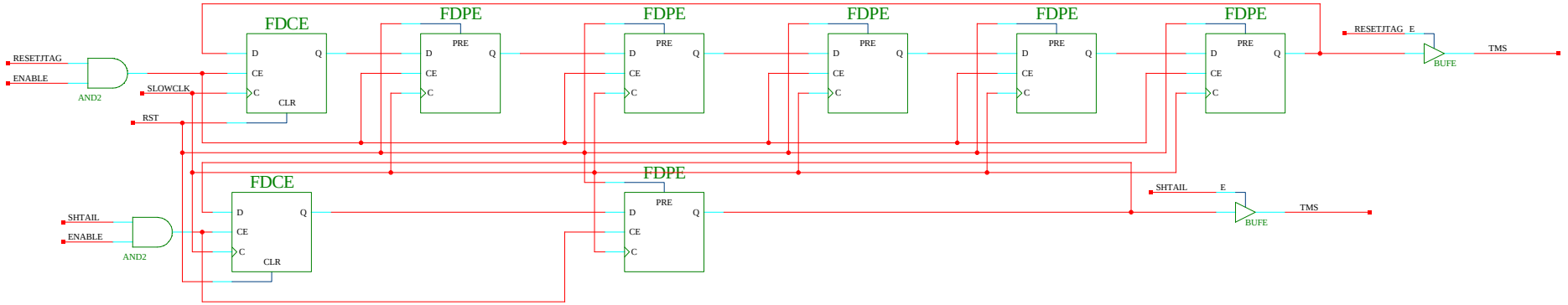
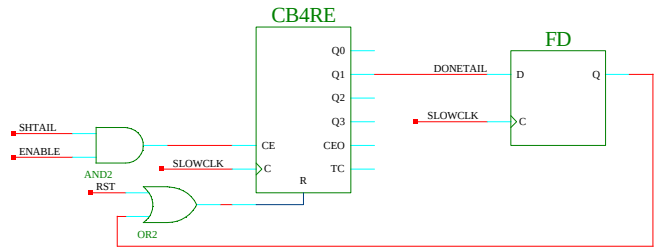
TITLE: CFEBs JTAG control
DAQMB VME Interface
CMS CSC Electronics

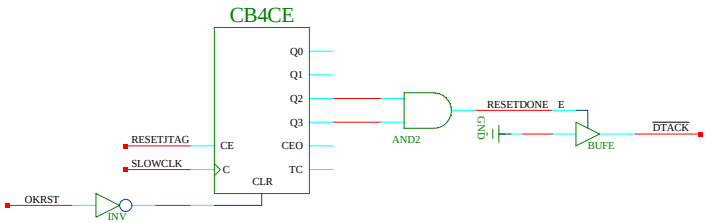
BY	PARENT PAGE	PROJECT
GU	2A	DAQMBV
DATE	FILE	PAGE
7-24-2001_9:13	CFEBJTAG . 1	20



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CFEBs JTAG control DAQMB VME Interface CMS CSC Electronics	BY: GU DATE: 10-4-2001_14:11	PARENT PAGE: 2A FILE: CFEBJTAG . 2
		PROJECT: DAQMBV	PAGE: 20A

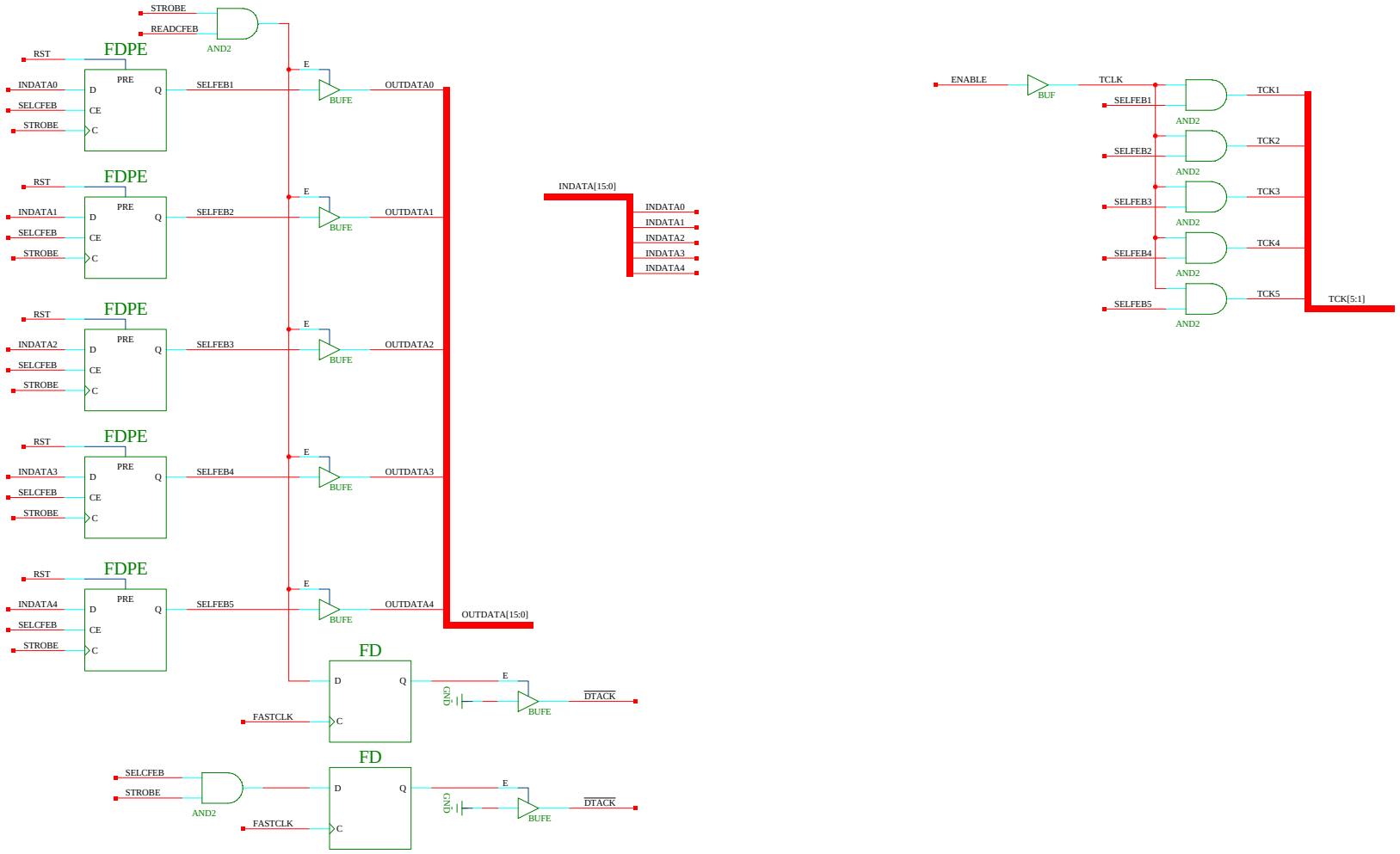






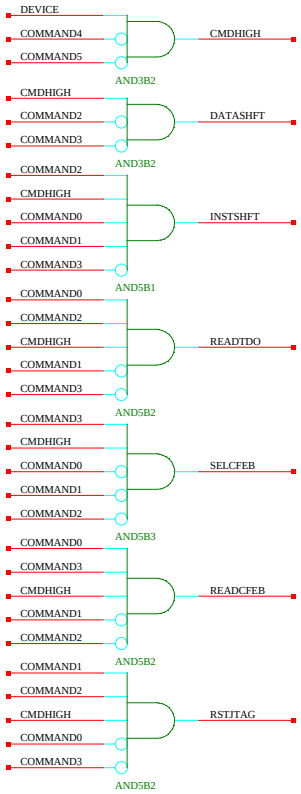
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CFEBs JTAG control DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2A	PROJECT: DAQMBV
		DATE: 8-29-2001_13:53	FILE: CFEBJTAG . 3	PAGE: 20B

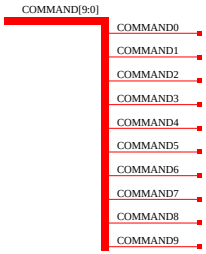
CFEB Selection and Readback logic



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: CFEBs JTAG control DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2A	PROJECT: DAQMBV
		DATE: 8-29-2001_14:03	FILE: CFEBJTAG . 4	PAGE: 20C

CFEB JTAG command decode





CFEB JTAG commands:

- 00 || Shift data, no header, no tailer
- 01 || Shift data with header only
- 02 || Shift data with tailer only
- 03 || Shift data with header and tailer
- 04 ||
- 05 || Read TDO register
- 06 || Reset JTAG State machine
- 07 || Shift Instruction register
- 08 || Write CFEB Select Register
- 09 || Read CFEB Select Register

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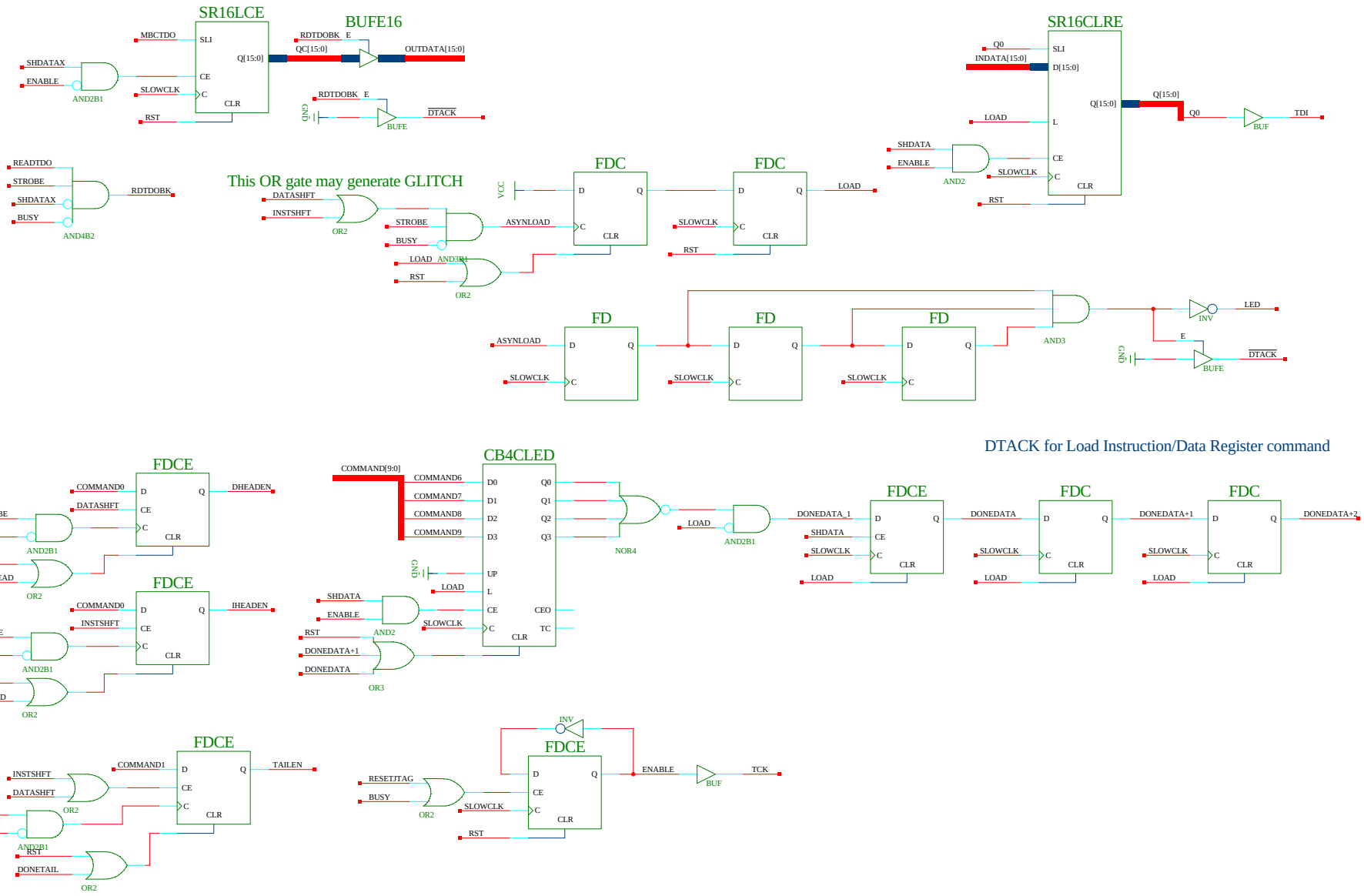
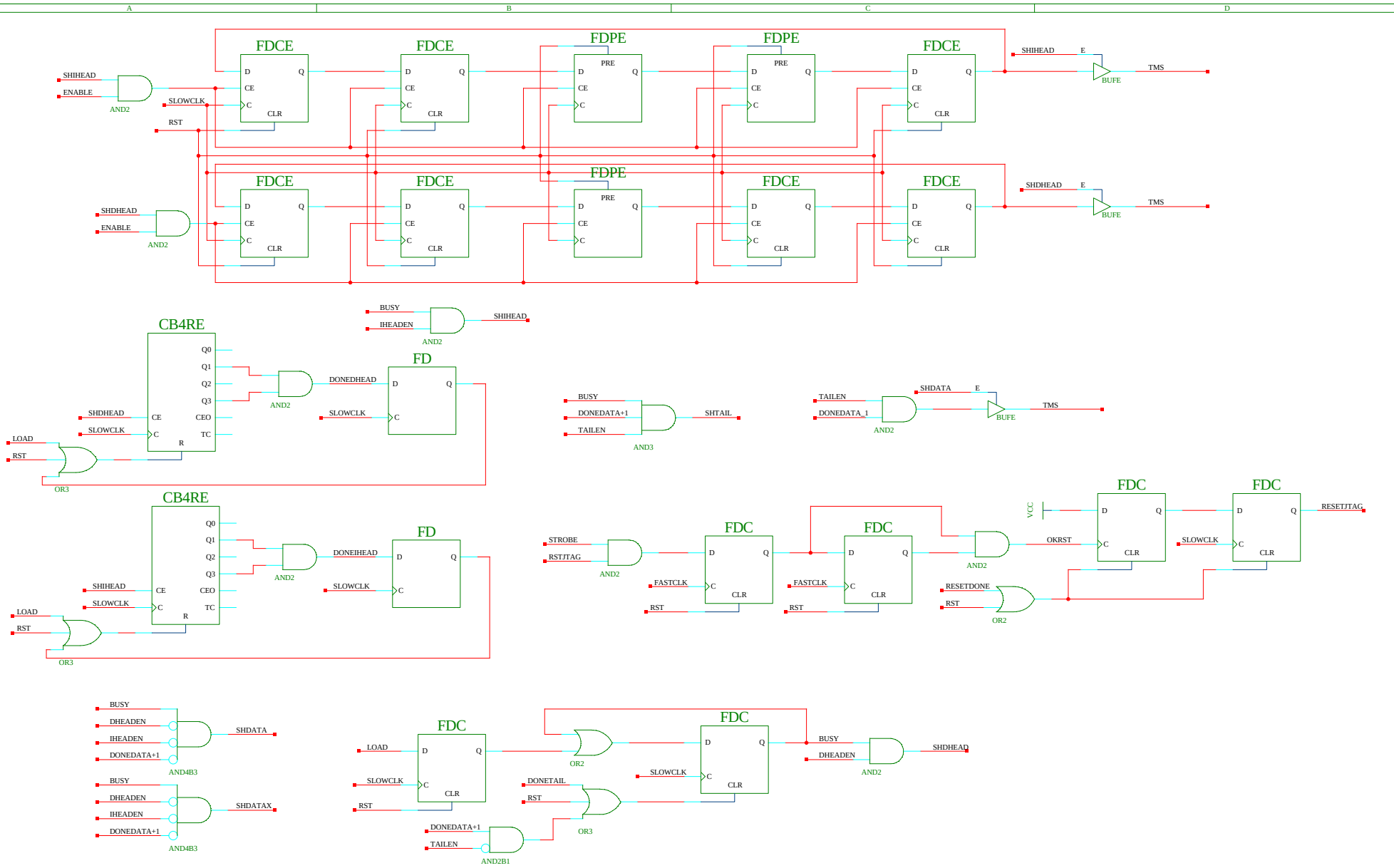
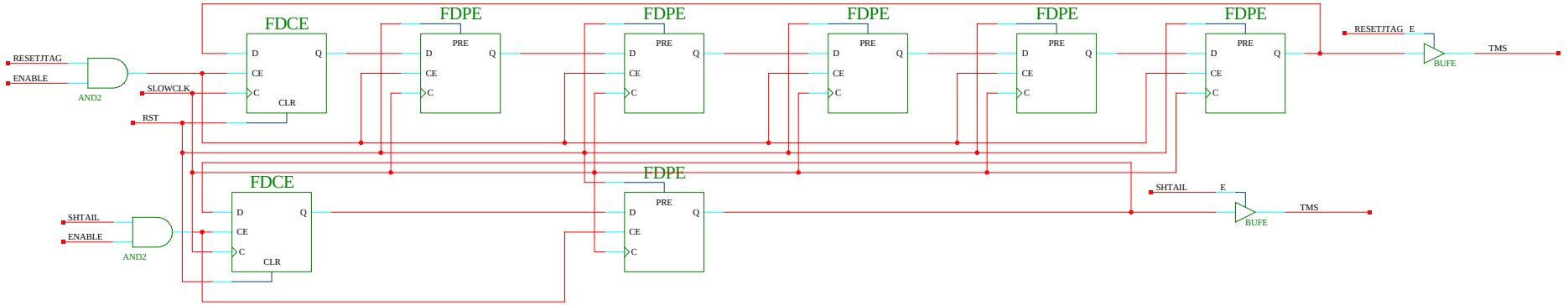
TITLE	CFEBs JTAG Command decoder DAQMB VME Interface CMS CSC Electronics
BY	GU
PARENT PAGE	2A
PROJECT	DAQMBV
DATE	5-3-2001_9:00
FILE	CFEBJTAG . 5
PAGE	20D

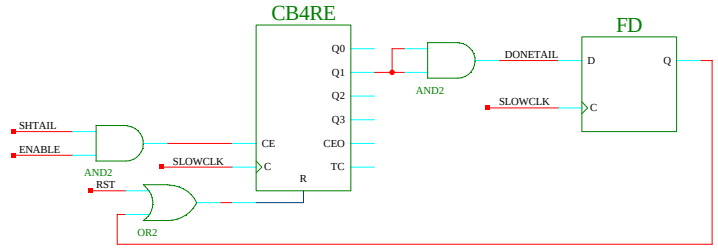


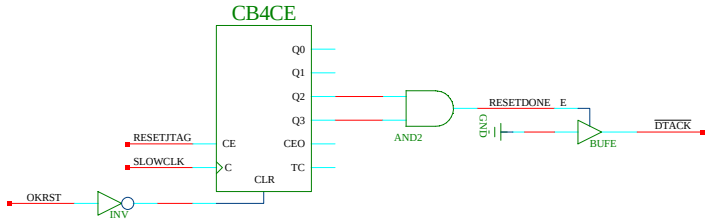
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DAQMB Cntroller FPGA JTAG control DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2B	PROJECT: DAQMBV
		DATE: 10-4-2001_12:35	FILE: MBCJTAG . 1	PAGE: 30



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DAQMB Control FPGA JTAG Header/Tailer DAQMB VME Interface CMS CSC Electronics	BY: GU DATE: 7-24-2001_9:19	PARENT PAGE: 2B FILE: MBCJTAG . 2
		PROJECT: DAQMBV	PAGE: 30A

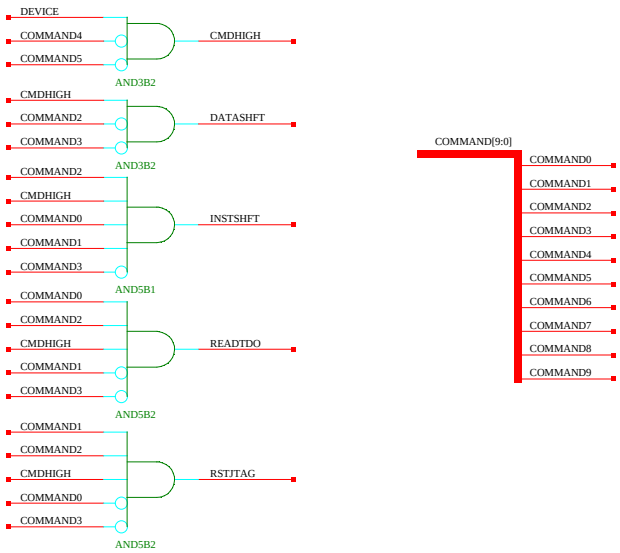






THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Controller FPGA JTAG Control DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2B	PROJECT: DAQMBV
		DATE: 5-3-2001_9:41	FILE: MBCJTAG . 3	PAGE: 30B

CFEB JTAG command decode



CFEB JTAG commands:

- 00 || Shift data, no header, no tailer
- 01 || Shift data with header only
- 02 || Shift data with tailer only
- 03 || Shift data with header and tailer
- 04 ||
- 05 || Read TDO register
- 06 || Reset JTAG State machine
- 07 || Shift Instruction register

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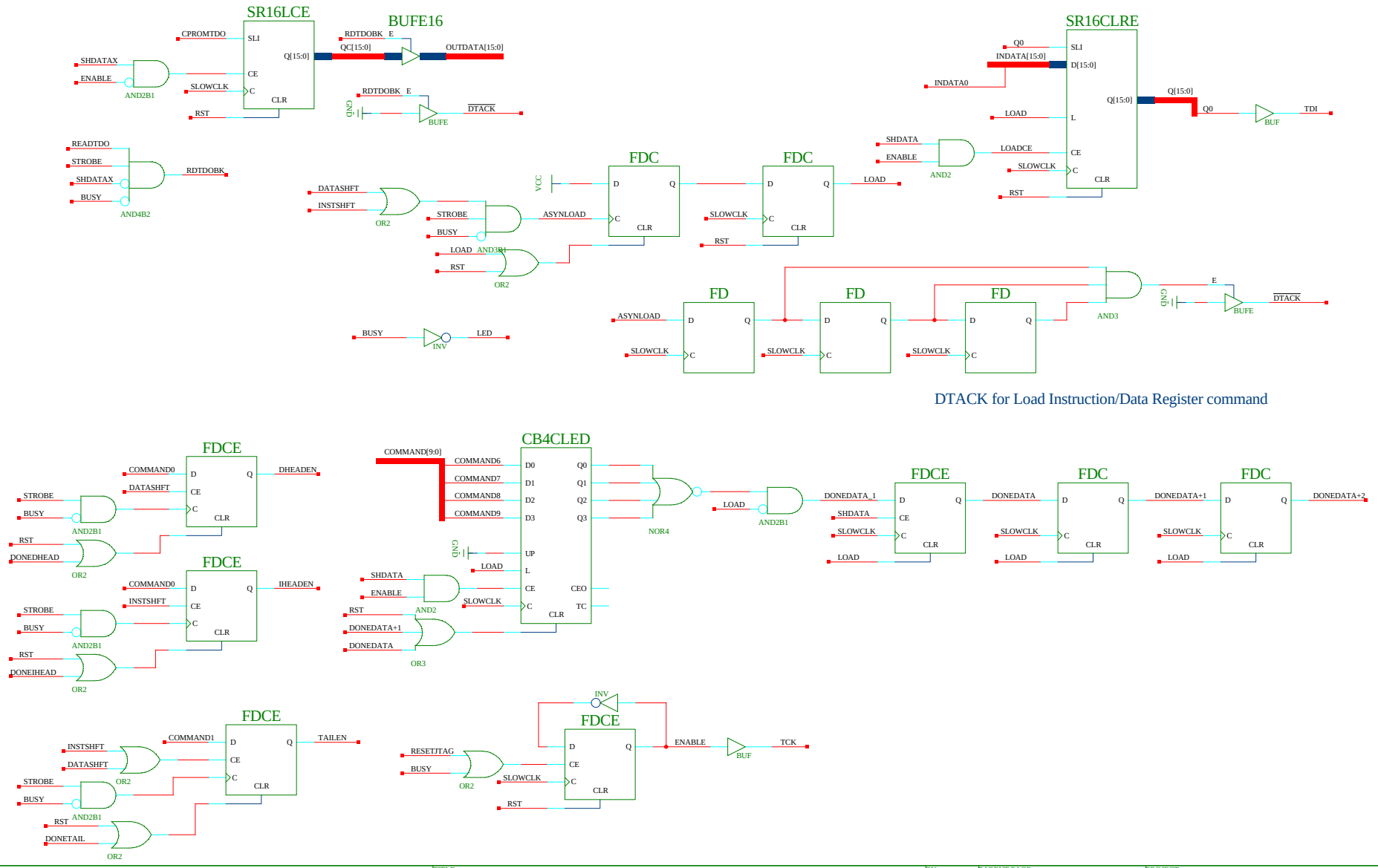
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: DAQMB Control FPGA JTAG command Decoder
DAQMB VME Interface
CMS CSC Electronics

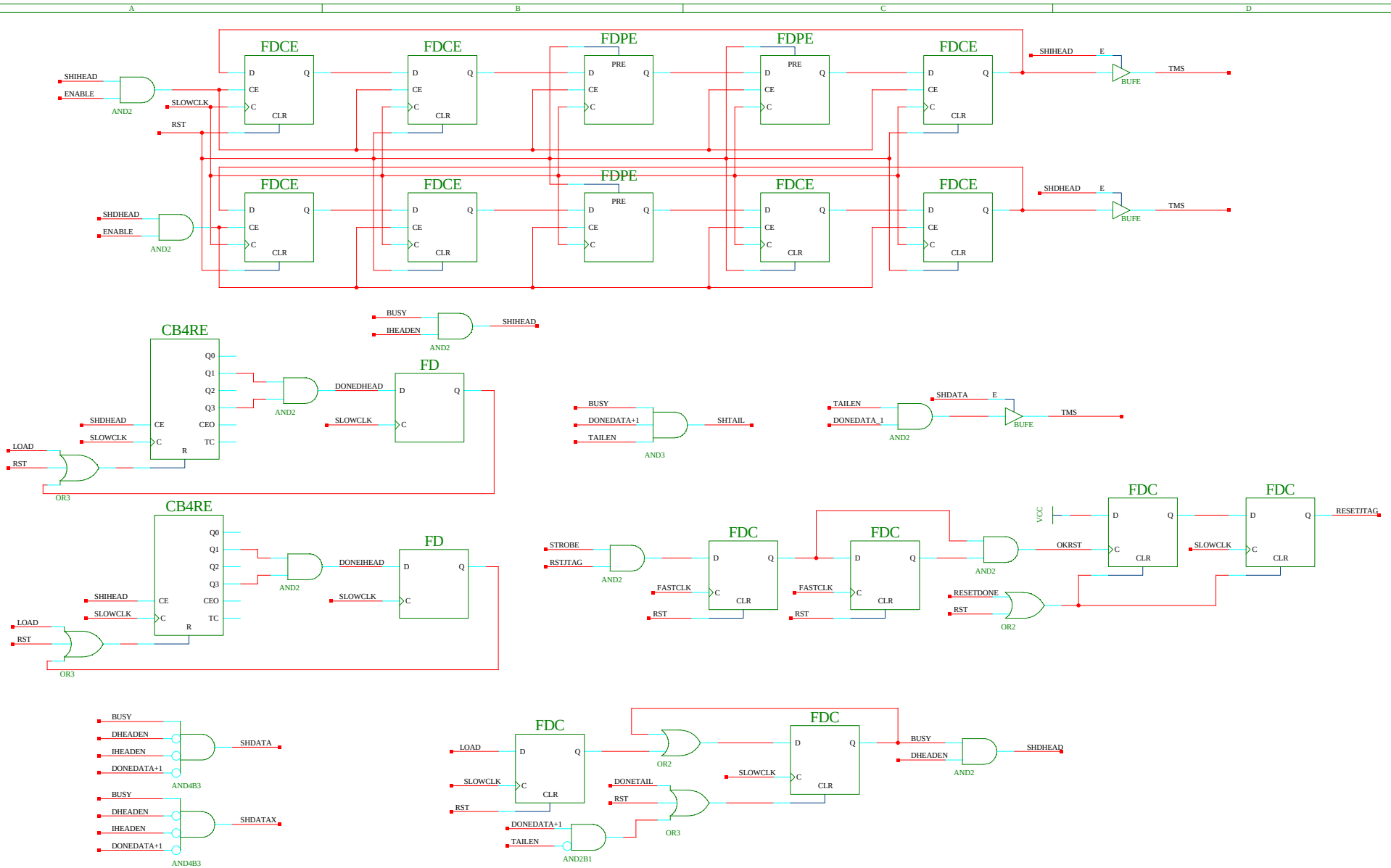
BY	PARENT PAGE	PROJECT
GU	2B	DAQMBV

DATE	FILE	PAGE
5-3-2001_9:41	MBCJTAG . 4	30C

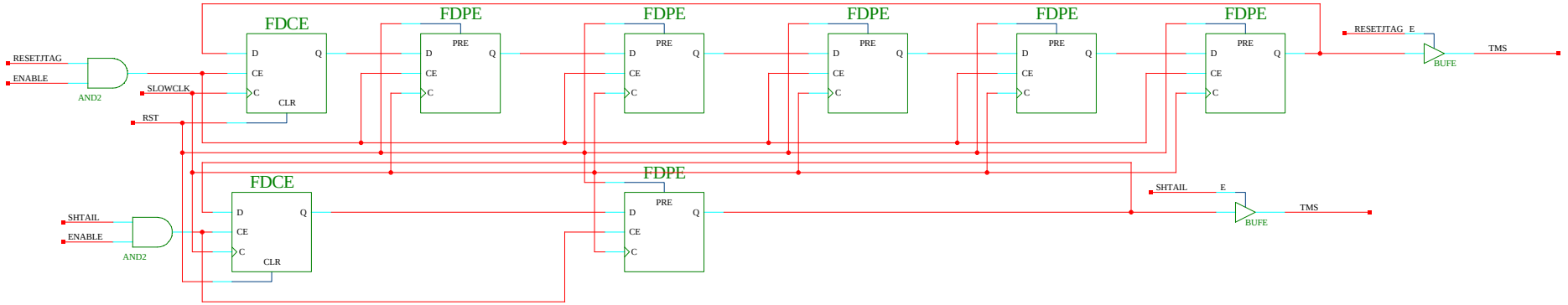


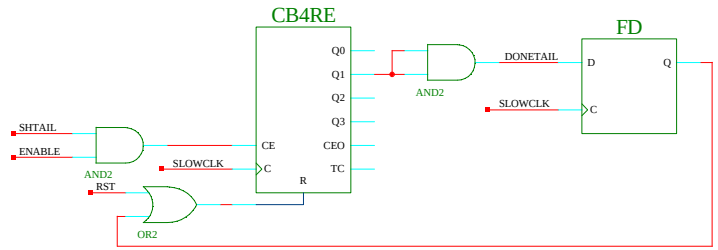
DTACK for Load Instruction/Data Register command

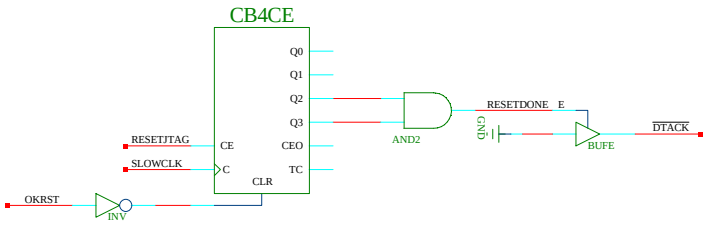
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DAQMB Cntroller FPGA's PROM JTAG control DAQMB VME Interface CMS CSC Electronics	BY: GU DATE: 7-25-2001_10:55	PARENT PAGE: 2C FILE: CPROMJTAG . 1
		PROJECT: DAQMBV	PAGE: 40



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DAQMB Control FPGA's PROM JTAG Header/Tailer DAQMB VME Interface CMS CSC Electronics	BY: GU PARENT PAGE: 2C PROJECT: DAQMBV DATE: 7-24-2001_9:25 FILE: CPROMJTAG . 2 PAGE: 40A	

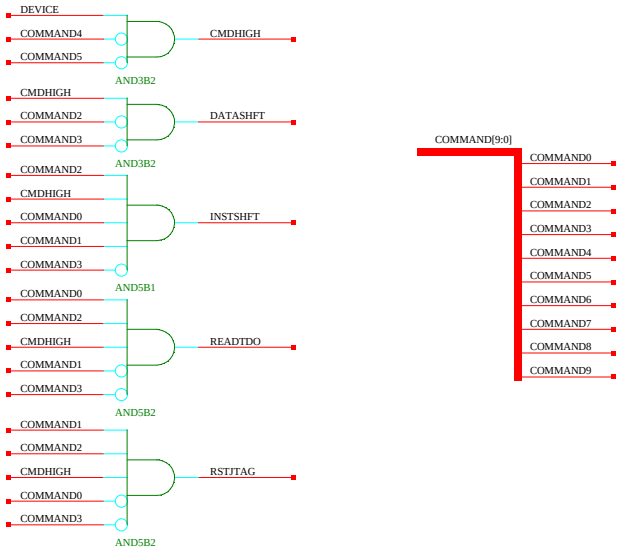






THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Controller FPGA's PROM JTAG DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2C	PROJECT: DAQMBV
		DATE: 7-24-2001_9:22	FILE: CPROMJTAG . 3	PAGE: 40B

CFEB JTAG command decode



CFEB JTAG commands:

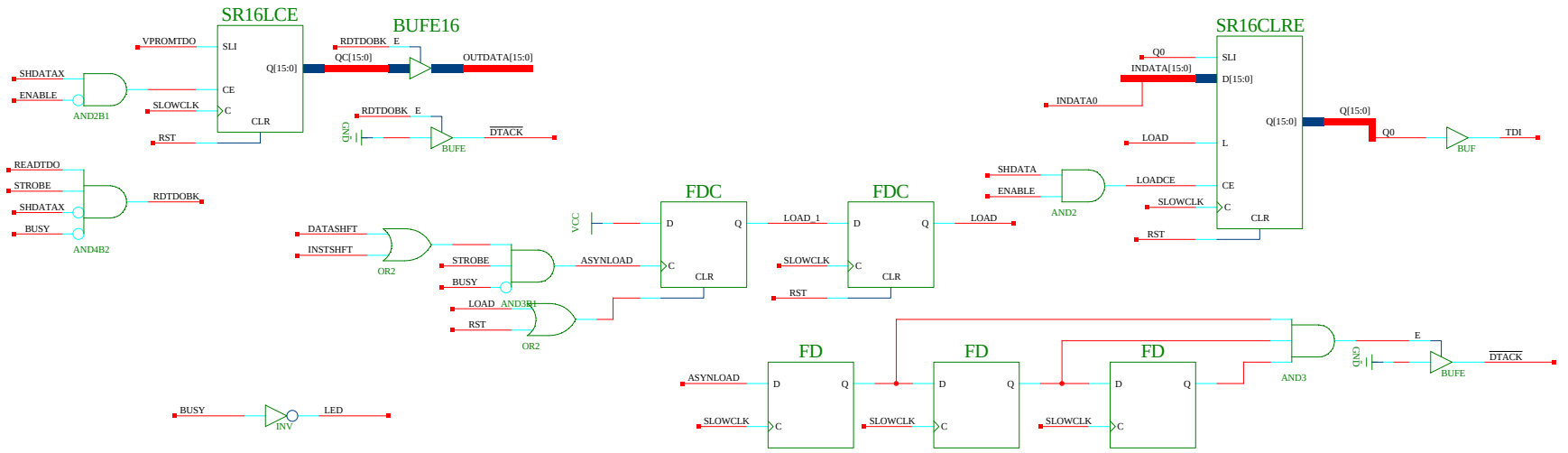
- 00 || Shift data, no header, no tailer
- 01 || Shift data with header only
- 02 || Shift data with tailer only
- 03 || Shift data with header and tailer
- 04 ||
- 05 || Read TDO register
- 06 || Reset JTAG State machine
- 07 || Shift Instruction register

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

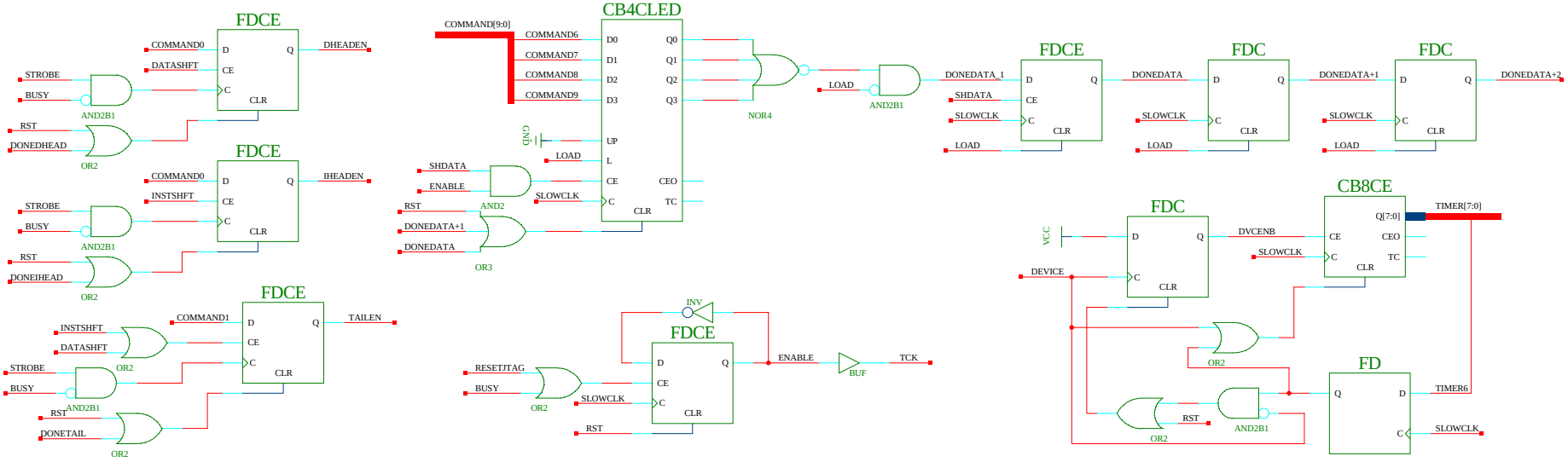
TITLE: DAQMB Control FPGA's PROM JTAG command Decoder
DAQMB VME Interface
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
GU	2C	DAQMBV

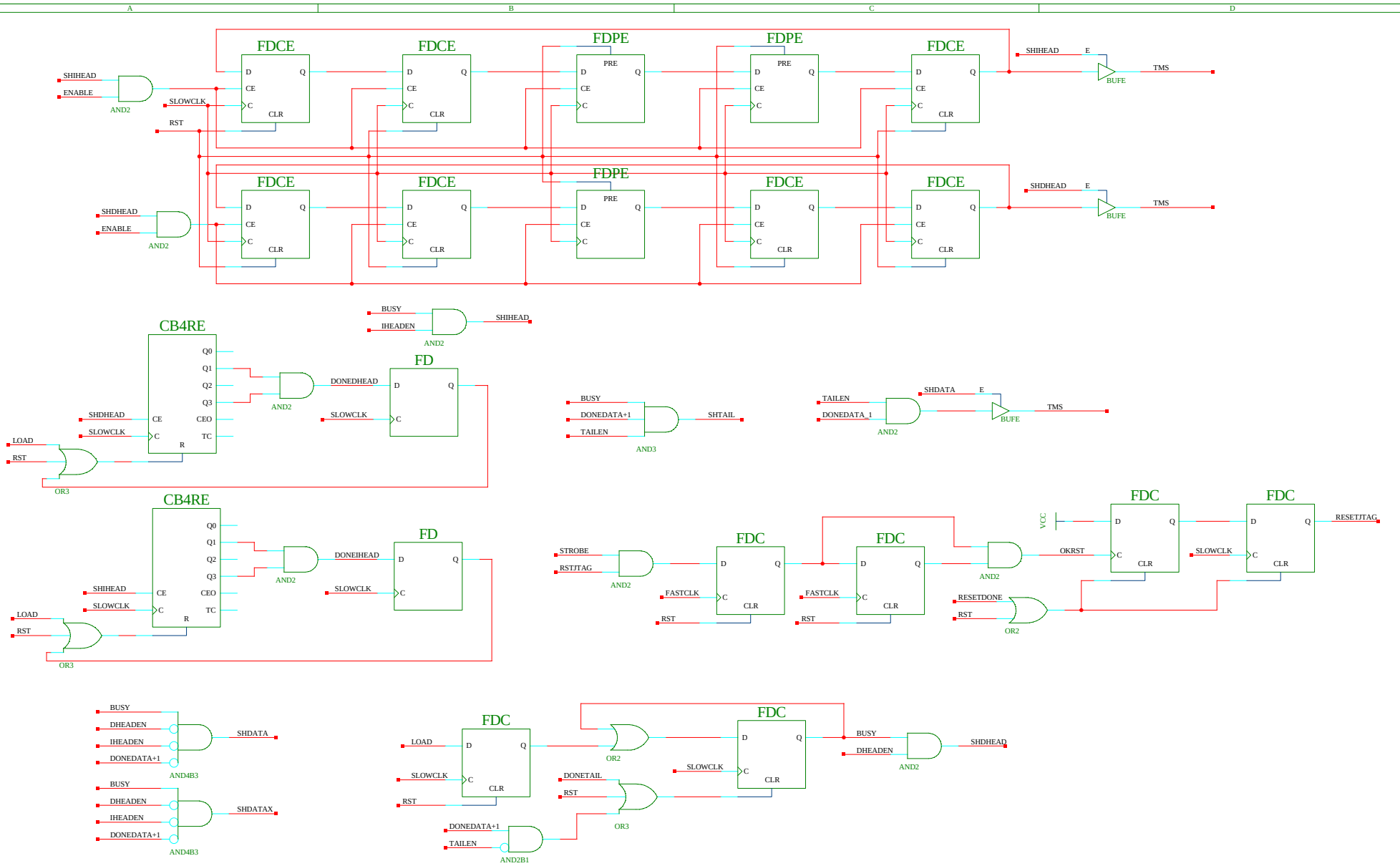
DATE	FILE	PAGE
5-18-2001_10:34	CPROMJTAG . 4	40C



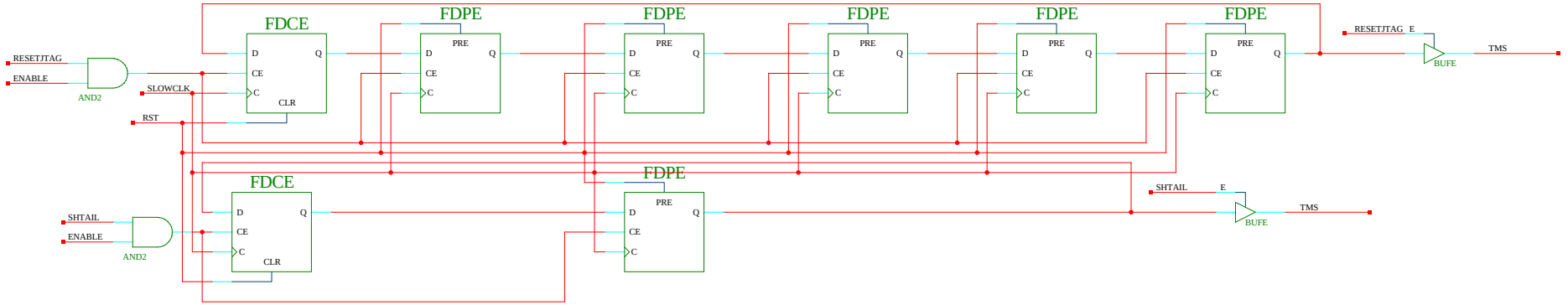
DTACK for Load Instruction/Data Register command

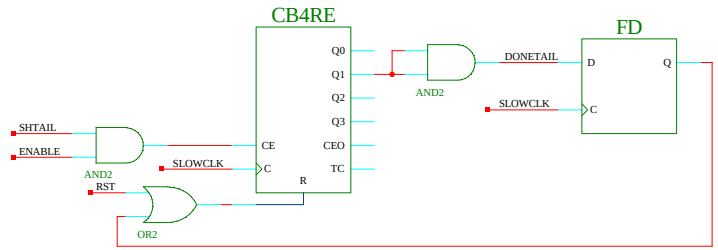


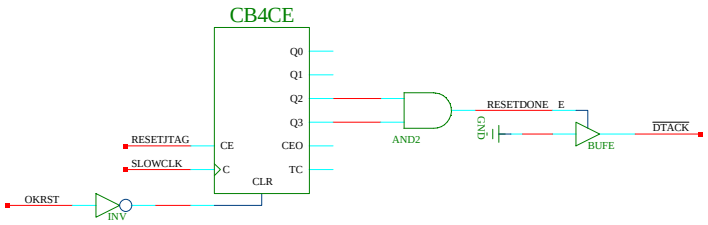
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DAQMB VME Interface FPGA's PROM JTAG control DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2C	PROJECT: DAQMBV
		DATE: 7-25-2001_15:41	FILE: VPROMJTAG . 1	PAGE: 45



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: DAQMB VME Interface FPGA's PROM JTAG Header/Tailer DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2C	PROJECT: DAQMBV
		DATE: 7-24-2001_9:28	FILE: VPROMJTAG . 2	PAGE: 45A

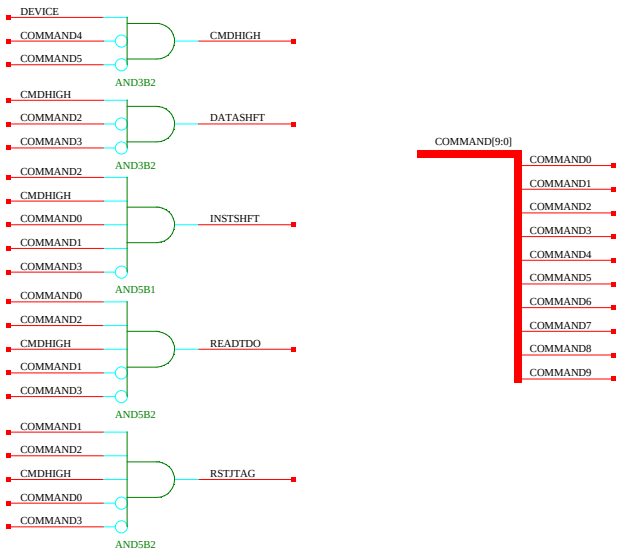






THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: VME Interface FPGA's PROM JTAG DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2C	PROJECT: DAQMBV
		DATE: 5-3-2001_9:43	FILE: VPROMJTAG . 3	PAGE: 45B

CFEB JTAG command decode

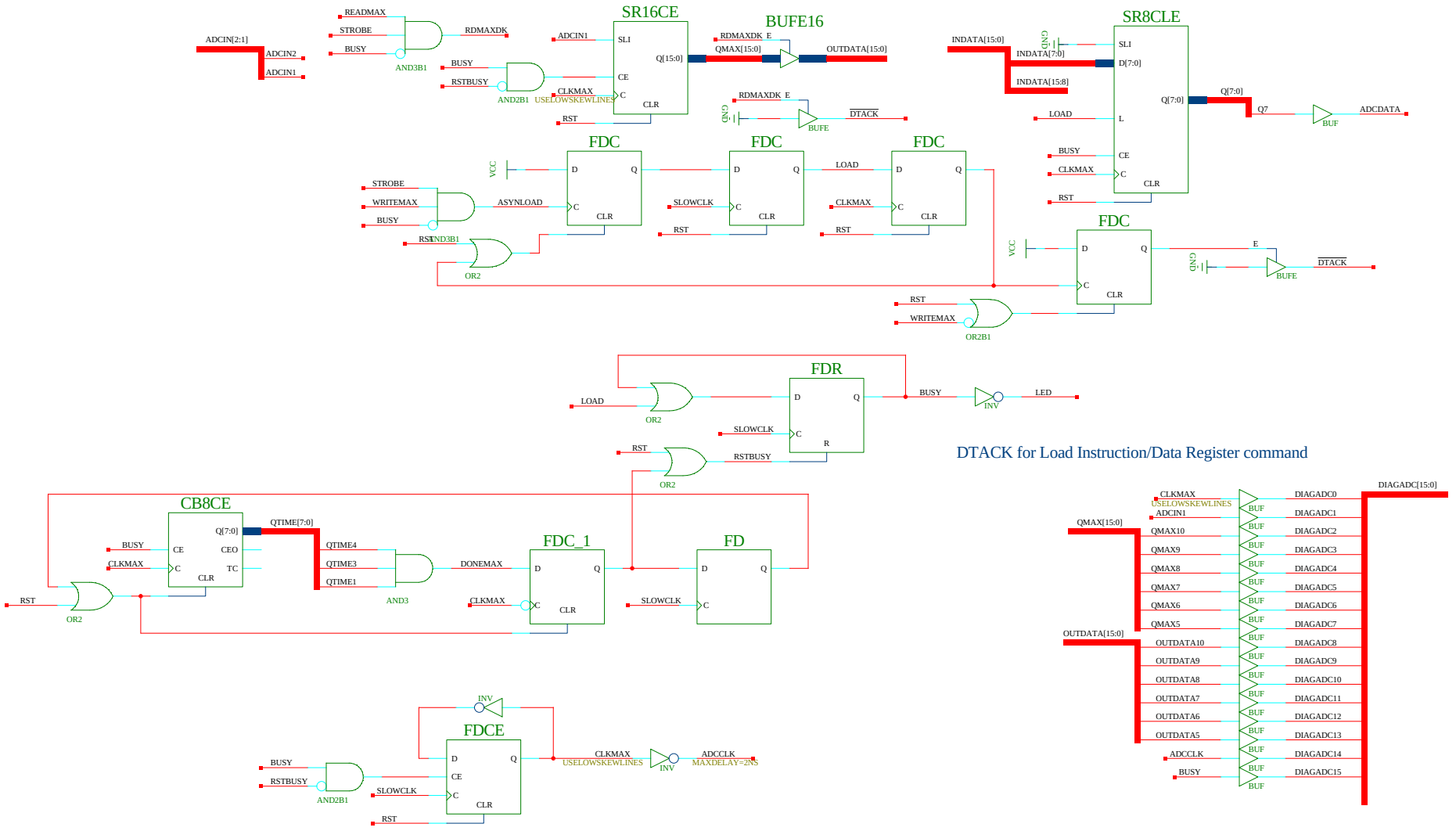


CFEB JTAG commands:

- 00 || Shift data, no header, no tailer
- 01 || Shift data with header only
- 02 || Shift data with tailer only
- 03 || Shift data with header and tailer
- 04 ||
- 05 || Read TDO register
- 06 || Reset JTAG State machine
- 07 || Shift Instruction register

THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

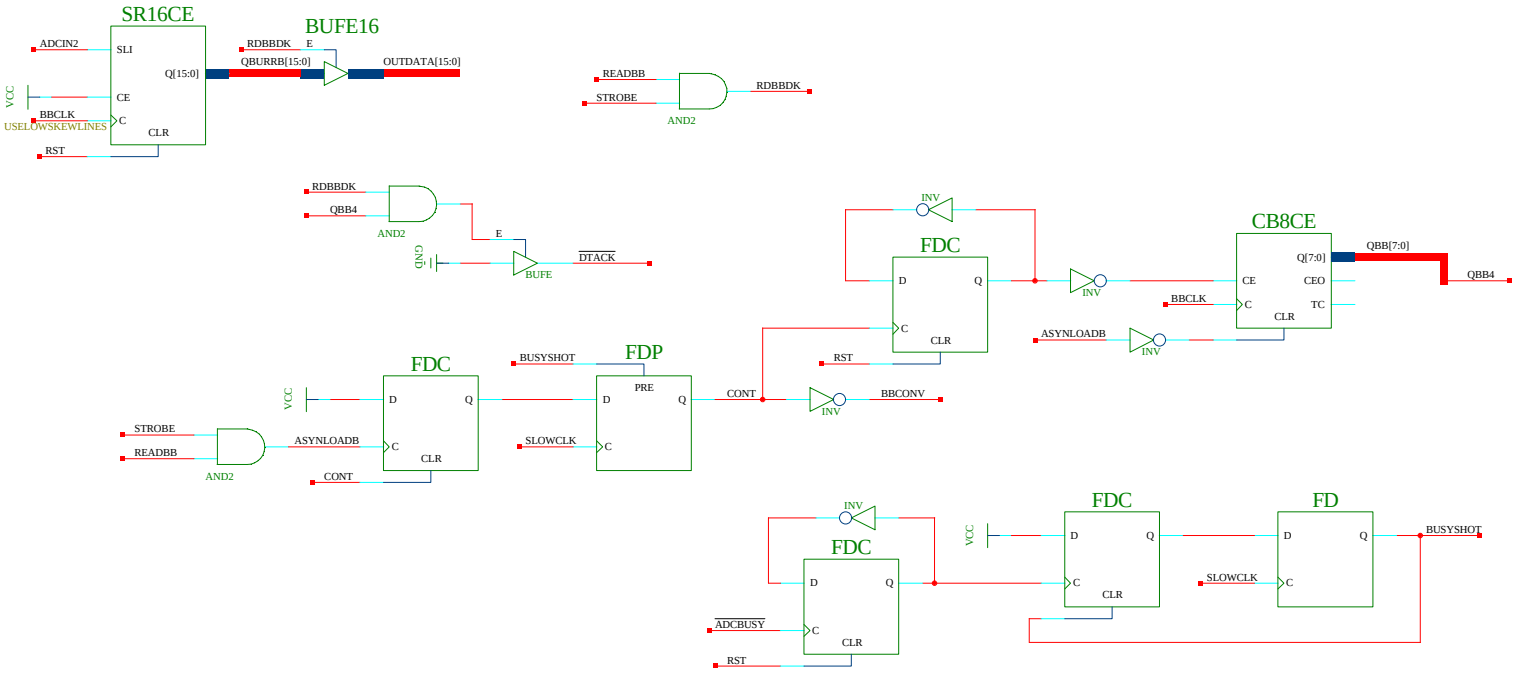
TITLE	DAQMB VME Interface FPGA's JTAG command Decoder DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2C
		PROJECT: DAQMBV	
		DATE: 5-3-2001_9:43	FILE: VPROMJTAG . 4
			PAGE: 45C



DTACK for Load Instruction/Data Register command

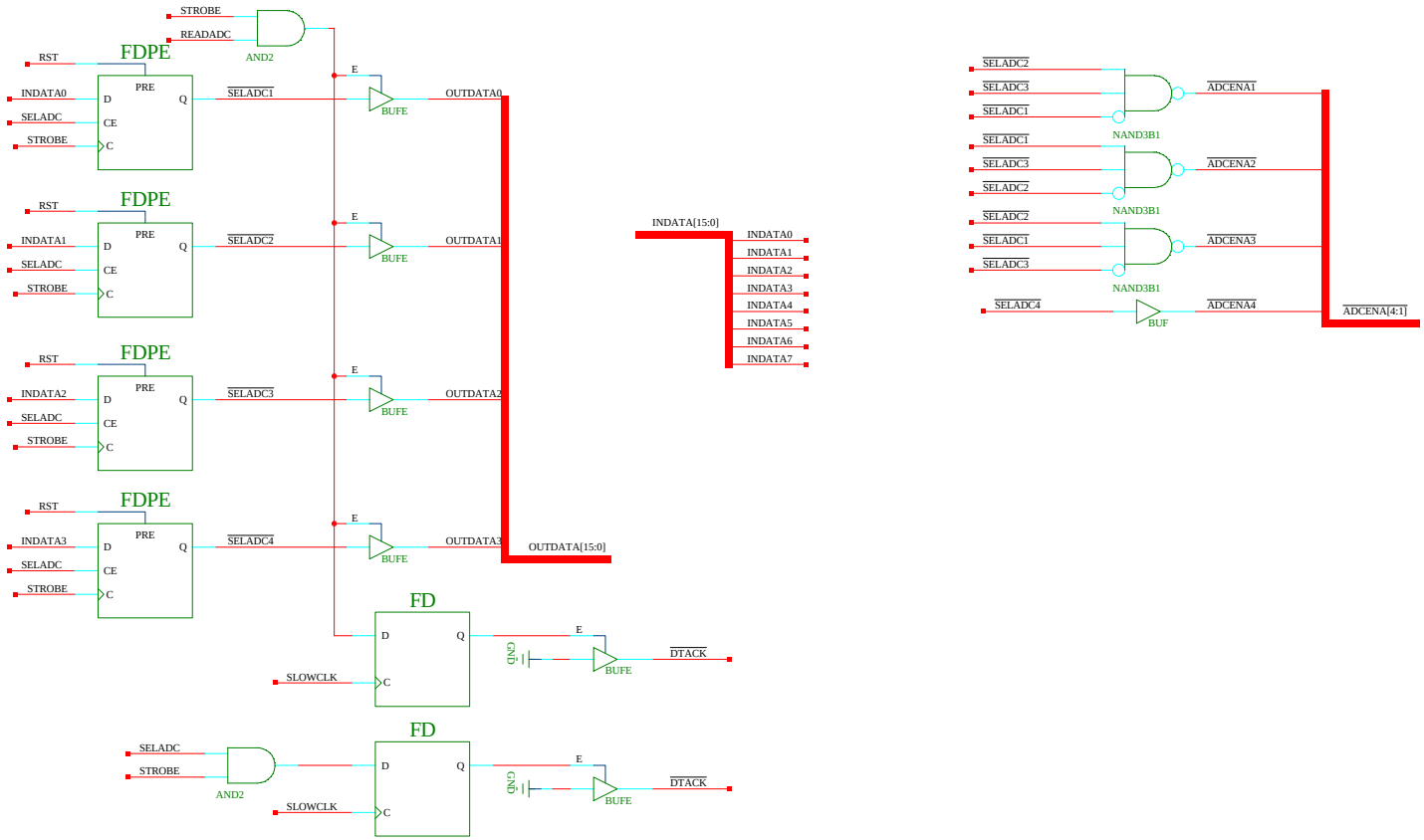
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Serial ADC Interface MAX1271 DAQMB VME Interface CMS CSC Electronics	BY: GU DATE: 3-1-2002_15:30	PARENT PAGE: 2D FILE: SERADC . 1
		PROJECT: DAQMBV	PAGE: 50

Burr-Brown ADS7809, or Analog Devices AD977 interface logic
Procedure: Pull BBCONV low for 400ns after VME command, then go back high. Disable the counter
After ADC BUSY go low to high, send another BBCONV low for 400ns, and enable the counter
At same time disable the BUSYSHOT. After 16 Clock cycles, set DTACK low to indicate Data Ready
Reset the DTACK after VME Address changed, the BB Read cycle ends



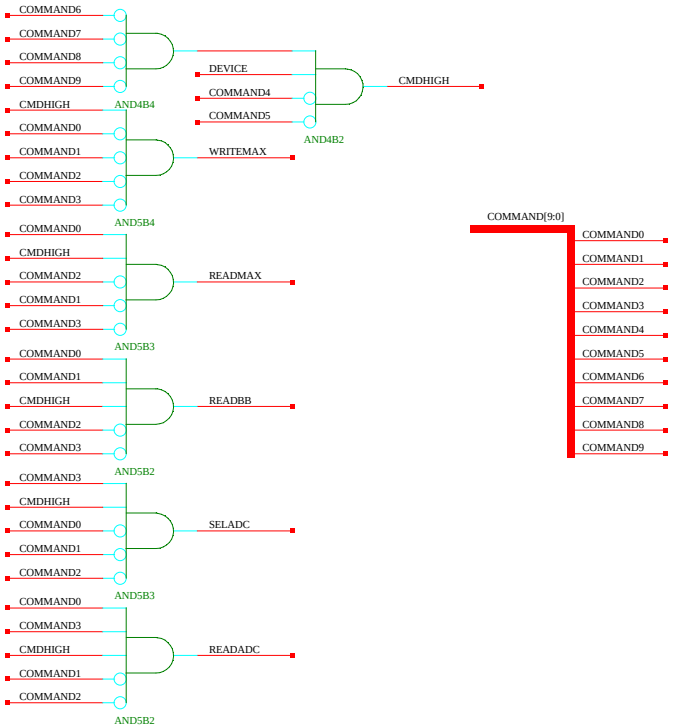
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Burr-Brown ADC Readout DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2D	PROJECT: DAQMBV
		DATE: 8-29-2001_15:18	FILE: SERADC . 2	PAGE: 50A

Serial ADC Selection and Readback Logic



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: ADC Selection and Readback DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2D	PROJECT: DAQMBV
		DATE: 8-28-2001_9:56	FILE: SERADC . 3	PAGE: 50B

CFEB JTAG command decode



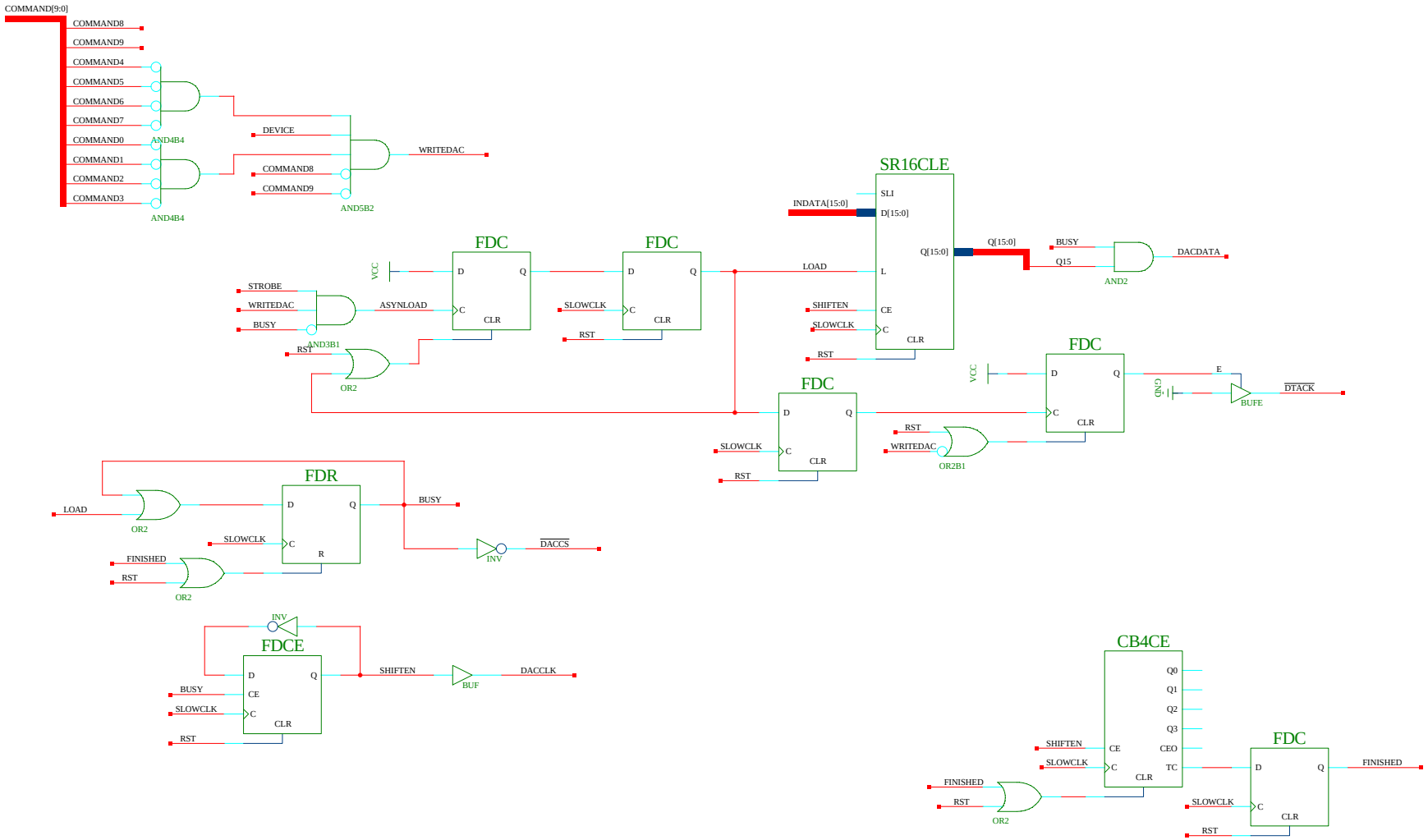
Serial ADC Command Decoder:

00 || Write Control Byte to MAX1271's
01 || Read Data Back from 1271 Register
02 ||
03 || Read Data Back from Burr-Brown Register
04 ||
05 ||
06 ||
08 || Write Serial ADC Chip Select Register
09 || Read Serial ADC Chip Select Register

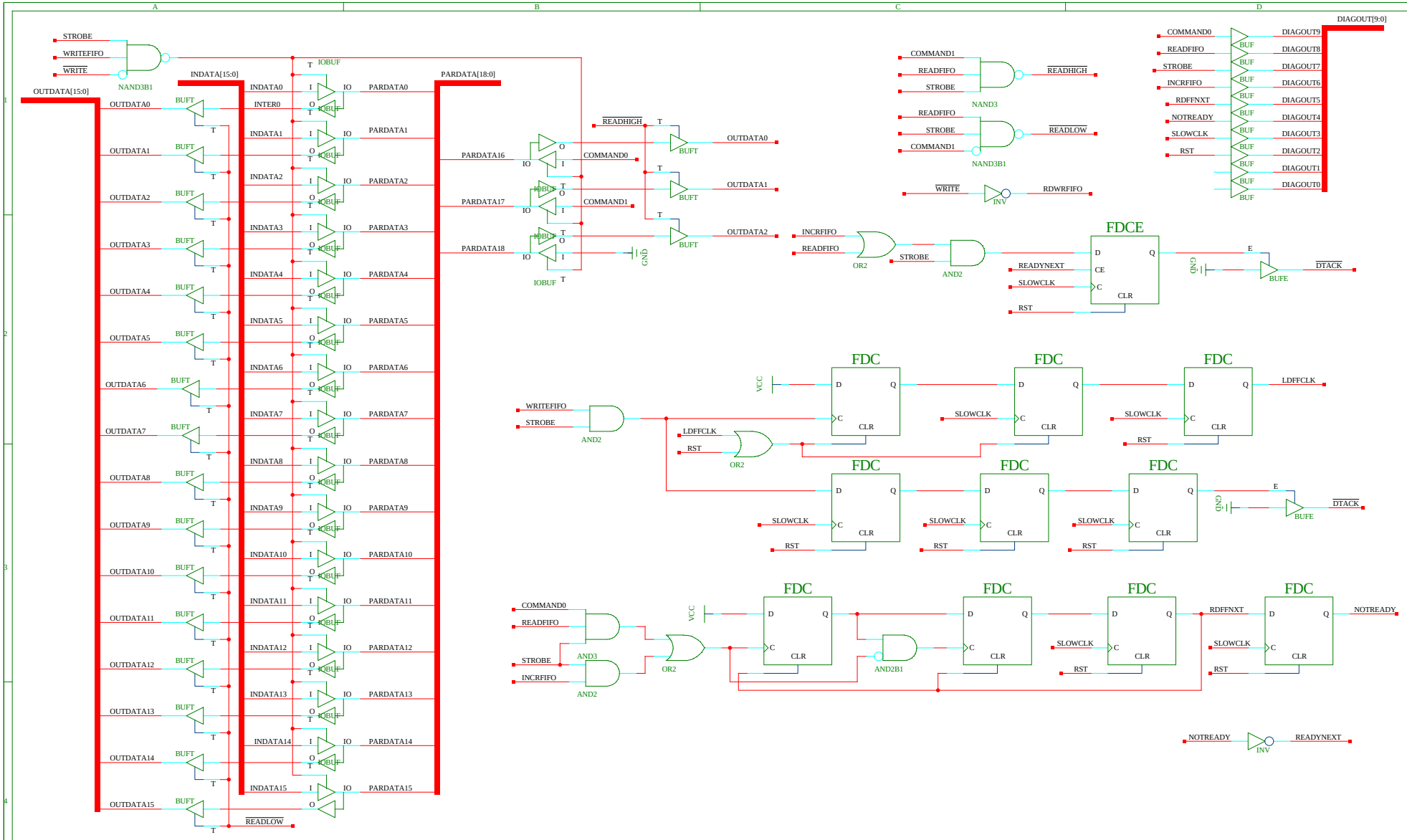
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Serial ADC Commands decoder
DAQMB VME Interface
CMS CSC Electronics

BY	PARENT PAGE	PROJECT
GU	2D	DAQMBV
DATE	FILE	PAGE
8-29-2001_14:09	SERADC . 4	50C

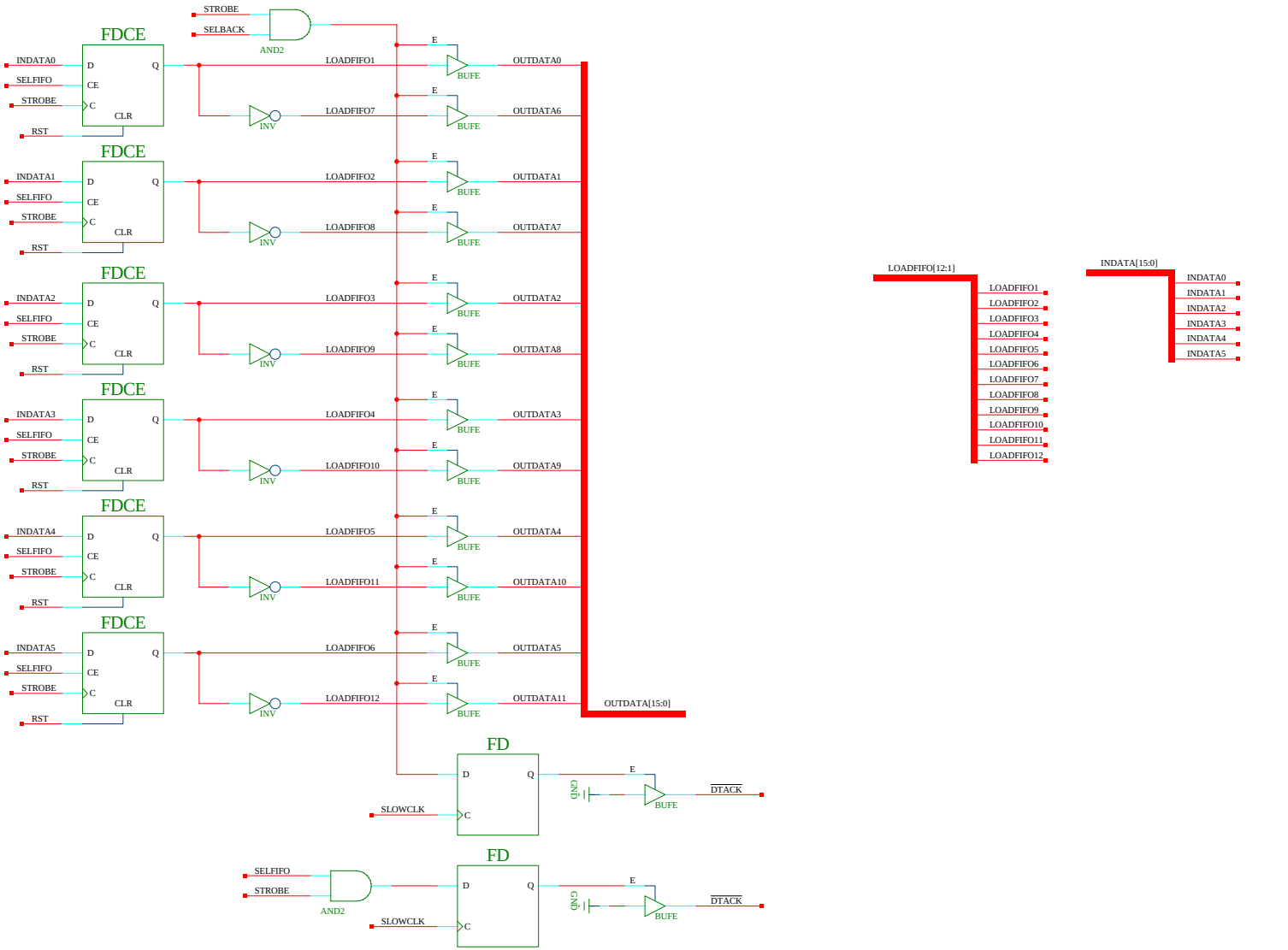


THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Serial DAC Interface DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2E	PROJECT: DAQMBV
		DATE: 5-14-2001_12:48	FILE: SERDAC . 1	PAGE: 60



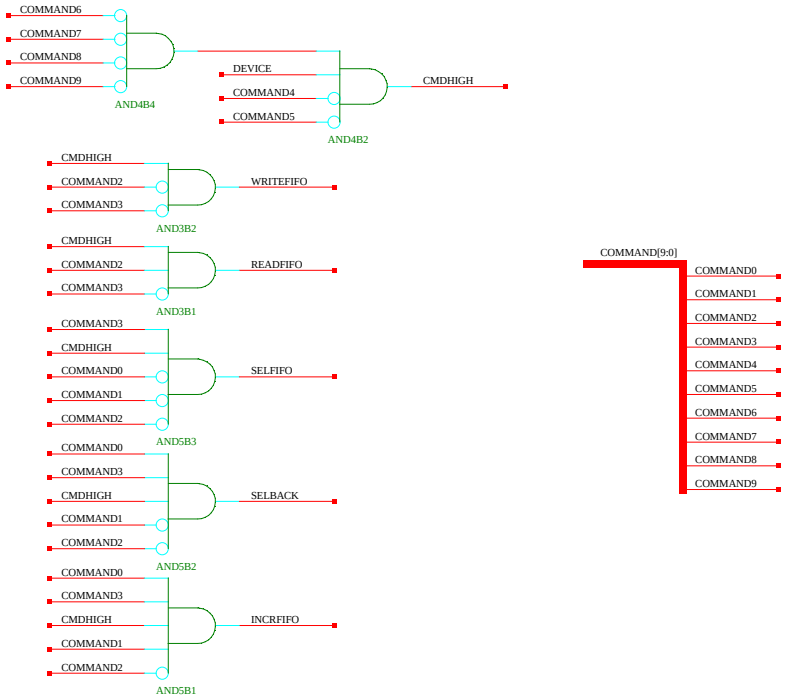
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Parallel Port Control DAQMB VME Interface CMS CSC Electronics	BY: GU DATE: 8-21-2001_14:09	PARENT PAGE: 2F FILE: PORTCNTL . 1
		PROJECT: DAQMBV	PAGE: 70

FIFO Data-loading path selection, and setting readback



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Fifo Register setup/readback DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2F	PROJECT: DAQMBV
		DATE: 7-24-2001_9:30	FILE: PORTCNTL . 2	PAGE: 70A

Parallel FIFO Read/Write Command Decoder



Parallel FIFO Read/write Command Decoder:

- 00 || Write to FIFO, 00 for LastWord/Overlap (no last, no overlap)
- 01 || Write to FIFO, 01 for LastWord/Overlap (last, no overlap)
- 02 || Write to FIFO, 10 for LastWord/Overlap (no last, overlap)
- 03 || Write to FIFO, 11 for LastWord/Overlap (last and overlap)
- 04 || Read low order 16 bits, no FIFO read counter Increment
- 05 || Read low order 16 bits, and FIFO read counter Increment
- 06 || Read high order 2 bits, no FIFO read counter Increment
- 07 || Read high order 2 bits, and FIFO read counter Increment
- 08 || Write FIFO Select Register, (more than 1 FIFO can be enabled)
- 09 || Read FIFO Select Register, just to check 08 function
- 11 || Just Increment FIFO Read Counter

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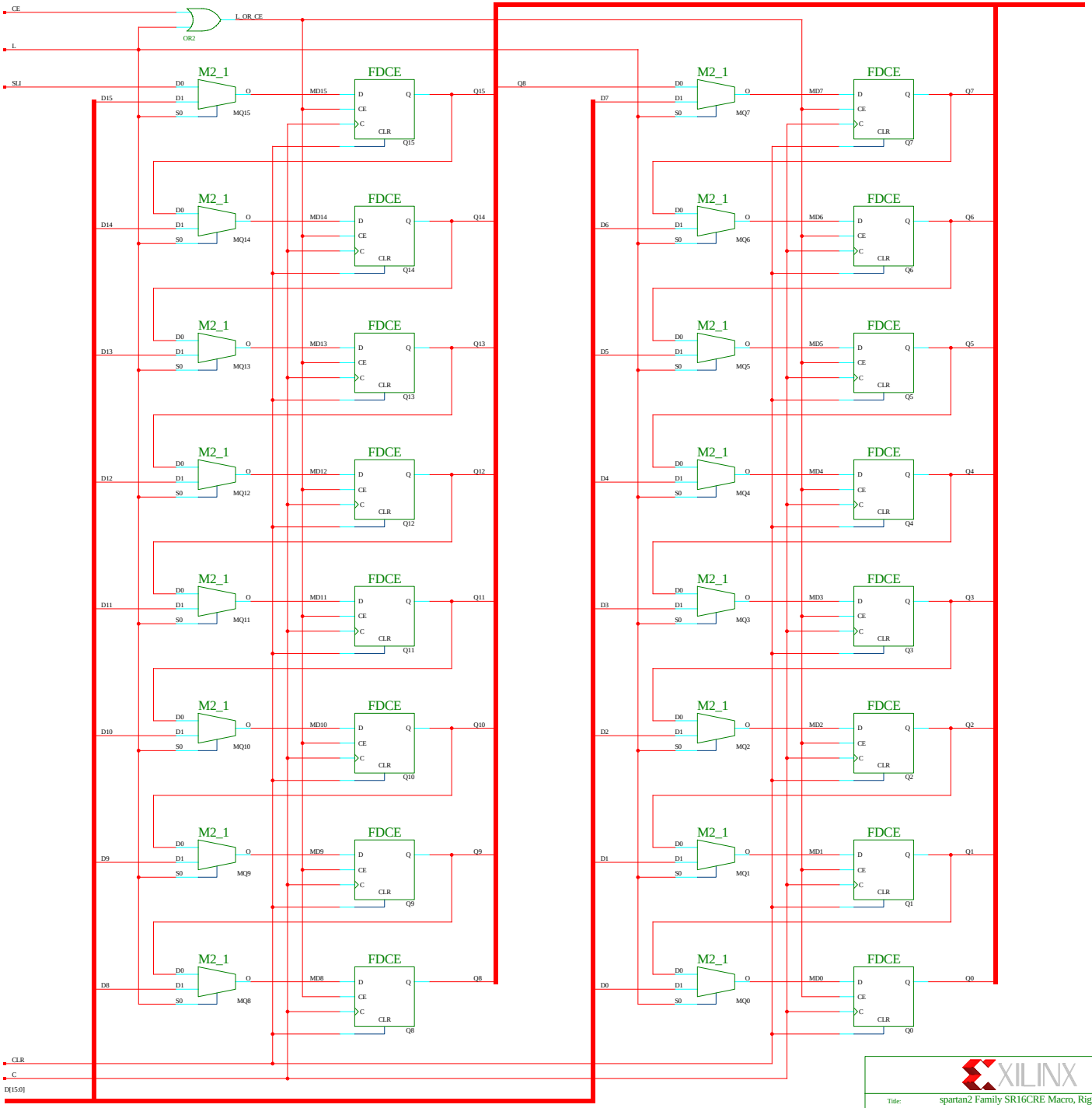
174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE: Parallel port/FIFO read_write Commands decoder DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2F	PROJECT: DAQMBV	
	DATE: 6-11-2001_9:07		FILE: PORTCNTL . 3	PAGE: 70B



drawn by KS

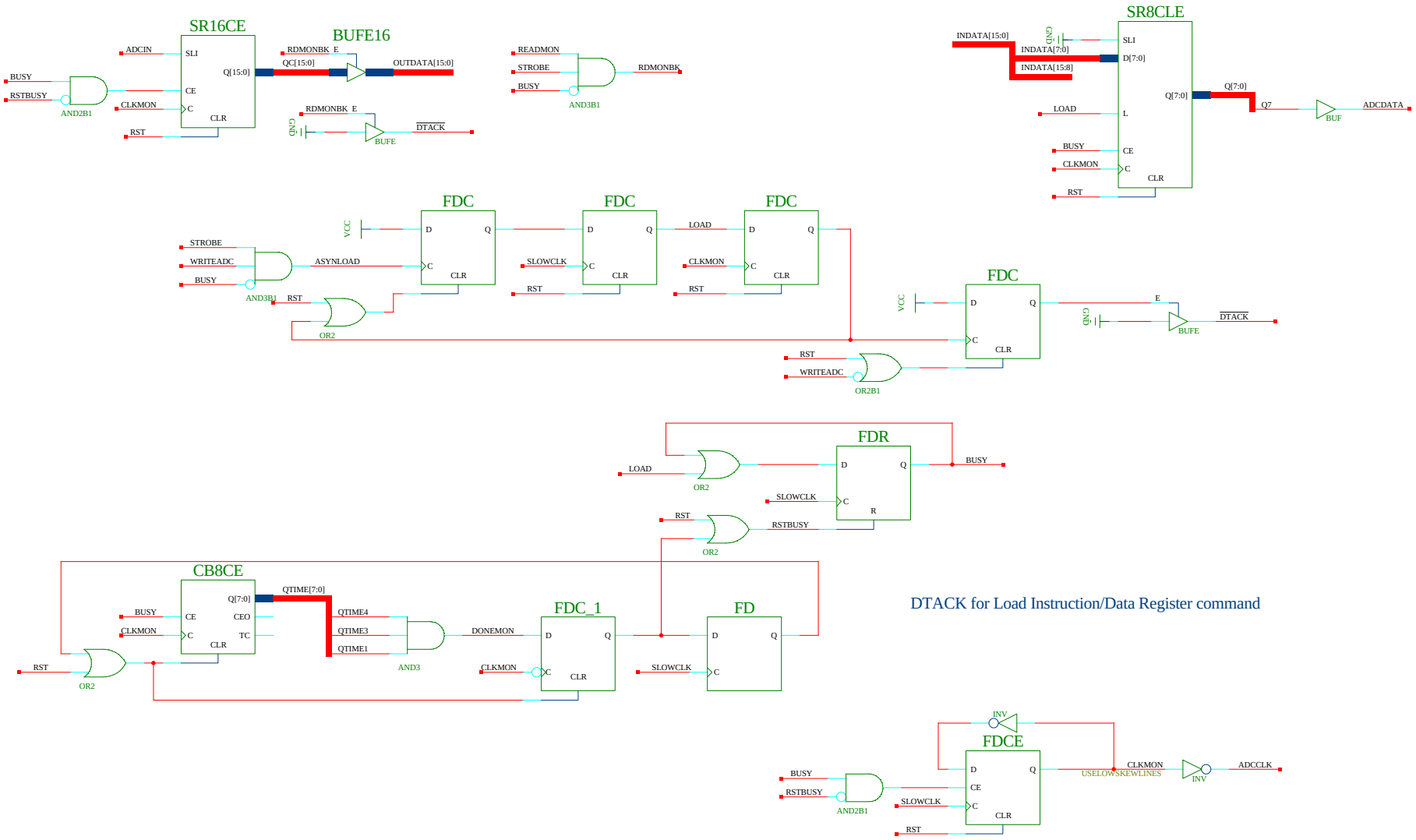
XILINX

Title: spartan2 Family SR16CRE Macro, Right Shift

Comments: 16-Bit Loadable Ser/Para-In, right shift Para-Out Shift Reg w/ Enable & Async Clr

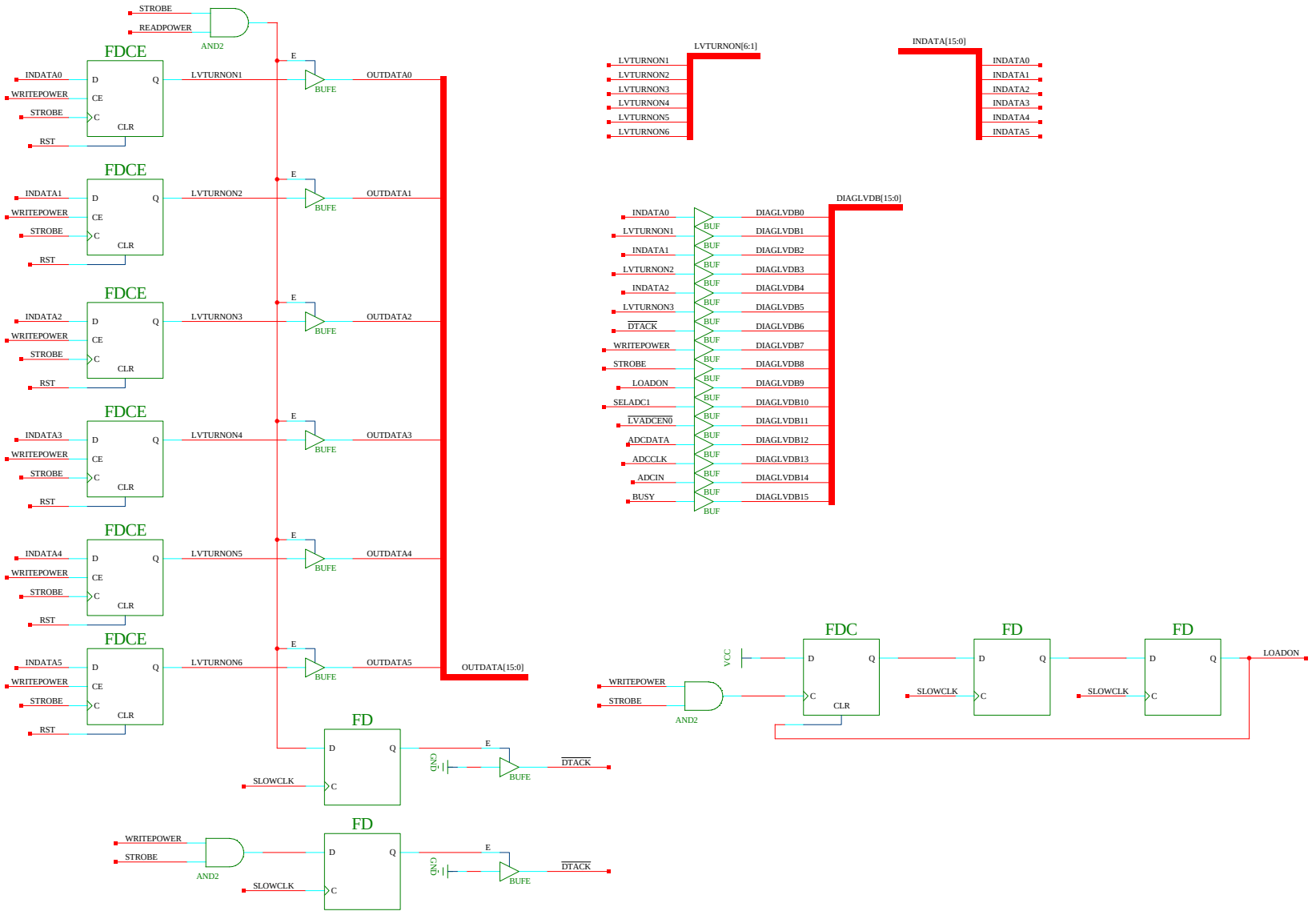
Date: 13th January 1993 | Ver: 1, Modified from XILINX, SR16CLE

Sheet Size: C | Rev: A



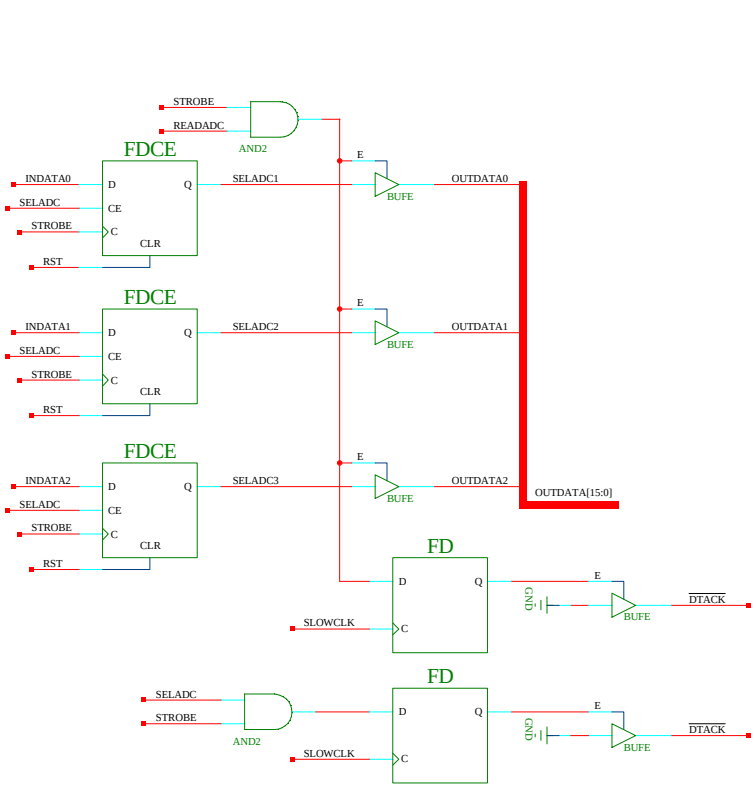
DTACK for Load Instruction/Data Register command

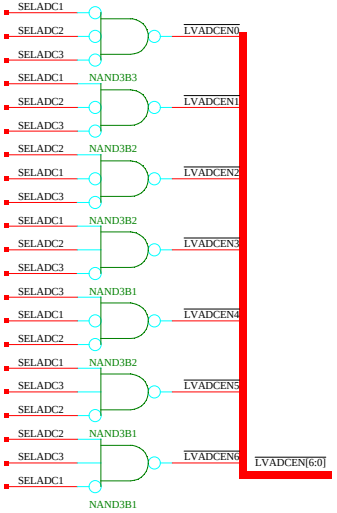
THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Low-Voltage Monitoring ADC DAQMB VME Interface CMS CSC Electronics	BY: GU	PARENT PAGE: 2G	PROJECT: DAQMBV
		DATE: 3-1-2002_15:32	FILE: LVDBMON . 1	PAGE: 80



THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Low-Voltage Turn-on/off control DAQMB VME Interface CMS CSC Electronics	BY: GU PARENT PAGE: 2G PROJECT: DAQMBV DATE: 9-11-2001_12:55 FILE: LVDBMON . 2 PAGE: 80A	

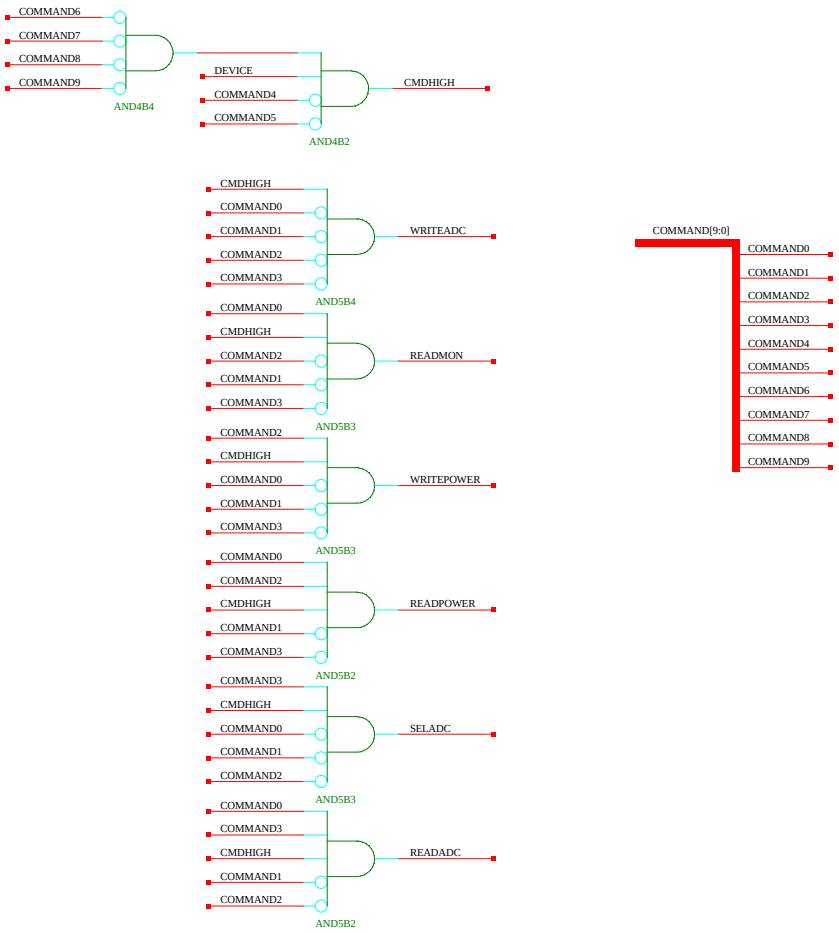
Serial ADC Selection and Readback Logic





THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: ADC Selection and Readback DAQMB VME Interface CMS CSC Electronics	BY: GU PARENT PAGE: 2G PROJECT: DAQMBV DATE: 9-11-2001_12:51 FILE: LVDBMON . 3 PAGE: 80B	

CFEB JTAG command decode



Serial ADC Command Decoder:

00 || Write Control Byte to MAX1271's
01 || Read Data Back from 1271 Register
02 ||
03 ||
04 || Write Low Voltage Power Register
05 || Read Low Voltage Power Register
06 ||
07 ||
08 || Write Low Voltage Monitoring Serial ADC Chip Select Register
09 || Read Low Voltage Monitoring Serial ADC Chip Select Register

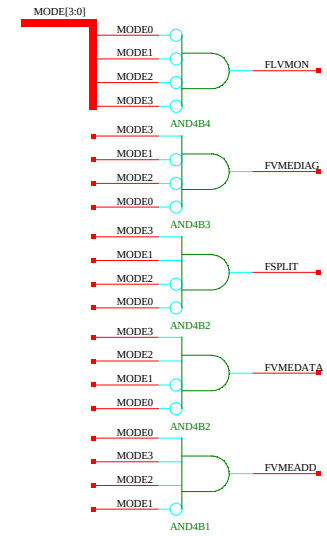
THE OHIO STATE UNIVERSITY
PHYSICS DEPARTMENT ELECTRONICS LAB
174 WEST 18TH AVE, COLUMBUS OH 43210

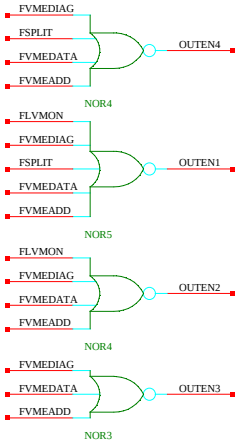
TITLE: Low-Voltage Monitoring Commands decoder
DAQMB VME Interface
CMS CSC Electronics

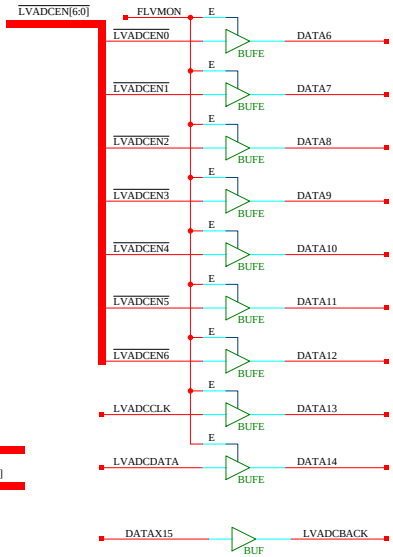
BY	PARENT PAGE	PROJECT
GU	2G	DAQMBV

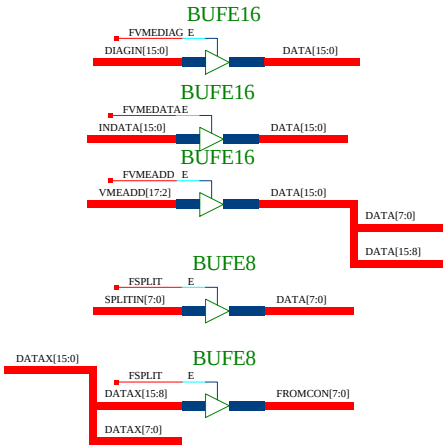
DATE	FILE	PAGE
4-4-2001_12:16	LVDBMON . 4	80C

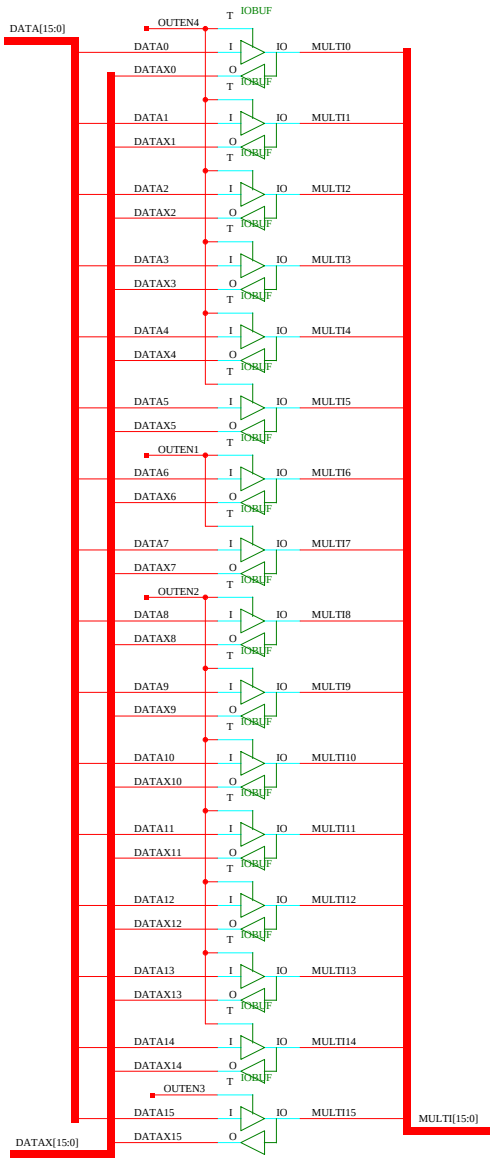
Multi-function Mode Decoder











THE OHIO STATE UNIVERSITY PHYSICS DEPARTMENT ELECTRONICS LAB 174 WEST 18TH AVE, COLUMBUS OH 43210	TITLE: Multi-function Connector Interface DAQMB VME Interface CMS CSC Electronics	BY: GU PARENT PAGE: 2H PROJECT: DAQMBV DATE: 7-25-2001_14:25 FILE: MULTICON . 1 PAGE: 90	