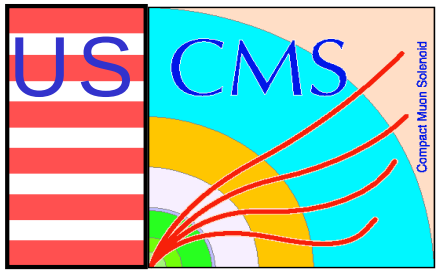
Results of Radiation Test of Cathode Front-end Board in the CMS Endcap Muon System



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T.Y. Ling, M. Tripathi

Reported by T.Y. Ling
LEB 2000

Location of EMU Electronics

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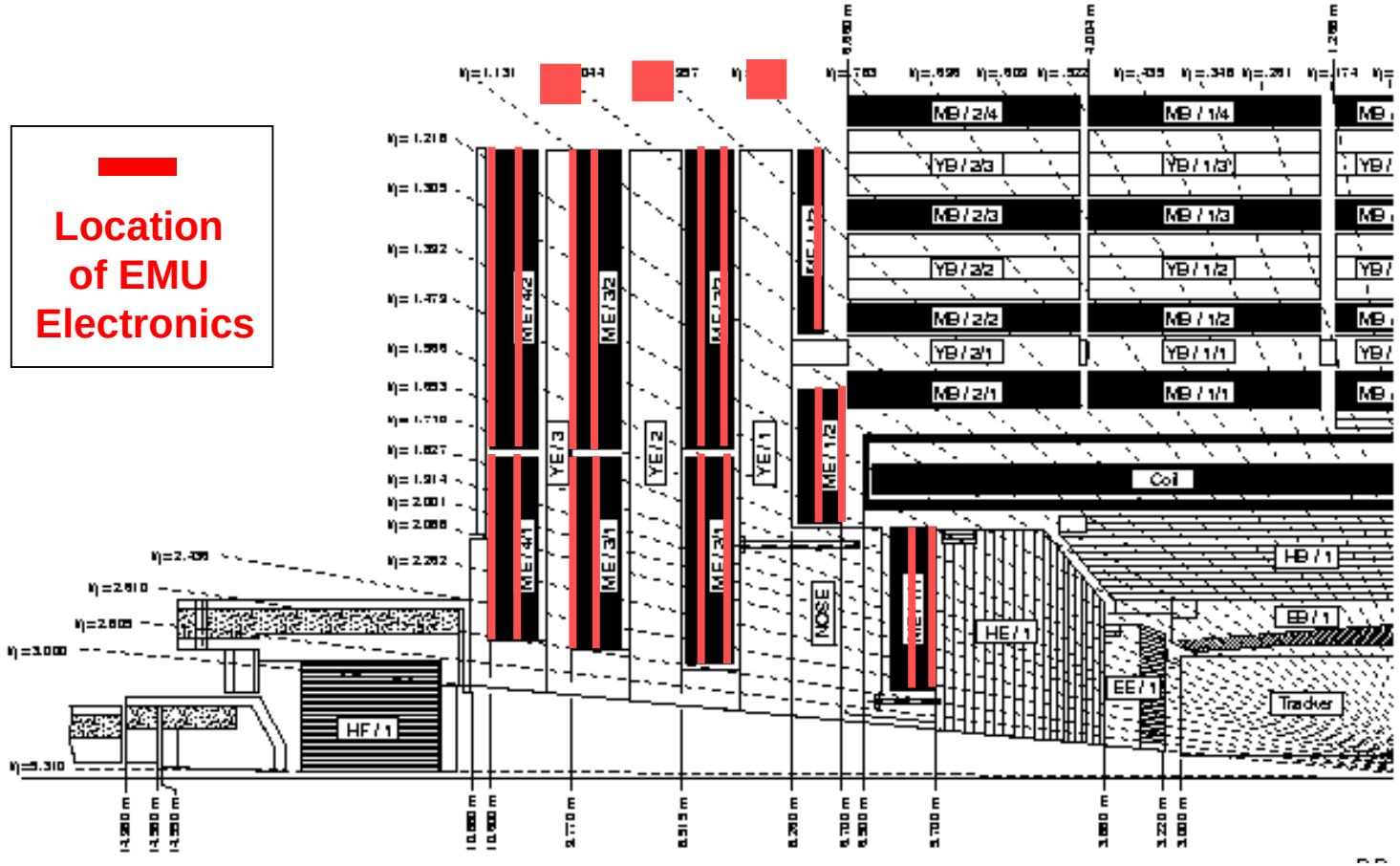


CMS Detector

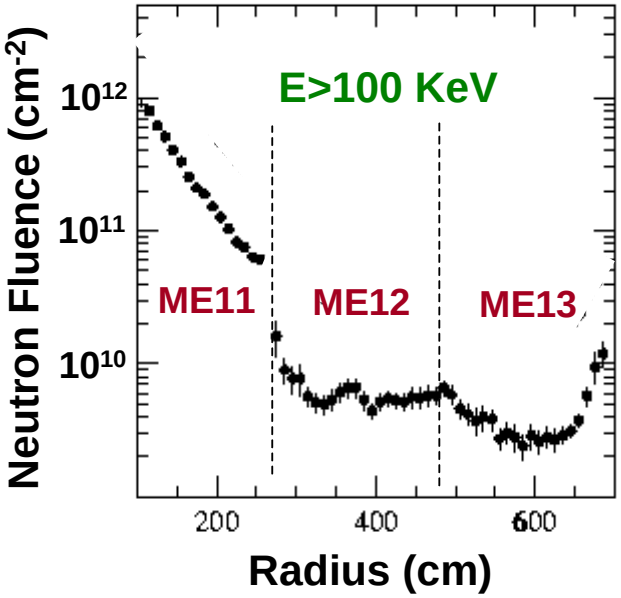
Radiation Levels in Endcap Muon

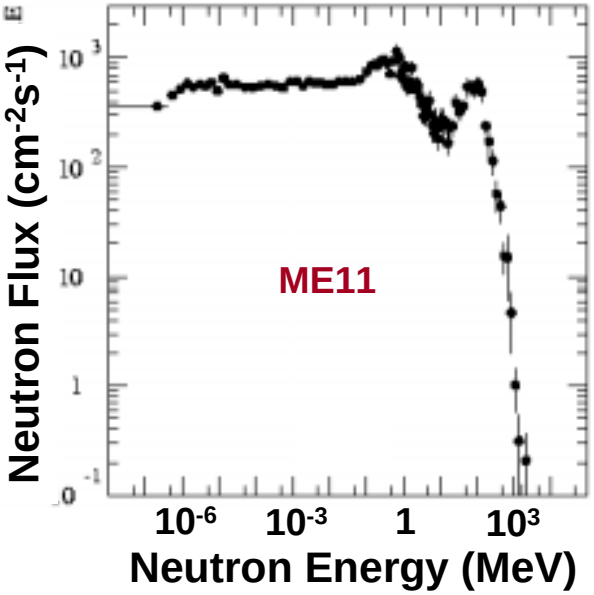
Calculations by *M. Huhtinen*

Integrated over 10 LHC years
(5×10^7 s at 10^{34} $cm^{-2}s^{-1}$)

Neutron Fluence (>100 keV): (0.02 - 6) x 10^{11} cm^{-2}

Total Ionizing Dose: (0.007 - 1.8) kRad





Test Requirements

- **Since all *on-chamber* ASIC's and COTS are the same for all chambers, they should survive the worst-case radiation environment. (Use calculated levels times a safety factor of 3)**
- **Expose ASIC's COTS on CFEB to radiation**
  - **Measure SEE (SEU and SEL) cross sections for COTS and ASIC's. Use the measurements to predict SEE rates for neutron fluence of 2×10^{12} cm^{-2}**
  - **Measure degradation of analog performance for ASIC's due to TID effects up to a dose of 5 kRad**
  - **Measure degradation of analog performance due to displacement damage of *bipolar* for an *equivalent* neutron fluence of 2×10^{12} cm^{-2}**

Test Plan

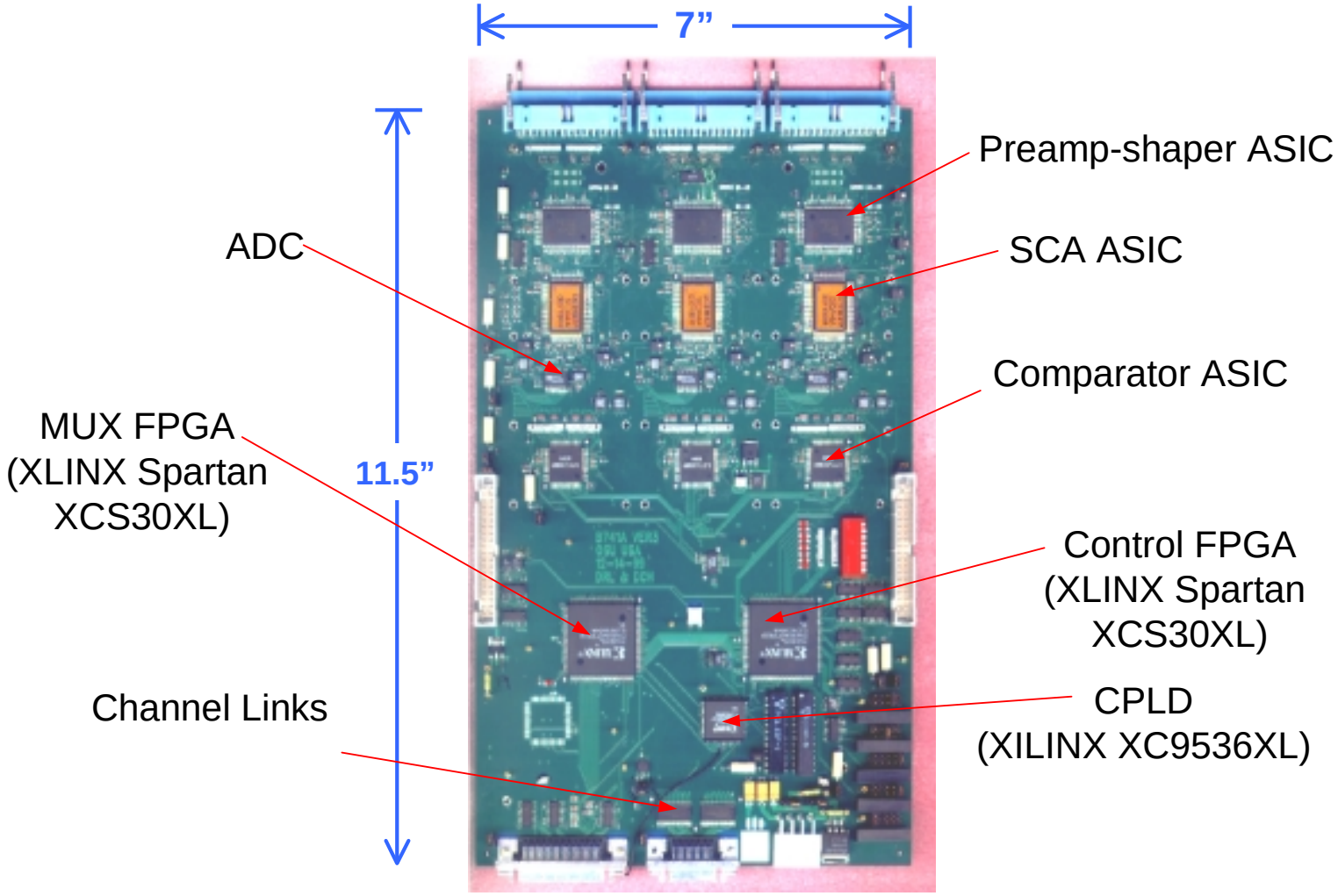
Modeling and Calculations by Huhtinen and Faccio shows:

- **At LHC environment SEU dominated by high energy hadrons (>20 MeV)**
- **For these energies, SEU cross section ~independent of particle type and energy**

Measure SEU Xection using 60-200 Mev proton beam

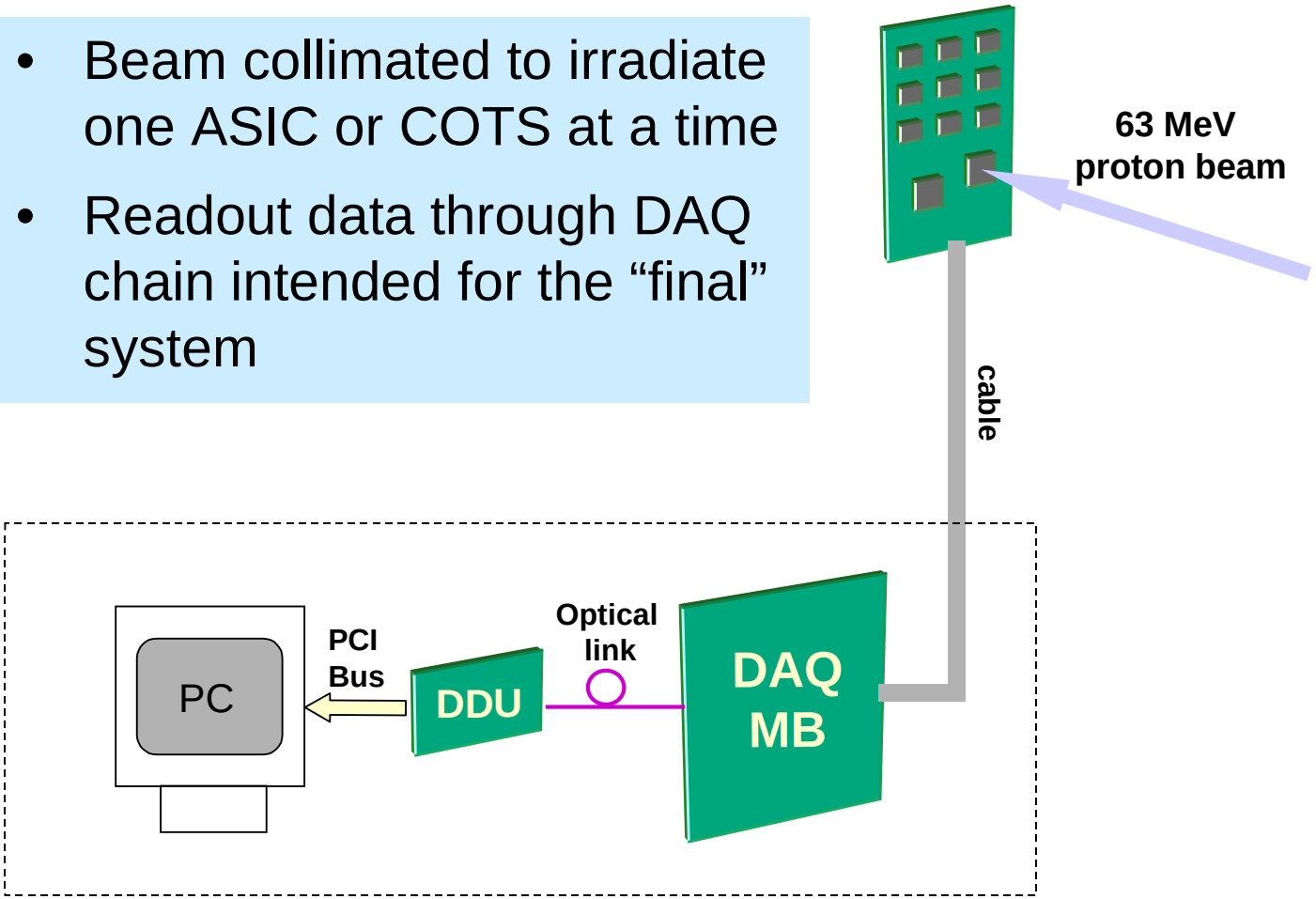
	63 MeV Protons *(UC Davis)*	**1 MeV Neutrons** *(Ohio State)*
CMOS Devices	**SEU, SEL, TID**	
Bipolars Devices	**SEU, SEL, TID**	**Displacement**

Cathode Front-end Board

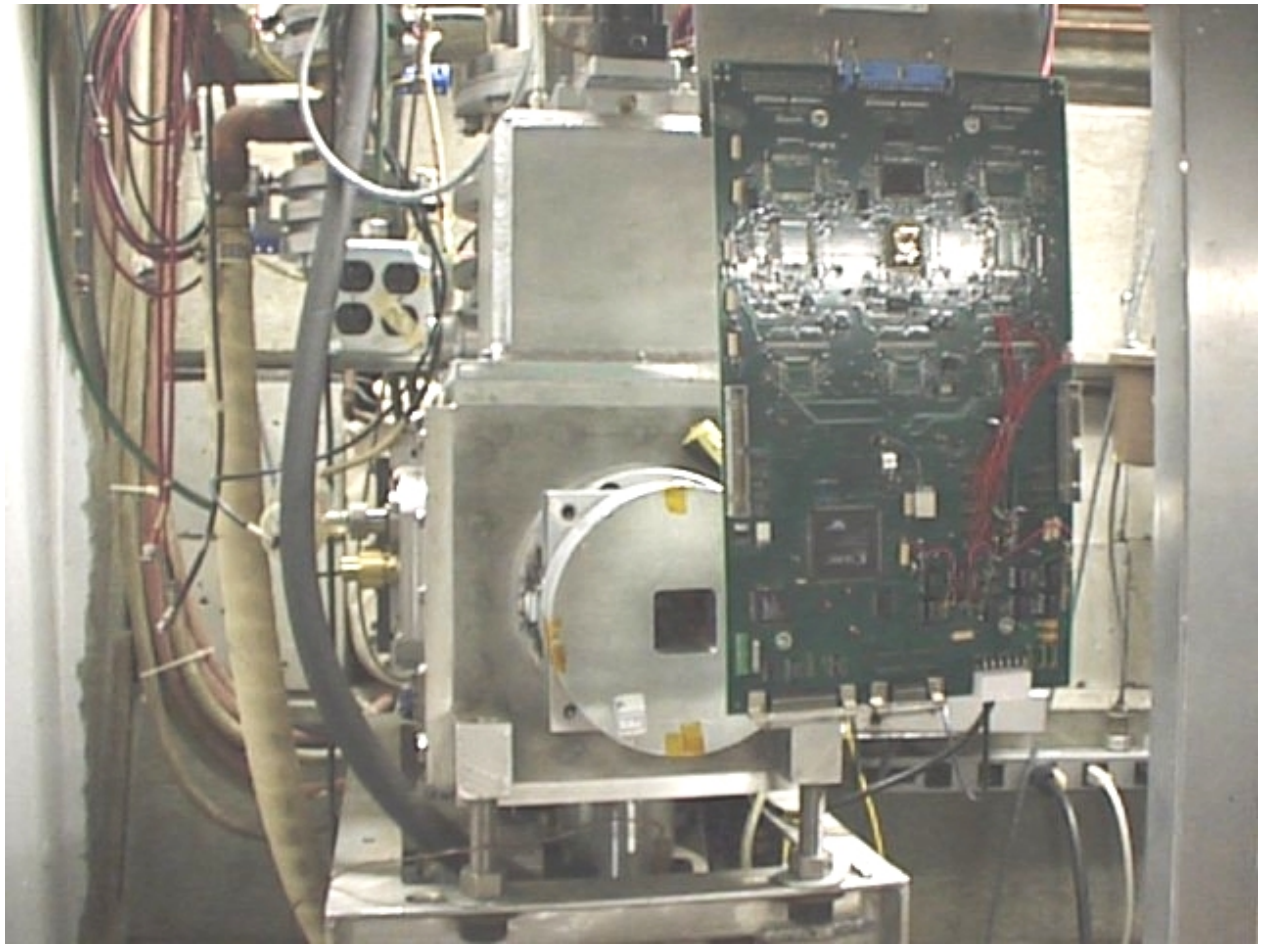


Test Setup

- Beam collimated to irradiate one ASIC or COTS at a time
- Readout data through DAQ chain intended for the “final” system

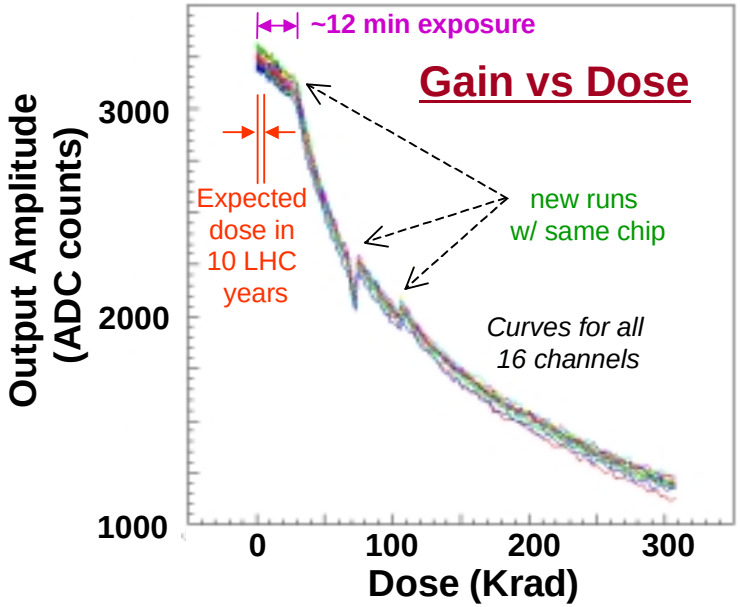


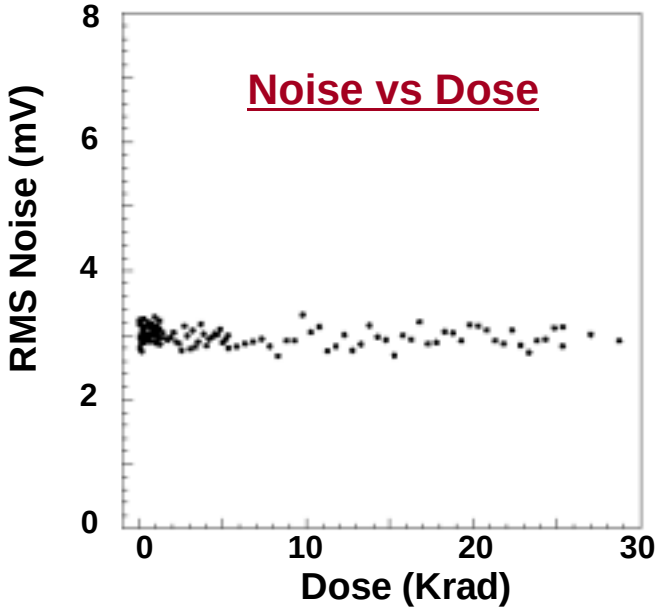
Cathode Board in Proton Beam



Preamp-shaper ASIC

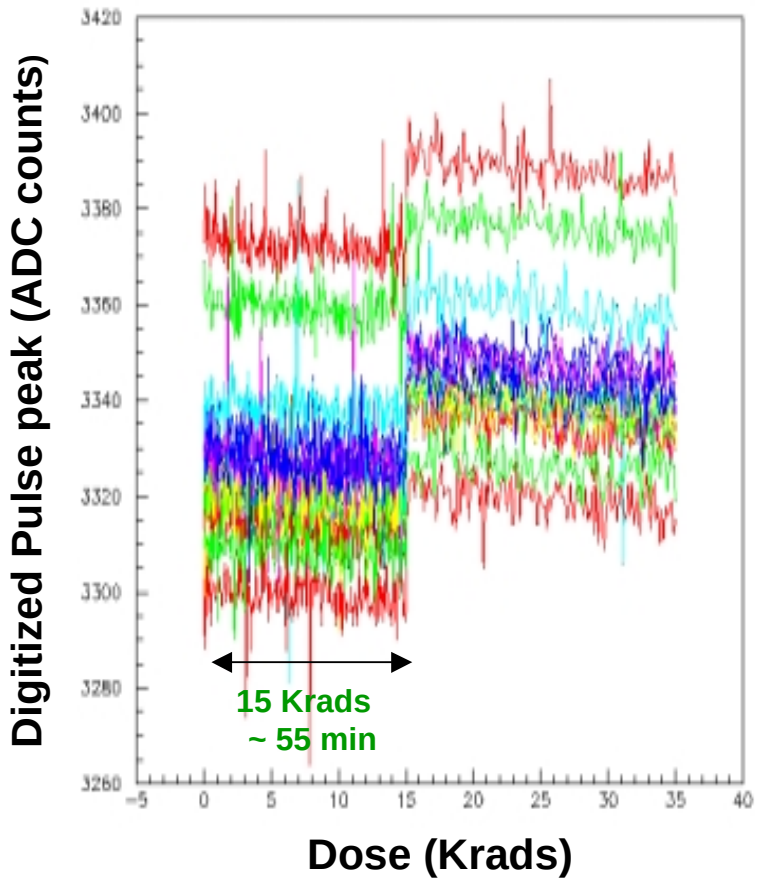
- No single event latch-up for proton fluence of **2.28×10^{12} p/cm^2**
- No shift register errors
- Gain decreases by factor of 2.8, from 0-300 Krads (~ 2 hr run). Not a problem at LHC rates.
- No change in amplifier noise 0-30 kRad.





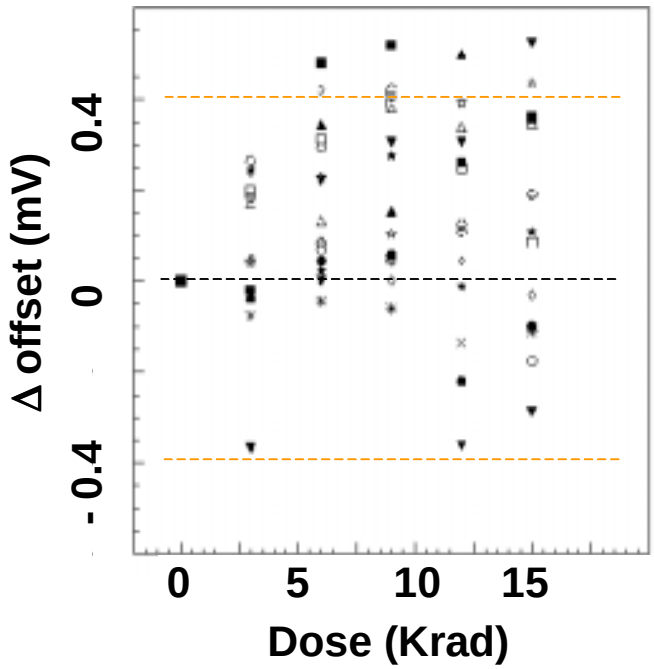
Switched Capacitor Array ASIC

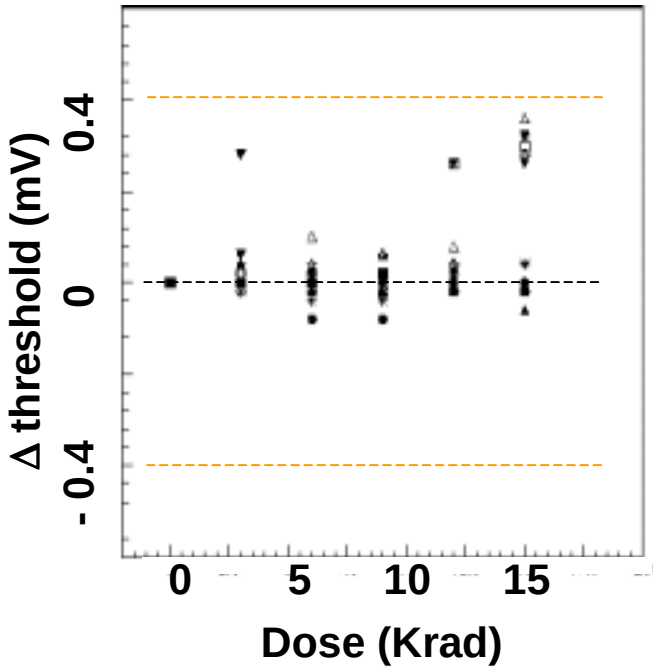
- No single event latch-up for proton fluence of **1.7×10^{12} p/cm^2**
- No degradation of analog performance
- Slight degrease in digitized pulse height vs dose due to output amp gain drop. Not a problem at LHC rates
- Negligible change in noise and pedestal 0 -10 kRad



Comparator ASIC

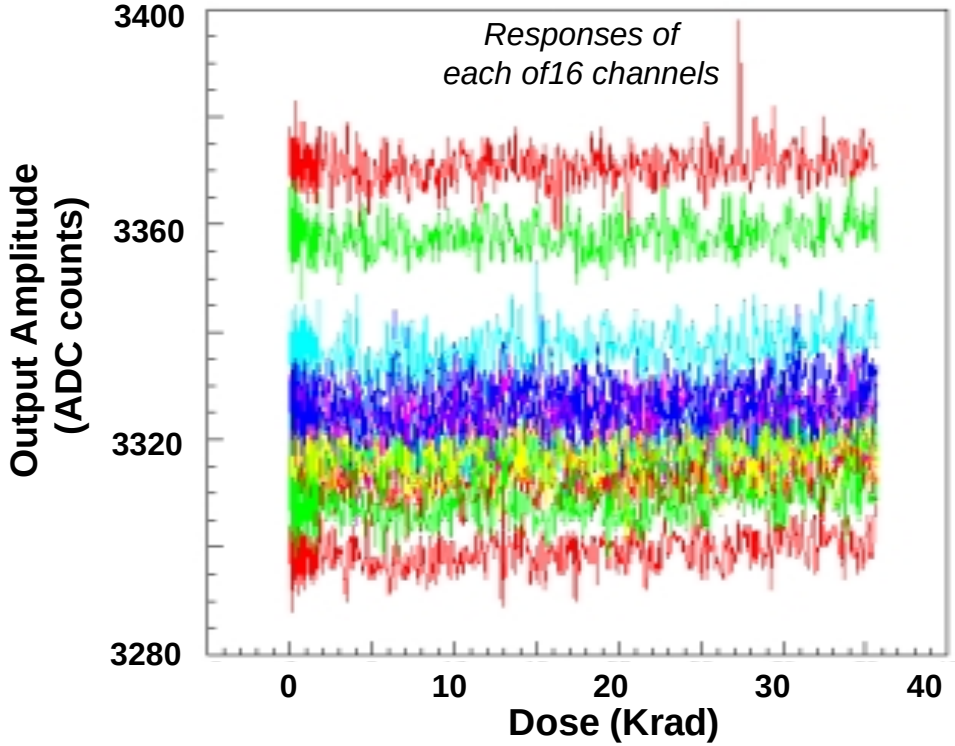
- No single event latch-up for proton fluence of **1.1×10^{12} p/cm^2**
- Shift of thresholds and offsets < 0.4 mV





ADC

- No single event latch-up for proton fluence of **2.7×10^{11} p/cm^2**
- No degradation of performance



Readout Controller FPGA

XILINX Spartan XCS30XL

Irradiation: 9.9×10^{10} p/cm^2
(2 runs; TID=13.4 Krads)

- No Single Event Latch-up.
- Capacitor block numbers predicted and checked w/ blocks numbers read back.
- SCA read/write addresses read back and checked.
- 27 Errors detected. All are recoverable by reloading FPGA.
  - 70% of these errors associated with a change in configuration memory. For these, only 1 in 16 configuration memory changes related to observed controller error
- SEU cross section = 2.7×10^{-10} cm^2

Multiplexer FPGA

XILINX Spartan XCS30XL

Irradiation: 2.86×10^{11} p/cm^2

(6 runs; TID=38.1 Krads)

- No Single Event Latch-up
- 34 MUX controller errors detected. All recoverable by reloading FPGA. (70% of these errors associated with a change in configuration memory.)
- SEU cross section = 1.2×10^{-10} cm^2
- Configuration errors occurs after 13.3 Krad and increase drastically after 23 Krad. These are not cleared by reset, but do not effect controller functioning.
- 5th run stops when MUX quit working (35.7 Krad). The same chip recovers after 2 hours.

CPLD

XILINX CPLD XC9536XL

Chip 1: 2.8×10^{11} p/cm^2 (3 runs; TID=37.8 Krads)

- No Single Event Latch-up
- No configuration errors
- 106 errors detected. All recoverable by reload.
- Chip died after exposed to 42.7 Krads

Chip 2: 3.1×10^{11} p/cm^2 (2 runs; TID= 41.3Krads)

- No Single Event Latch-up
- No configuration errors
- 117 errors detected. All recoverable by reload.

SEU cross section = 3.8×10^{-10} cm^2

Readout Control/MUX FPGA

XILINX Virtex XCV50

Irradiation: 9.3 x 10^{10} p/cm^2

(5 runs; TID=12.5 Krads)

- No Single Event Latch-up.
- Capacitor block numbers predicted and checked w/ blocks numbers read back.
- SCA read/write addresses read back and checked.
- 16 Errors detected. All are recoverable by reloading FPGA.
- SEU cross section = 1.7 x 10^{-10} cm^2

Summary of SEU Measurements

Device (Function)	Proton Fluence (10^{11} cm^{-2})	Dosage (kRad)	Number of SEU's	SEU Xection (10^{-10} cm^2)
XILINX Spartan XCS30XL (Readout Controller)	1.0	13.4	27	2.7
XILINX Spartan XCS30XL (Multiplexer)	2.9	38.1	34	1.2
XILINX CPLD XC9536XL (Chip 1)	2.8	37.8	106	3.8
XILINX CPLD XC9536XL (Chip 2)	3.1	41.3	117	
XILINX Virtex XCV50 (Readout Controller & MUX)	0.9	12.5	16	1.7
Channel Link Receiver	14.8	200	277	1.9
Channel Link Transmitter	14.8	200	1023	6.9

Bipolar devices

- **Irradiated with 1 MeV neutrons at OSU**
- **Fluence = 2.8 x 10^{12} / cm^2**
- **Following devices passed the test**
  - **LM1117-adj** (adjustable voltage regulator)
  - **LM4120-3.3** (voltage reference; 3.3 V, 5 mA)
  - **LM4120-1.8** (voltage reference; 1.8 V, 5 mA)
  - **LM4041** (shunt voltage reference)
  - **SDA321** (Diode Array – reversed biased)
  - **Red LED**
  - **AD8011** (300 MHz Current Feedback OpAmp)
- **Need a rad-tolerant 2.5 V regulator**
  - **Good candidate identified. Need to be tested.**

Conclusions

- **Cumulative effects**
  - **Total ionization dosage (with 63 MeV protons)**
    - **No deterioration of analog performance up to 10 krad for all three CMOS ASIC's**
    - **All FPGA's survive beyond dosage of 30 krad**
  - **Displacement damage (with $2x10^{12}$ cm^{-2} n's @ 1 MeV)**
    - **Usable voltage regulators and references identified**
    - **Protection diodes OK**
- **Single-Event Effects**
  - **No latch-up for all ASIC's up to $2x10^{12}$ p cm^{-2}**
  - **Single Event Upset (SEU)**
    - **Cross sections measured for all FPGA's, C-Links.**
    - **All SEU's in recoverable by reloading FPGA's**