EMU FED
--- Crate and Electronics

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The Ohio State University

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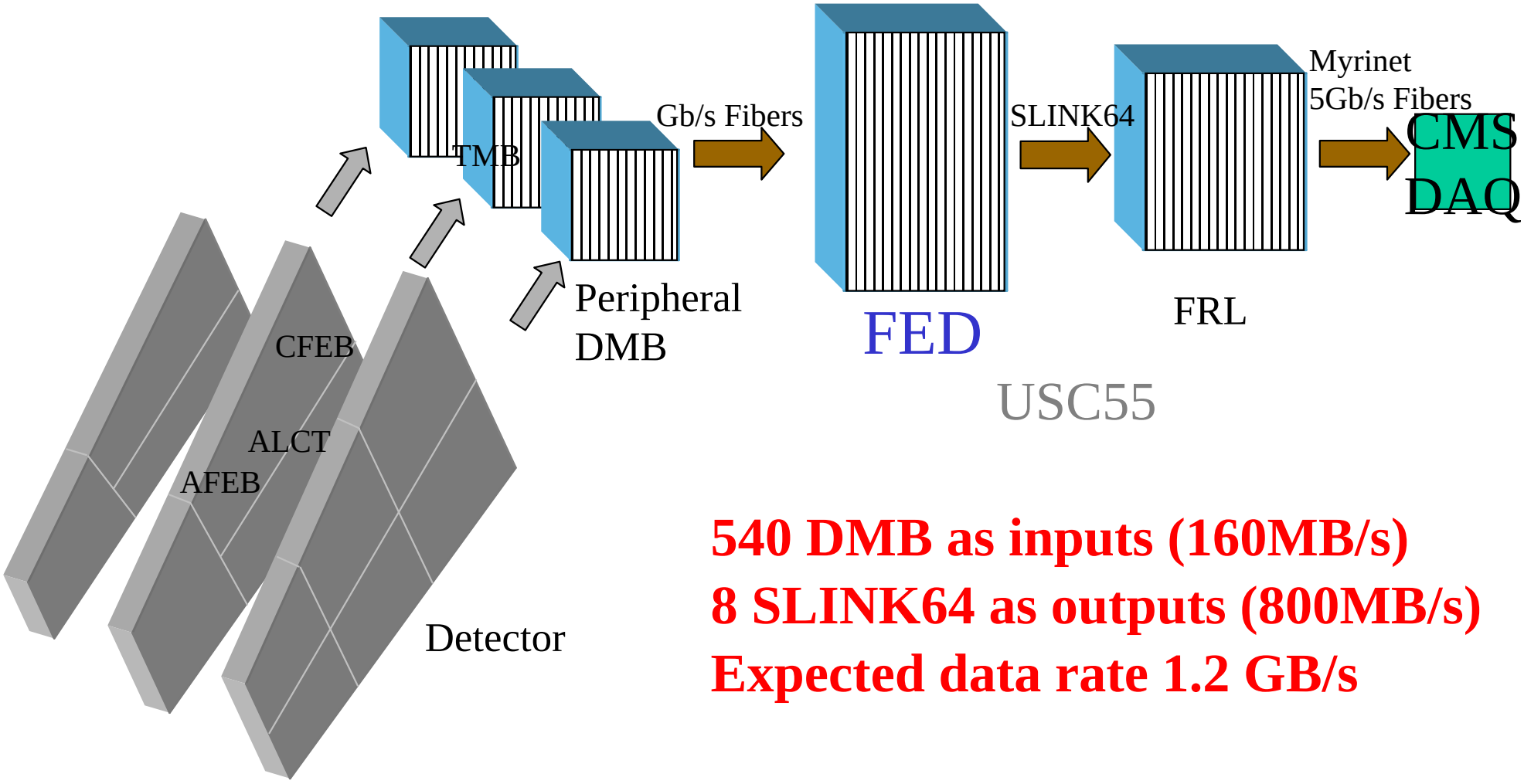
EMU FED: Outline

- EMU FED Design
- FED Crate & Custom Backplane
- DDU Functions and Tests
- DCC Functions and Tests
- Data Flow Control
- FED Production Preparation

EMU FED: EMU FED Design



540 DMB as inputs (160MB/s)

8 SLINK64 as outputs (800MB/s)

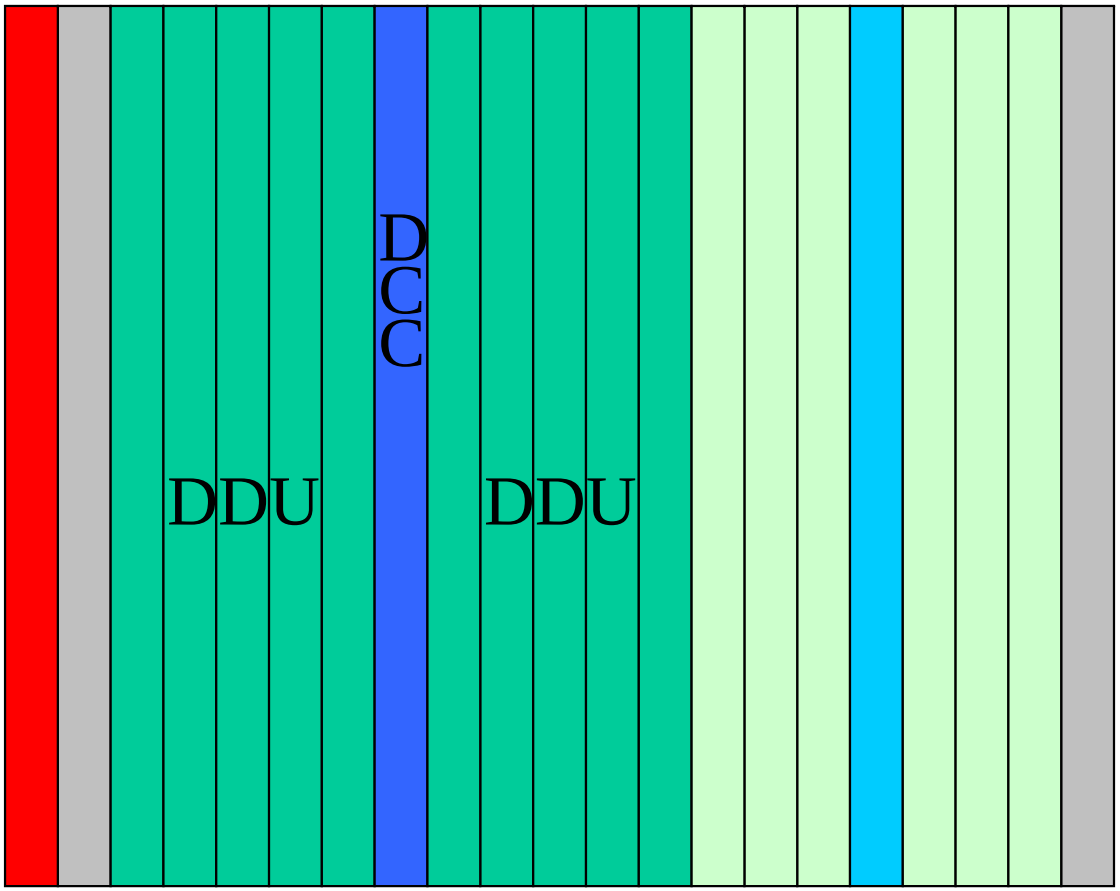
Expected data rate 1.2 GB/s

EMU FED: EMU FED Location

+Z			Upper	Floor	(Zone S2)			-Z
	A	B	C	D	E	F	G	H
01	--	--	--	ECAL spare	Cal Reg Trig	HCAL HTR	--	--
02	TOTEM	TOTEM	DAQ	ECAL ULR	Cal Reg Trig	HCAL HTR	DAQ	x
03	TOTEM	TOTEM	HCAL Calib	ECAL ULR	Cal Reg Trig	HCAL HTR	EBE DCS	x
04	TOTEM	TOTEM	HCAL Calib	ECAL ULR	Cal Reg Trig	HCAL HTR	EBE DCS	x
05	TOTEM	DAQ	HCAL Calib	ECAL SRP/TTC	%Cal Reg Trig	%HCAL HTR	Presh. DCS	x
06	ASSM	EB HV	HCAL DCS	ECAL ULR	Cal Reg Trig	HCAL HTR	EB HV	x
07	ASSM	EB HV	HCAL DCS	ECAL ULR	Cal Reg Trig	HCAL HTR	EB HV	x
*08	ASSM	EB HV	HCAL SrcDrv	ECAL ULR	Cal Reg Trig	HCAL HTR	EB HV	x
*09	ASSM	EE HV	HPD HV	DAQ	Cal Reg Trig	DAQ	EE HV	x
10	ASSM	Presh. LV/HV	HPD HV	Presh. FED	Cal Reg Trig	x	Presh. LV/HV	x
11	ASSM	Presh. LV/HV	HPD HV	Presh. FED	TOTEM Trig	EBE Lt Mn	Presh. LV/HV	F.D.
12	ASSM	Presh. LV/HV	HPD HV	DAQ	CASTOR Trig	EBE Lt Mn	Presh. LV/HV	F.D.
13	ASSM	Presh. Misc	HPD HV	ECAL Cool	x	EBE Lt Mn	EB LV	F.D.
14	ASSM	x	PMT HV	ECAL Cool	Align PCs	EBE Laser	EE LV	F.D.
15	ASSM	DSS	DSS	DSS	Align Laser	DSS	DSS	F.D.

+Z			Lower	Floor	(Zone S1)			
	A	B	C	D	E	F	G	H
00	--	--	--	Presh. FEC	TK. FEC	TK. FEC	DT/RO/SC	--
01	--	--	--	DT TrkFnd	Opt.Cpl.	RPC Trig	Pixel FEC	--
02	TK. Ctrl	DAQ	DAQ	DT TrkFnd	TTC	RPC Trig	Pixel Ctrl	RPC B HV
03	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	DT TrkFnd	TTC	RPC Trig	Pixel FED	RPC B HV
04	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	CSC TrkFnd	Global	RPC Trig	Pixel FED	RPC B HV
05	TK. Ctrl	TK. FED TIB+TID	TK. FED TOB	CSC TrkFnd	%Cal Global	%RPC Trig	DAQ	RPC B HV
06	CSC HV	DAQ	DAQ	DAQ	TTS	RPC Trig	CSC FED	RPC B HV
07	CSC HV	FED PCs	DAQ	DT HV	TTS	RPC Trig	CSC FED	RPC B HV
*08	CSC HV	DAQ	DAQ#	DT HV	BPTX	RPC Trig#	CSC FED	RPC E+ HV#
*09	CSC HV	TK. FED TEC-	TK. FED TEC+#	DT HV	LHC	DAQ#	ME1/1 HV	RPC E+ HV
10	CSC HV	TK. FED TEC-	TK. FED TEC+	DT HV	BPM	DSS	ME1/1 HV	RPC E- HV
11	DAQ	TK. FED TEC-	TK. FED TEC+	DT HV	DSS	DSS	DSS	RPC E- HV

EMU FED: EMU FED Design

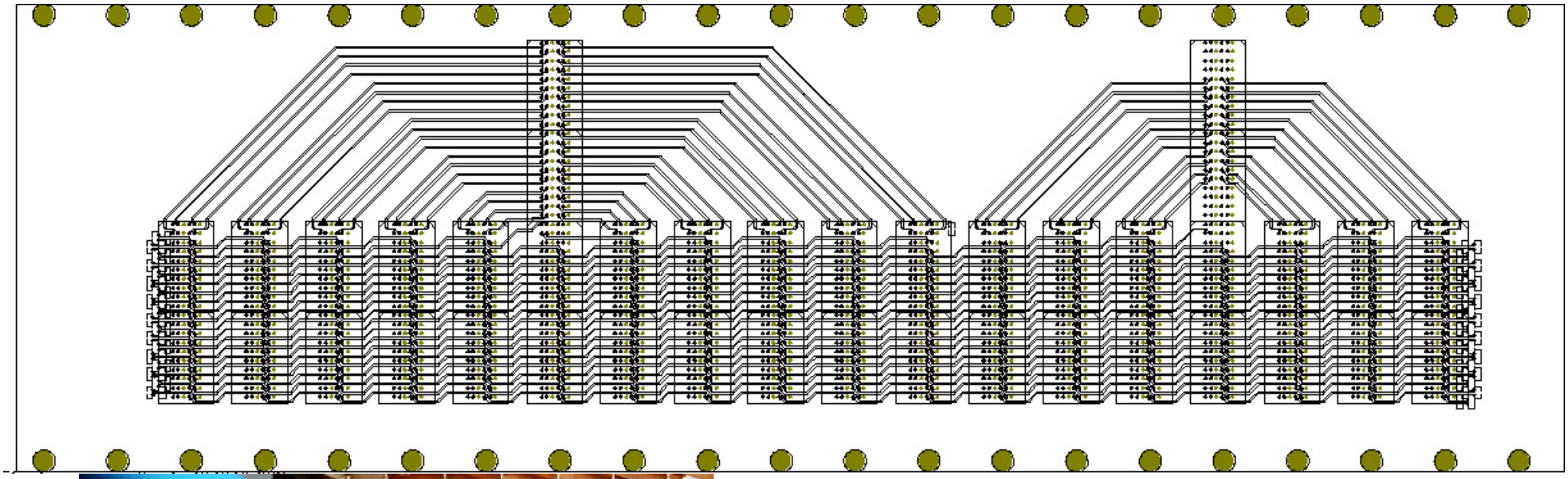


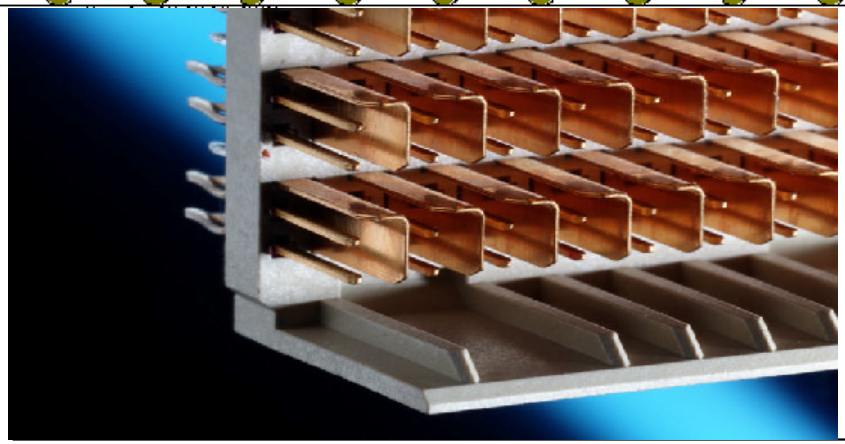
- **Four 9U Crates**
  - **9U X 220mm Board**
- **Data Concentration:**
  - **15 DMB to 1 DDU**
  - **9 DDU to 1 DCC**
  - **1 DCC to 2 SLINK64**
  - **9 DDU per SLINK (4)**
  - **4/5 DDU per SLINK (8)**
  - **2/3 DDU per SLINK (16)**
  - **1 DDU per SLINK (36)**
  - **36 DDU, 4/8 DCC needed**

The crate will be a standard 9U crate with minor modification

EMU FED: EMU FED crate backplanes

P1: Standard VME64x, for slow control
P2: empty
P3: custom for TTC control and Fast data transmission between DDU and DCC





6.4 Gbps rated connector
Data from DDU to DCC
TTC control bus

EMU FED: DDU Prototype

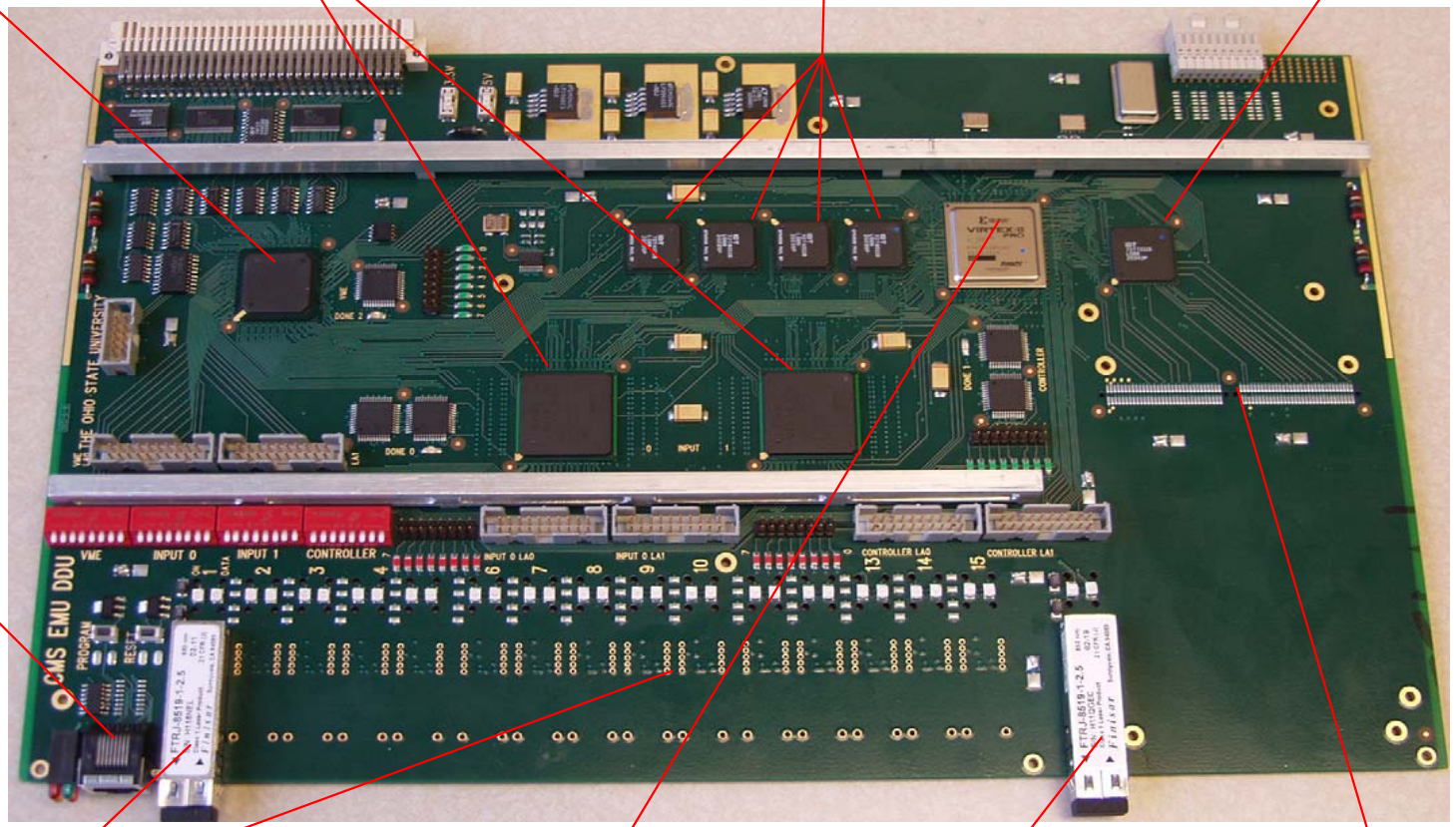
VME FPGA
XILINX Virtex2-500

DMB Input FPGAs
2 XILINX Virtex2Pro-20

4 Input FIFOs
512 KB each

GBE FIFO
1024 KB

9U VME board, 220 mm depth



FMM output port

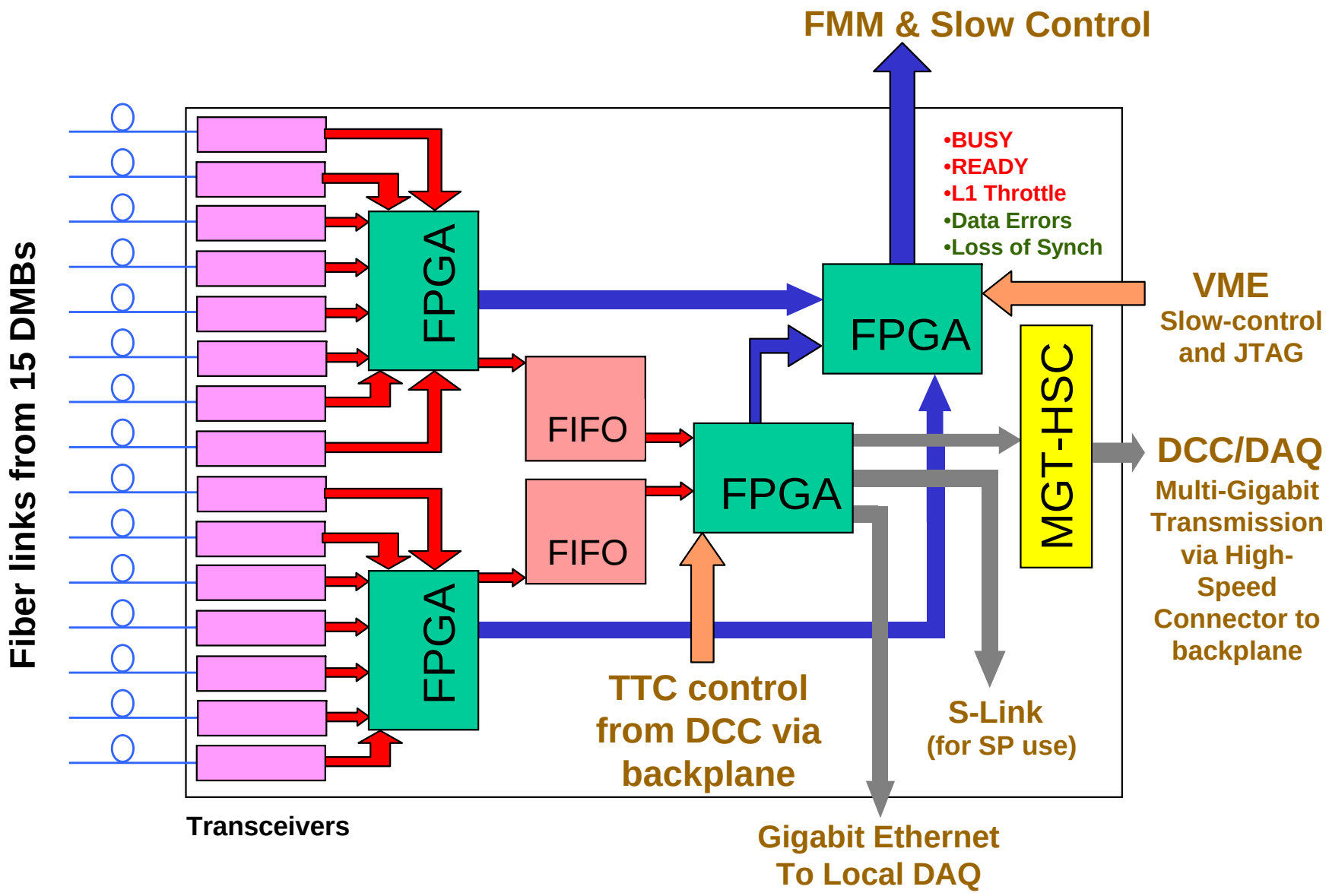
15 Optical fiber inputs (just 1 for now)

DDU Control FPGA
XILINX Virtex2Pro-7

Gbit Ethernet Output
To Local DAQ

SLINK Mezzanine board connector

EMU FED: DDU Plan



EMU FED: DDU Design (1)

- **DDU Functions**
  - **High-Bandwidth data concentration and buffering**
    - **13 DMB ⇨ DAQ via DCC, capable of continuous 600+ MB/sec rate**
    - **Parallel data readout via Gigabit Ethernet (local DAQ path)**
  - **Full error checking and status monitoring**
    - **CRC check, word count, L1 number, BXN, overflow, link status**
  - **FMM communication path for EMU DAQ**
- **DAQ Buffer capacity**
  - **Average EMU occupancy is ~3 CSCs with data per event at LHC**
    - **8 Byte event header sent from DMB for empty "no data" events**
      - Headers from empty events are zero-suppressed at DDU
    - **A typical DDU "data event" has 3 kB at LHC**
    - **Average event size in the DDU is 450 Bytes**
  - **Each DDU has 2.5 MB buffer: 20% in FPGA BRAM, 80% in FIFO**
    - **Typically enough to hold 2000 events at LHC**
    - **Typical event process time ~1 μsec**

EMU FED: DDU Design (2)

- **TTC clock & control from DCC via backplane**
- **Slow control via VME**
  - **Provides link to on-board serial/JTAG paths**
    - **Load firmware into on-board EPROMs**
    - **Load constants into on-board Flash memory**
      - Warning thresholds, offsets and Board ID
  - **Provides path for system-wide status monitoring**
    - **VME Controller can see "global overview" of all 36 DDUs**
    - **Allows fast detection/response for subtle effects**

DDU_STATUS_ERROR(32) in DDU-2004 Format

Note 1: In the table below, grouping and order of bits are based on their logical meaning. The error checks are expected to change as often as needed.
Note 2: Y/N in columns H and T indicates whether a particular DDU_STATUS_ERROR bit can/cannot be updated in Header3 and Trailer-2, respectively.
Note 3: Kinds of RESET (sync, hard) and on whether it happens on a single or multiple error occurrences are to be defined later.
Note 4: The most notable change wrt DDU-2003 Format: Bit37 has been completely redefined (and moved to another group of bits in this note).

	Bit	Short Description	Comments	H	T	Event Integrity S-link	Event Integrity SPY	RESET Req'd[5]
Input Data Transmission Errors/Warnings	56	No Live Fibers	No DDU fibers are physically connected.	Y	Y	no data	no data	Status Only
	34	Lost/New Fibers	Lost/New DDU fiber physical connections wrt the status after last Reset.	Y	Y	BAD	BAD	Reset Req'd
	55	One Event Bit-Vote Error	First event with a bit-vote failure per 64-bit word on an input fiber channel.	Y	Y	BAD	BAD	Status Only
	36	Second Bit-Vote Error	Second event with a bit-vote failure per 64-bit word on the same input channel.	Y	Y	BAD	BAD	Reset Req'd
	43	Hardware Bit Errors	Bit error detected in de-serializing hardware.	Y	Y	BAD	BAD	Reset?
	38	Timeout Error	Data from a fiber input either never started or never finished.	N	Y	BAD	BAD	Reset Req'd
DDU FIFO Errors & Warnings	44	INPUT FIFO Near Full	One or more DMB INPUT FIFOs or L1-FIFO are nearly full.	Y	Y	OK	OK	Status Only
	35	INPUT FIFO Full	One or more DMB INPUT FIFOs or L1-FIFO are full. Data/Sync. may be lost.	Y	Y	BAD	BAD	Reset Req'd
	58	L1A-FIFO Full	L1A-FIFO is full. Some triggers/events may be lost or garbled.	Y	Y	BAD	BAD	Reset Req'd
	57	Data Stuck in FIFO	One or more INPUT FIFOs have data, but no trigger was received.	Y	Y	BAD	BAD	Reset Req'd
	63	DDU Output Constricted	Any of input FIFO going full because of a request from DCC not to send data.	Y	Y	BAD	BAD	Reset Req'd
FPGA	42	Control FPGA Clock-DLL Error	DDU lost its clock for some time; some S-Link and SPY data may have been lost.	Y	Y	OK?	OK?	Reset Req'd
DMB Event Structure/Content Errors & Warnings	59	Wrong First Word	First word for at least one FIFO is inconsistent with the first word signature	Y	Y	BAD	BAD	Status Only
	39	Corrupted Control Word Sequence	Detected wrong control word sequence, probable fatal data loss or mixed event data[6]	N	Y	BAD	BAD	Reset Req'd
	40	Missing Control Words	Failed to find expected control words within an event[7]	N	Y	BAD	BAD	Status Only
	33	DMB-DDU L1A Mismatch	DMB-DDU L1A event numbers mismatch for at least one CSC	Y	Y	BAD	BAD	Reset?
	37	TMB/ALCT CRC Error	TMB/ALCT CRC check failed	N	Y	BAD	BAD	Reset?
	48	TMB/ALCT-DDU L1A Mismatch	TMB/ALCT-DDU L1A numbers mismatch for at least one CSC	N	Y	BAD	BAD	Reset?
	49	TMB/ALCT Word Count Error	TMB/ALCT word count inconsistent	N	Y	BAD	BAD	Reset?
	50	ALCT Error	ALCT DAV exists, but: (no ALCT Trail).or.(ALCT-DDU L1A error).or.(CRC-error).or.(Word Count error)	N	Y	BAD	BAD	Reset?
	51	TMB Error	TMB DAV exists, but: (no TMB Trail).or.(TMB-DDU L1A error).or.(CRC-error).or.(Word Count error)	N	Y	BAD	BAD	Reset?
	32	CFEB CRC Error	CRC-error for ADC time-sample data on one or more CFEBs	N	Y	BAD	BAD	Reset?
	41	CFEB Lost Samples	B-code encountered in at least one DMB/CFEB (SCA Full Condition)	N	Y	BAD	BAD	Status Only
OR	45	DDU Single Event Warning	Problem detected, possibly not bad or fatal error (can be modified, now set to be OR of bit55, bit42)	Y	Y	OK?	OK?	Status Only
	46	DDU Single Event Error	OR of all possible "bad event" cases.	Y	Y	BAD	BAD	Reset?
	47	DDU Critical Error	OR of all possible "RESET required" cases.	Y	Y	BAD	BAD	Reset Req'd
S-link Errors	52	S-Link Not Ready	No active S-link connection, no will be sent via S-Link (bit52=1 can be seen only in SPY data; SPY data are OK)	Y	Y	no data	OK	Status Only
	53	S-Link Full Bit Present	Data will not be sent if "active S-link" is present (bit53=1 can be seen only in SPY data steam)	Y	Y	no data	OK	Status Only
SPY-ing Errors	54	SPY FPGA Clock-DLL Error	SPY FPGA lost its clock for some time; some SPY data may have been lost/wrong.	Y	Y	OK	OK?	Status Only
	60	SPY Fiber Error	Fiber connection is not present. Does not affect S-Link data flow.	Y	Y	OK	no data	Status Only
	61	SPY FIFO Near Full	Giga-Bit Ethernet FIFO is close to being full.	Y	Y	OK	OK	Status Only
	62	SPY FIFO Full	Cannot get full if DDU operates properly. Does not affect S-Link data flow.	Y	Y	OK	BAD	Status Only

[5] Error bits resulting in RESET REQUIRED persist until the RESET occurs. Questionable cases (in gold) are for mitigation of recurring errors. TBD: sync/hard reset distinctions.
[6] Found inside an event at least one of the following: Extra DMB_Header1, Extra DMB_Header2, Lone Word, Extra TMB/ALCT_Trailer, Extra DMB_Trailer1, DMB_Trailer2
[7] Missing TMB/ALCT_Trailer word, missing DMB Header word, Wrong First word, or Extra Control words.

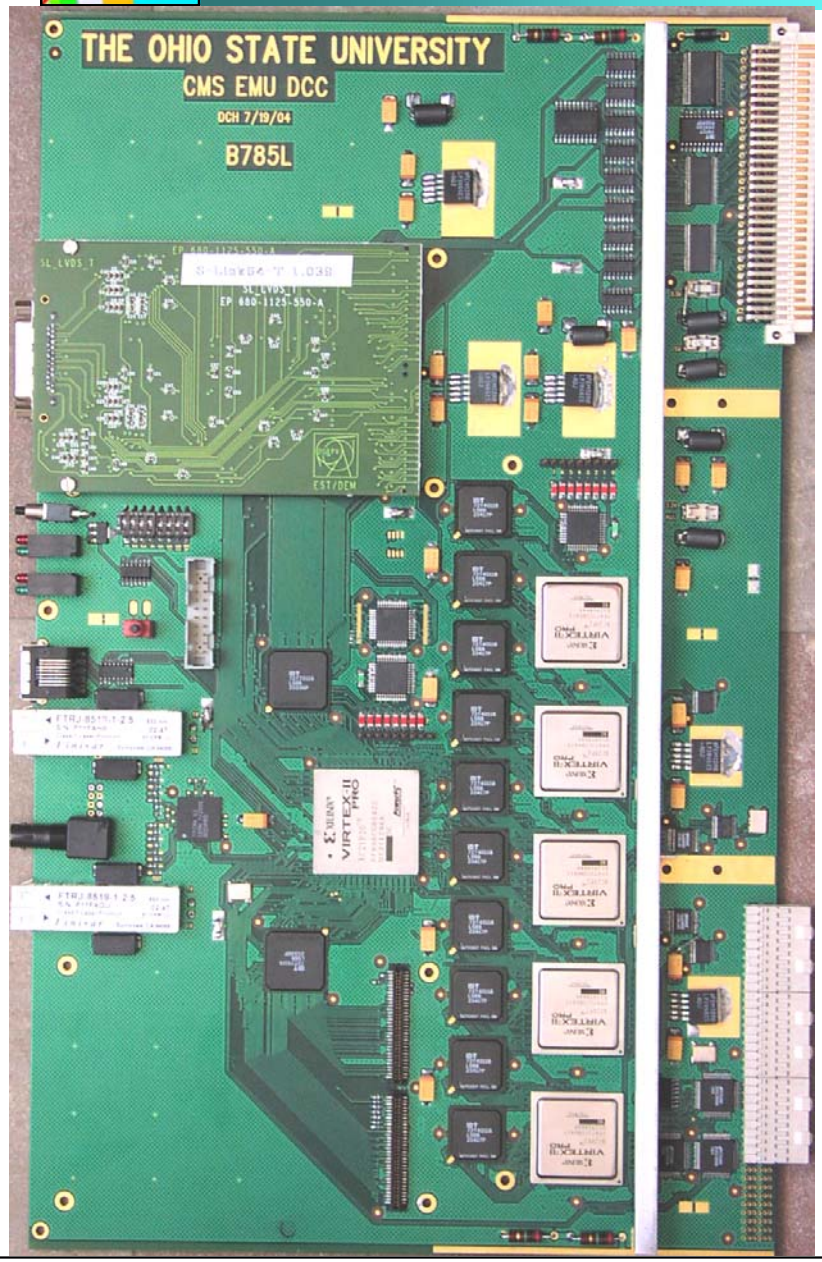
EMU FED: DDU Performance

- **Oct. 2004 Beamtest results: no problems**
  - **Multiple DMB readout to DAQ**
    - **Good performance via DCC/S-Link and gigabit Ethernet spy path**
  - **Error-free operation at high rates**
    - **Muon rates at H2 beam up to 25 kHz**
    - **Passed all tests at 9-times LHC expected data rate**
    - **DDU buffer size is more than sufficient for LHC**
  - **Status/error monitoring**
    - **All checks performed as expected, verified in offline software**
    - **Verified consistent fast monitoring path performance**

EMU FED: DDU Testing Procedure

- Receive board from assembly house
- Load the VME_FPGA PROM
- Load the DDU_Ctrl PROM
- Load the InFPGA PROM
- Read in the board ID from PROM user code
- Every time after RESET, the DDU will be in a ready state
- Before LHC run, download a BX_Number offset through VME slow control, so the BX_number will match between DDU, DMB and other peripheral crate electronics
- EMU needs 36 DDUs plus spares

EMU FED: DCC Function



Each DCC serves 1/4 of EMU
9 DDU, 2 SLINK64

Data Concentration

- Merge 10 DDUs data into two slink64, two optional gigabit spy path

Fast Control

- Receive TTC fiber signals using TTCrx, send L1A CMS_clock and other TTC command to FED crate
- Optional FMM interface

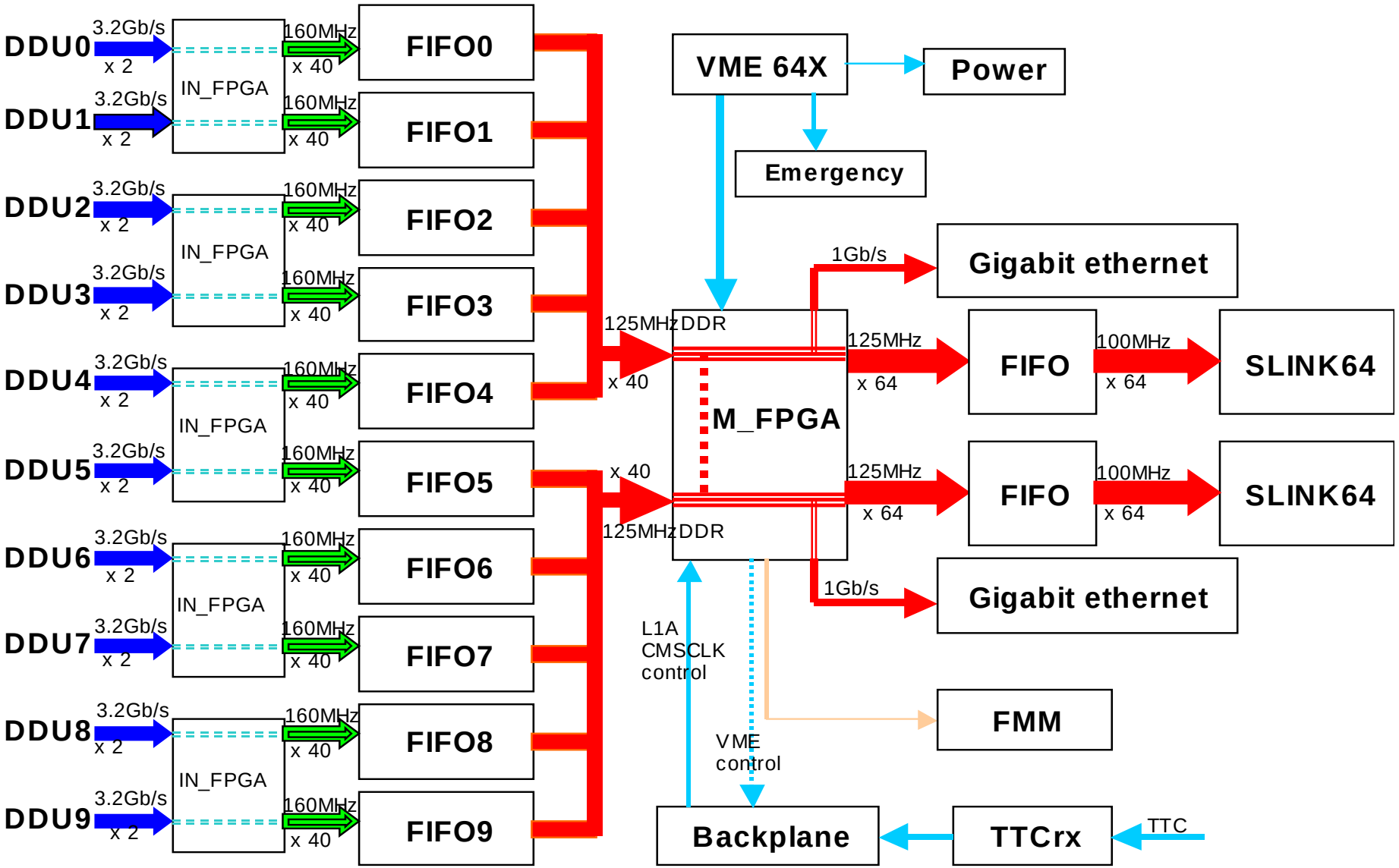
Slow Control

- VME Slave

Misc.

- 9U x 220mm VME slave
- +5V (<1A), +3.3V (~6A)
- Regulators for +2.5V, +1.5V, +1.5V

EMU FED: DCC Data Acquisition



EMU FED: DCC Few Extra features

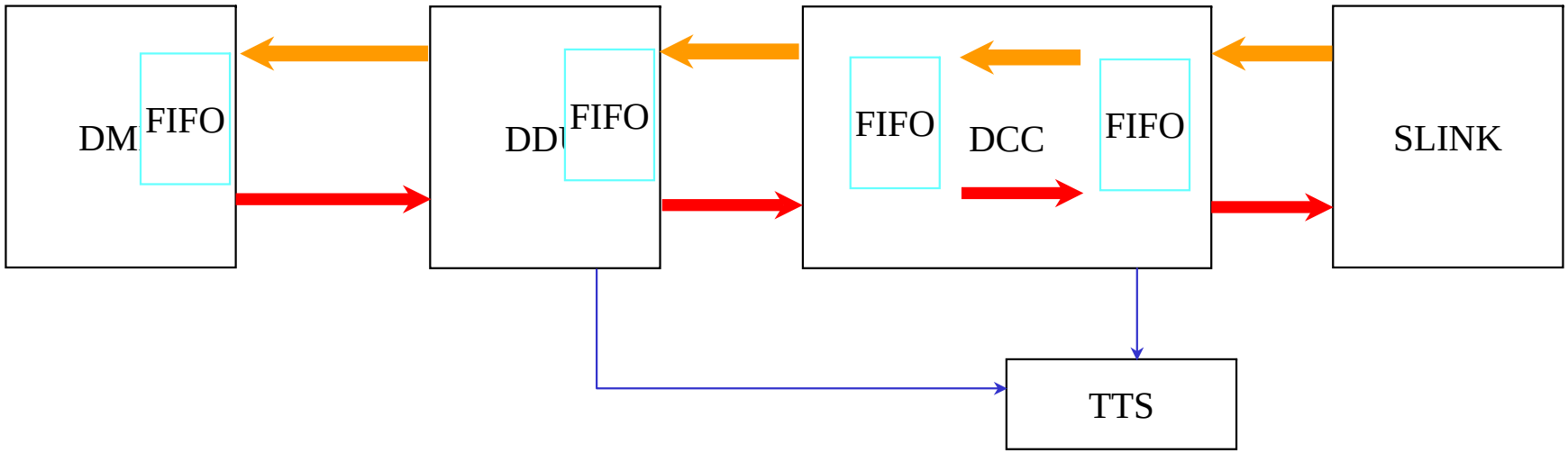
9Mb FIFO to buffer the data from FPGA to SLINK transmitter:

- **This will keep the speed on data readout at 1GByte/s, and SLINK throughput at 800MByte/s**
- **It serves as a storage, to even out the L1A fluctuation**

DDR FIFO keeps the same data rate using less number of wires.

The DCC has the ability to combine the two sets of FIFO inputs and send the data to one SLINK transmitter.

Data transmission backpressure:



EMU FED: Data Back pressure

When Slink is full, the DCC will stop sending data to Slink, the data will be buffered at the DCC S_FIFO,
When the DCC S_FIFO is 'Almost_full', it will stop the DCC assembling events. The data will backup on the IN_FIFO;
When the IN_FIFO gets to a certain point, it will backpressure on DDU, the DDU will stop sending data to DCC. The data will be backup on DDU;
When DDU FIFO get to a certain point, it will backpressure the DMB, and send warning signals through FMM to TTS.
If the DMB FIFOs will be monitored by DDU, and the DMB can also disable the trigger sending to CFEB in case the DMB FIFO close to full.
If the TTS does not respond to DDU warning, the DDU will send data to DCC to prevent DDU FIFO get full, the DCC will only receive and process data header/trailer to prevent FIFO get full, and at the same time, keep the data package integrity.
This mechanism should give sufficient time for TTS to respond.

EMU FED: DCC Data Acquisition

On L1A (Data is always sent on L1A)

DDU sends data to DCC asynchronously (relative to L1A)

DCC assembles data from DDUs into events and sends to FRL asynchronously

LV1_ID(24), Bx_id(12) and Orbit_ID(32) are used to identify the event

EMU DCC Event Size:

no data	~300 bytes
1 CFEB	~3 Kbytes
5 CFEB	~10Kbytes
Average	~2 Kbytes
max_size	800 Kbytes

DCC Data format:

	63…60	59..56	55……32	31……20	19……8	7…4	3..1	0
Header 1:	K 5	Evty	LV1_ID (24)	Bx_id (12)	source_id	FOV	Hx$$	
Header 2:	K D	9	Orbit_ID (32)	FIFO_stat(16)	9	7		
Data Load	D	……						
Data Load	D	……						
…….								
Data Load	D	…….						
Trailer 2:	K E	F	D_time(8)	DDU4(8)	DDU3(8)	DDU2(8)	DDU1(8)	DDU0(8)	FIFO_s(8)
Trailer 1:	K A	X	Evt_lgth(24)	CRC(16)	X	Evt_S	TTS	Tx$$	

EMU FED: DCC Slow Control

VME A24/D16 in VME64X P1 Backplane

- A[23:19] match with GA[4:0] for specific slot, broadcast.
- A[18:12] is used to address the different slow control paths (devices)
- A[11:1] are specific to the given device

A[18:12] device definition:

00: VME registers on the FPGA
02: JTAG for Controller PROMs
03: JTAG for IN_FPGA's PROM
04: JTAG for IN_FPGA
05: JTAG for SLINK_A
06: JTAG for SLINK_B
07: TTCrx I2C interface
0F: Emergency load for Controller PROMs

The DCC are always VME controllable even after FPGA ISPROM get SEU

EMU FED: DCC Fast Control

Custom Backplane carries all Fast control Signal

Fast control signals TO the backplane (Bus_LVDS):

- TTCrx on board, automatically select the TTC clock or the on-board oscillator as 40MHz source, four segments on the backplane
- Automatically select TTC L1A, command bus or on board VME generation
- The command bus and Data bus are switched, depending on the command_bus_strobe and Data_bus_strobe
- Summary of backplane signals: Clock, L1A, Command_Strobe, Data_Strobe, Cmd_Dat_Bus(8), Hard_reset

Fast control signals FROM the backplane (Bus_LVDS):

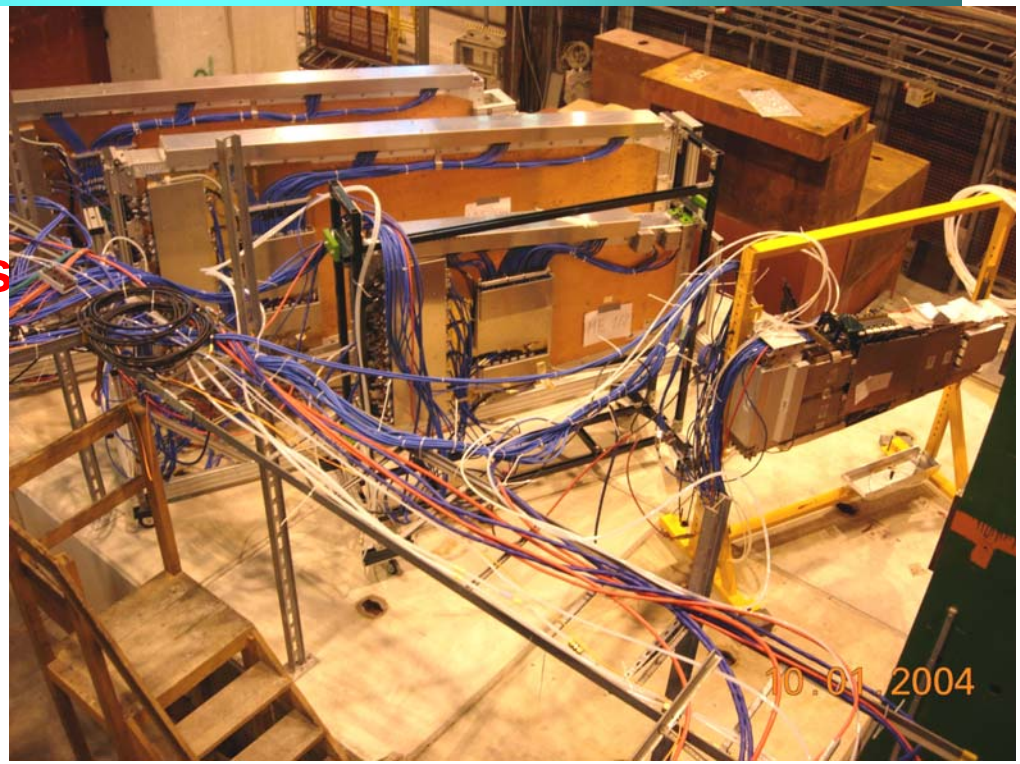
- Clock, L1A, Command_Strobe, Data_Strobe, Cmd_Dat_Bus(8)

Only one DCC is enabled for control signals to the backplane

EMU FED: DCC Structure Beam Test

Sept/Oct. 2004, H2 beams

- **TTC control – no issues**
- **Backplane communications – no issues**
- **Synchronization – no issue**



DCC rate tests carried out with high trigger rate.

– 100 KHz L1A (TTCvi random trigger), >100 KHz LCT (lowering the comparator threshold to 2mV), FakeDDU sends 2.3KB per L1A, The DDU sending five chambers data, this gives >240MB/s data rate to SLINK. Check the L1A_number, Event size, 1/1000 write to disk and check synchronization offline. No Problem on DCC.

EMU FED: DCC tests: Some issues

On the DDR FIFO, there are internal cross talk from D22 to D21 line. Get around: do not use D21, we only need 33 bits out of 40bits on the FIFO.

The DDR FIFO works at 125MHz reading speed, but the manufacture downgraded its rating to 100MHz. Solution: Even 100MHz (800MB/s) is good enough for our application (Slink ~200MB/s)

At the CERN beam test, we do not have a readout system fast enough to handle the 200MB/s data, required by SLINK, this is not a real problem.

EMU FED: DCC Bench test

By plugging the DDU in different slot of the FED crate, all the ten DCC inputs are tested, and the two slink outputs are tested.

Because the FED crate are in underground counting house, there is no need for radiation test and magnetic test !

EMU FED: DCC procedures

- VME emergency load the Main_FPGA PROM
- VME load the IN_FPGA PROM
- The FPGA read in the board ID from PROM usercode
- Load in the channel enable (DDU_in_use)
- Every time after RESET, the DCC will be in a ready state
- During LHC run, download a BX_number offset through VME slow control, or set the delay on the TTCrx, so the BX_number will match between DCC, DDU and peripheral crate electronics.

EMU FED: Production preparation

- **How many boards do we need?**

DDU	DDU needed	36 + 1
	Total (+ 20% spare)	45
DCC	4/5/9 DDU per Slink	4
	(2/3 DDU per Slink	8)*
	spare boards	2
	Total boards producing	10

* This is just for very high data rate, requires 16 SLINK64

- **The Ohio State University will maintain the DDU and DCC**
- **some spare parts will be ordered in addition to the spare board for anticipated repair**

EMU FED: Production Test

PC boards will be etched and stuffed commercially

Boards will be measured and debugged on computerized tester before and after burn-in at OSU

Each board will have a unique ID

Board tracking: Microsoft Access

To test the DDU:

-Read DAQMB will be used as DDU input source, DCC as output destination

-Check all inputs by moving fiber from connector to connector

-Check Gigabit readout (spy path) by computer readout

To test the DCC:

-DDU signals mimicked by 'fakeddu'

-Check all inputs by moving 'fakeddu' from slot to slot

-Check all outputs by moving SLINK transmitter card

After we have enough DDUs, the full FED crate will be tested

EMU FED: Production Burn in

Burn In

CDF: 50-60 C for 8-24 Hrs
Sufficient for tantalums failures
No sensitivity to semiconductor failure

US Military: 125 C for 320 Hrs
Chip Makers recommend against this

CFEB, DAQMB: 65 C for 24 Hrs
Prove to be effective, not damaging

Each DDU/ DCC: 65C for 24 Hrs

Test Before and After

EMU FED: Production Validation

-First DDU was made in Jun. 2002

-Redesigned DDU was made in Jan. 2004

-Both boards are working reliably.

-First DCC was made in Jan. 2004

-Second DCC was made in April 2004 with minor change

-Both boards are working.

The full production will be procured after full FED crate test

DDU, DCC Meet Design Specifiations!

We are ready to procure the DDU and DCC At The Ohio State University

EMU FED: DDU & DCC Documentation

http://www.physics.ohio-state.edu/~cms/ddu/

- What is it?
  - EMU DDU details
- DDU Operation
  - General Hardware Info
  - Technical Operation Details
  - DDU Data Format

http://www.physics.ohio-state.edu/~cms/dcc/

- DCC User's Manual
- DCC ESR at CERN (Powerpoint)
- DCC PCB schematic design (pdf)
- DCC Data receiver FPGA design (latest version .svf) (pdf)
- DCC Slink interface FPGA design (latest version .svf) (pdf)
- DCC Output (Slink, Gigabit Ethernet) data format