

In5Ctrl (file Oddu_in)10-15-2013_14:12

CMS CSC DDU5, Input Control FPGAs DF026A01 Version 26

Process Rocket I/O Data from DMB, format output to DDU FIFOs

this DDU:

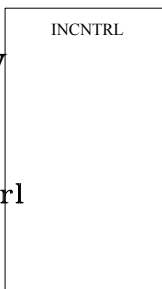
- RXER words are skipped, FILLER added as needed
- Use code "C" with FILL flag set (b34 & b16)
- could use code "8" instead...
- Should we Reset RxErr Monitor? How?

- v22: replace F_OK with LFOK for InUnits
- r2, use FDP for LFOK; r3, use FOK to control GT PwrDr
- v23, RxErr sets SingleWarn, but LRxErr goes on Stat11, Lfilled on Stat30, LDLLerr on STAT31
- v24: Tune RdBusy logic, extend RHL to 1200ns; r2: add Search/Free Errorrdetection to FMM & L1m2b7
- r3: add REN-while-StackMT error to FMM & L1m2b7; r4: new LA signals on 2H
- r5: try OEF_F/REN_F fix in RdCtrl.9, allows Fiber/NextMem bookeeping when FIFO Empty at EO
- r6: add mode 8-F options for LAs & LEDs; r7: add RstEOE to OEM_fctrl counter, bring BadFW to L0m
- v25: RdCtrl.9 disable LnxTFFIFO until NextFiber+6, prevents Previous fiber moving Current Read pointer
- r2: Now SCAovfl (DMBerr) does Not set SingleError at InFPGA. r3: modified XMITerr def
- r4: DMB FIFO Full no longer sets WARN. r5: fix Reset for InUnit filler/word-phase counter
- r6: prevent LastFill for single 8-code case

PART=XC2VP20-6-FG676

AVOID=Y21, E23, C22, E21
(INIT, BUSY, WRITE, CS)
NC_XCV400_FG676=B13, AF13
NC_XCV400E_FG676=D13, Y13

All I/O is 3.3V



Mode 1 Switch Block

- 1: Mode Bit 0
- 2: Mode Bit 1
- 3: Mode Bit 2
- 4: Mode Bit 3
- 7: Set Fake_L1A (data passthrough)
- 8: Show STAT31-0 on LAs, ~FPGA version on LEDs

PROM=2*XC18V04-VQ44 (PARALLEL)

DDU5in\In5Ctrl\in5ctrl

* af_clb_5x31rpm has Core EDN file

PROGRAM takes < 55ms

NEED TO Change FIFO Full, lost sync NOT Warning....done?

VME Broadcast Addresses:

- 24=OSU-TCB "Test Control Board"
- 25=DMB
- 26=TMB
- 27=Both DMB and TMB
- 28=DDU
- 22=DCC

PromID: 05026093h
FPGAid: 31266093h

ELECTRONICS LAB
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
174 WEST 18TH AVE
COLUMBUS OHIO 43210

- To Do:
- COMPARE LINUM & BXN (DMB/TMB too)
 - add BX_offset constants to SRAM?
 - use DDU-DMB fiber to STOP DMB on FULL, check
 - Watch for TRG buff overflows
 - No logic for TXEN, TXDIN, PAE0/1, Mode5/4...OK.
 - Add InUnit Check for DMB Timeouts & set FMM Error

Special Startup Order:

- 2) Release WE
- 3) Release DLL
- 5) En. Outputs
- 6) DONE

DDU Format Since DDUctrl v15:

H1: 0x/51/NN.NNNN/XXX/1.II/VK
H2: 0x/8000/0001/8000/HHHH
H3: 0x/LLLL/0000/ZZZZ/GGMY

T-2: 0x/8000/FFFF/8000/8000

T-1: 0x/SSSS.SSSS/QQQQ/PPPP

TR: 0x/A/?/WW.WWWW/RRRR/UUMK

DDU WordCount (64-bit words) for "No Data" event: 0x006.
DDU WordCount for one DMB (only one CFEB): 0D2h = 210 dec, 1680 Bytes
DDU WC, 1 DMB with 2 CFEB (8 samples each): 19Ah = 410 dec, 3280 Bytes
DDU WC, 2 DMB with 1 CFEB (nCFEB=2): 19Eh = 414 dec, 3312 Bytes
DDU WC, 2 DMB with 2 CFEB (nCFEB=4): 32Eh = 814 dec, 6512 Bytes

DDU_WordCount = (6 + 25*Nts*nCFEB + 4*nDMB) < 30070: 240560 Bytes

Ignore TMB Data GBE ByteCount = 8*DDU_WordCount 8 TS assumed

DDU WC, 3 DMB with 1 CFEB (nCFEB=3): 26Ah = 618 dec, 4944 Bytes
DDU WC, 4 DMB with 1 CFEB (nCFEB=4): 336h = 822 dec, 6576 Bytes
DDU WC, 7 DMB with 1 CFEB (nCFEB=7): 59Ah = 1434 dec, 11472 Bytes
DDU WC, 8 DMB with 1 CFEB (nCFEB=8): 666h = 1638 dec, 13104 Bytes

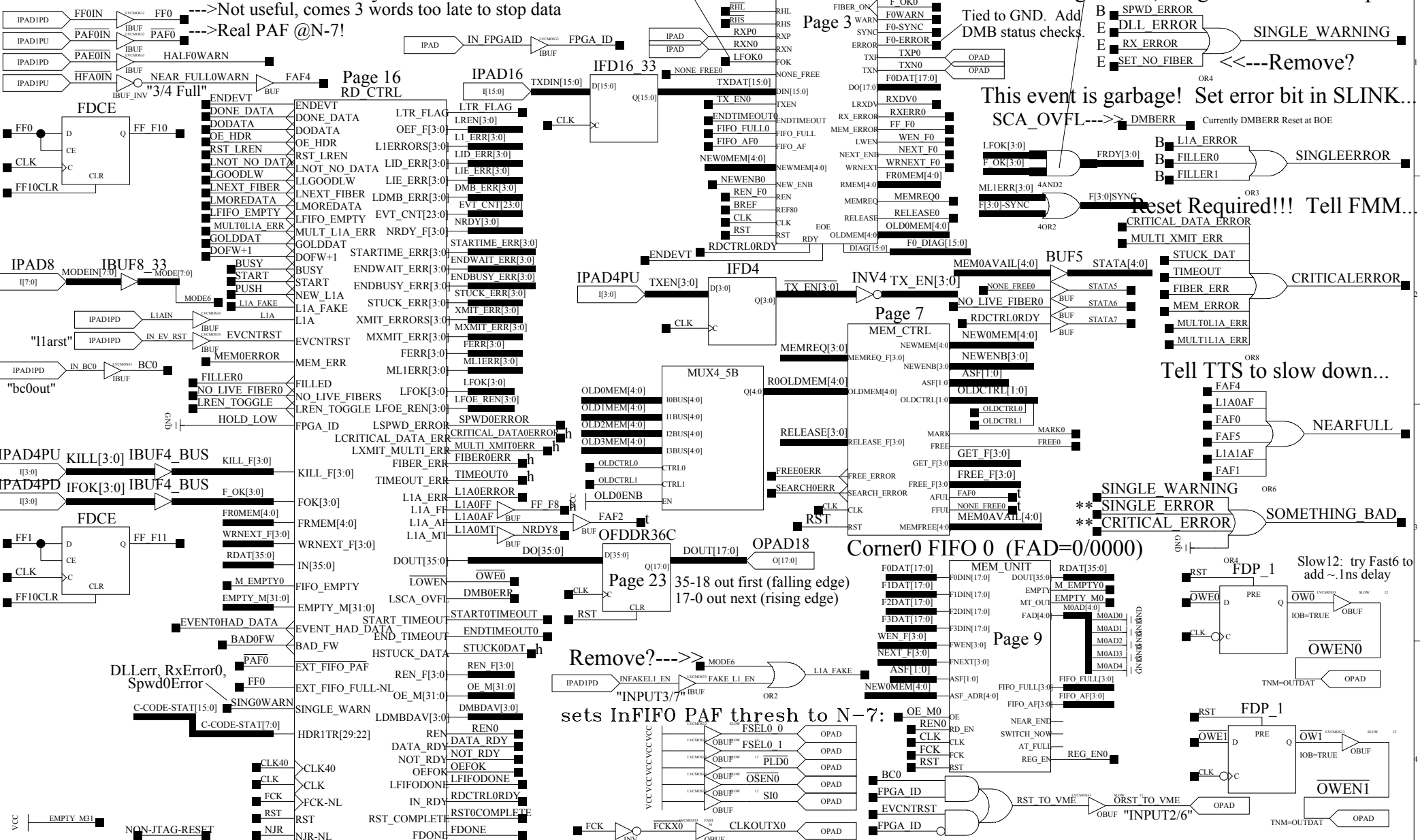
DDU WC, 11 DMB with 1 CFEB (nCFEB=11): 8CAh = 2250 dec, 18000 Bytes
DDU WC, 12 DMB with 1 CFEB (nCFEB=12): 996h = 2454 dec, 19632 Bytes
DDU WC, 15 DMB with 1 CFEB (nCFEB=15): BFAh = 3066 dec, 24528 Bytes

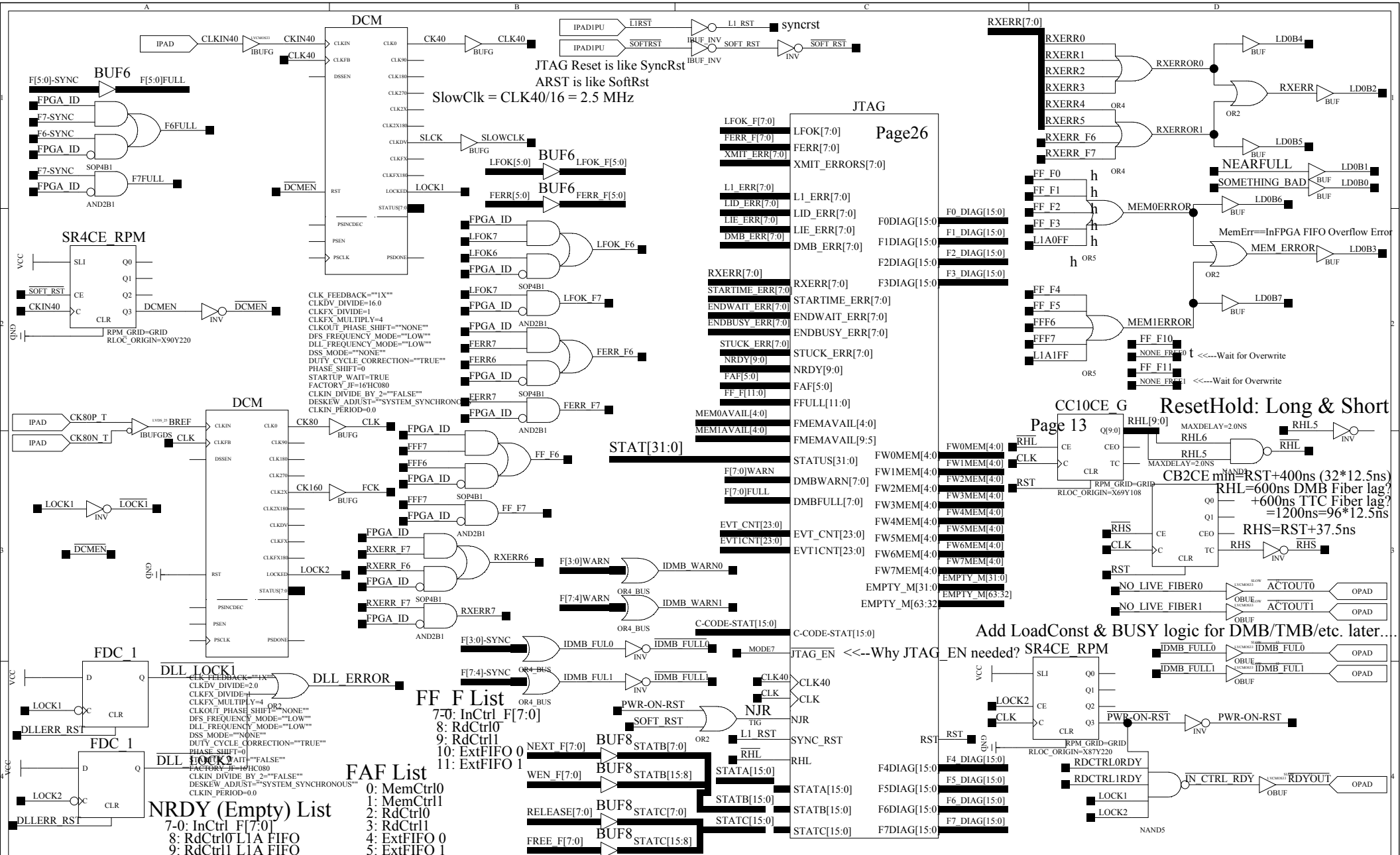
Later use FRDY logic to determine when InUnit is killed; allow real-time Kills (until Reset) in case of Errors/Glitches?

Mask DMBs with critical error until they're Reset?

For now just use LFOK.

Single error, insignificant unless repeated





DCM

JTAG Reset is like SyncRst
ARST is like SoftRst
SlowClk = CLK40/16 = 2.5 Mhz

JTAG

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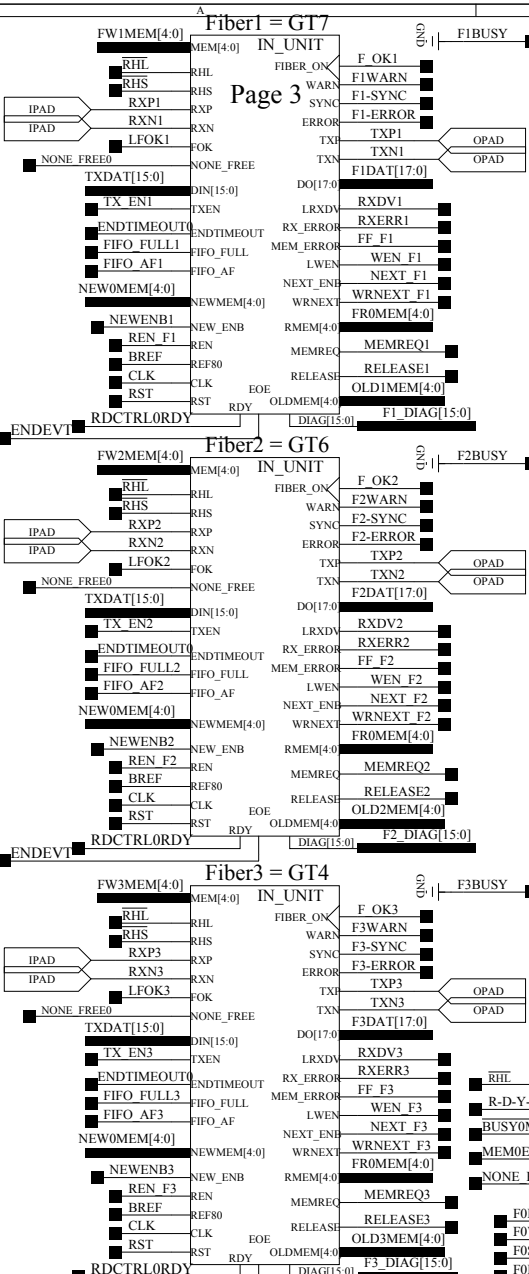
ResetHold: Long & Short

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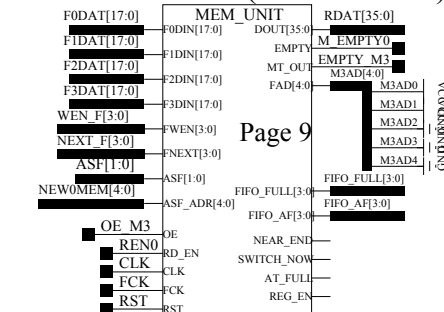
NRDY (Empty) List
7-0: InCtrl F[7:0]
8: RdCtrl0 L1A FIFO
9: RdCtrl1 L1A FIFO

FAF List
0: MemCtrl0
1: MemCtrl1
2: RdCtrl0
3: RdCtrl1
4: ExtFIFO 0
5: ExtFIFO 1

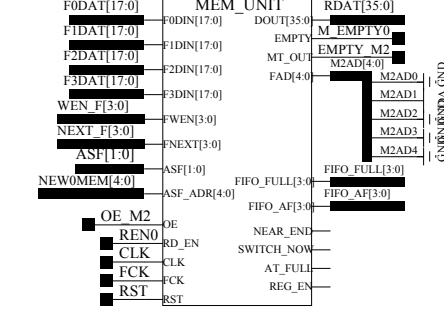
FF F List
7-0: InCtrl F[7:0]
8: RdCtrl0
9: RdCtrl1
10: ExtFIFO 0
11: ExtFIFO 1



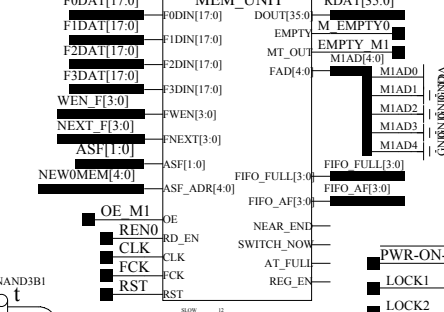
Corner0 FIFO 3 (FAD=0/0011)



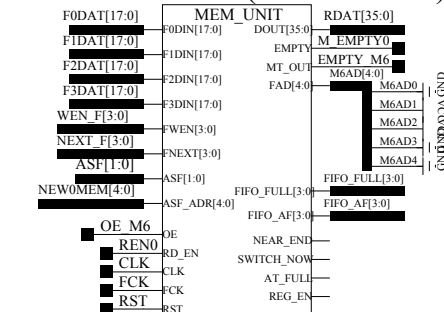
Corner0 FIFO 2 (FAD=0/0010)



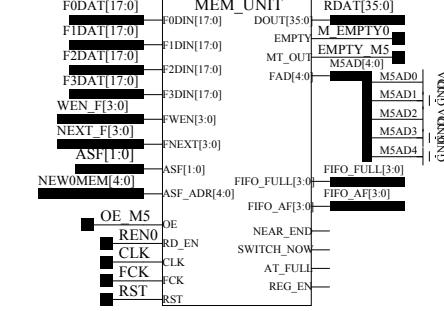
Corner0 FIFO 1 (FAD=0/0001)



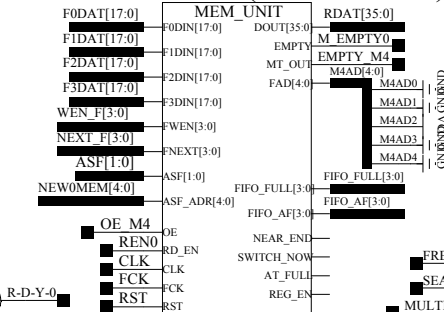
Corner0 FIFO 6 (FAD=0/0110)



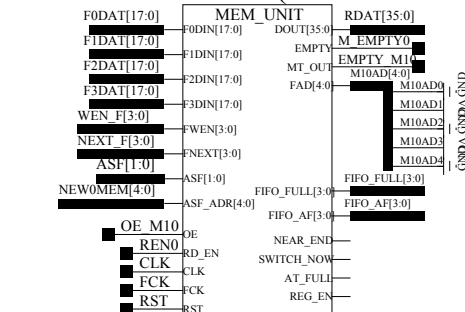
Corner0 FIFO 5 (FAD=0/0101)



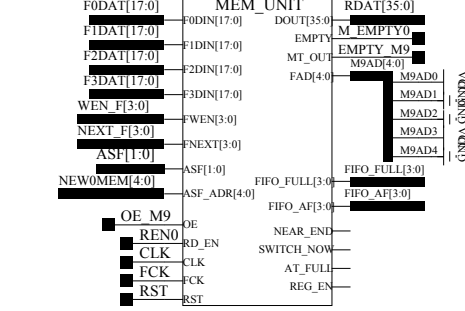
Corner0 FIFO 4 (FAD=0/0100)



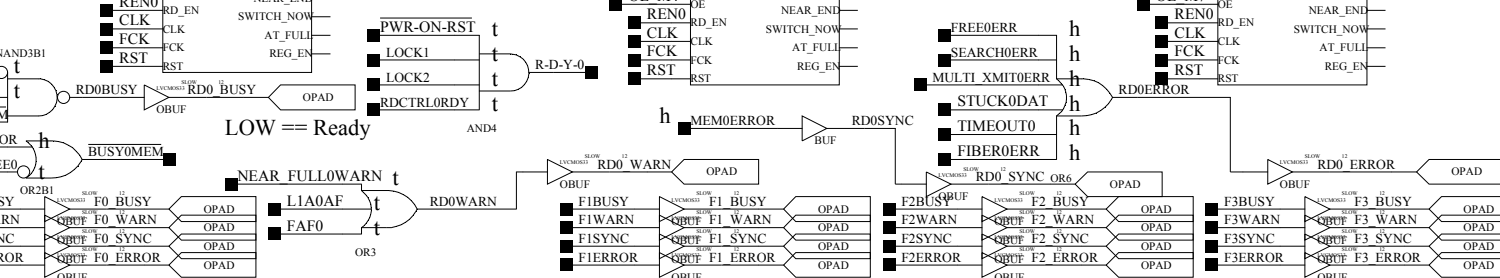
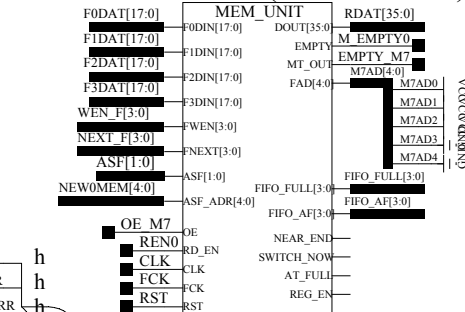
Corner0 FIFO 10 (FAD=0/1010)



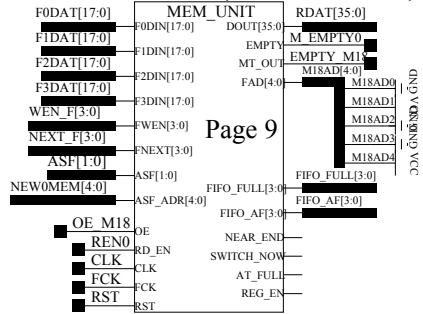
Corner0 FIFO 9 (FAD=0/1001)



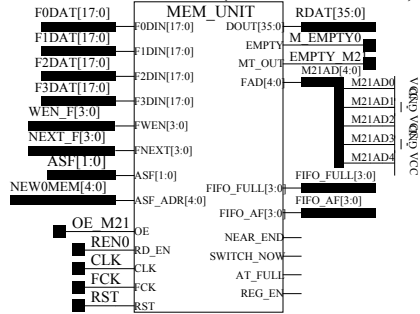
Corner0 FIFO 7 (FAD=0/0111)



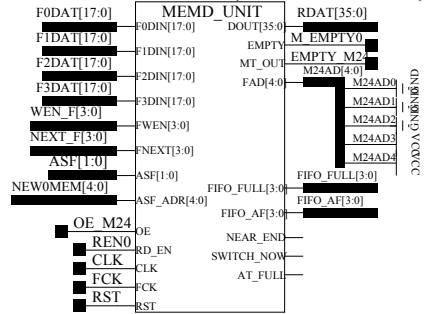
Corner1 FIFO 2 (FAD=1/0010)



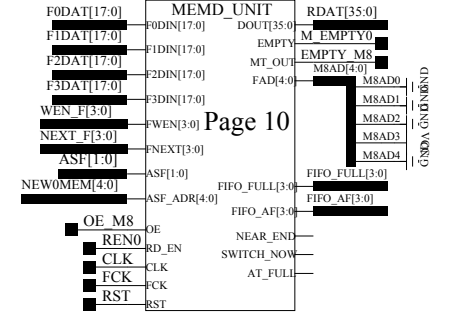
Corner1 FIFO 5 (FAD=1/0101)



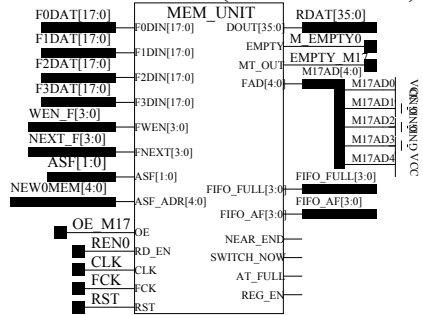
Corner1 FIFO 8* (FAD=1/1000)



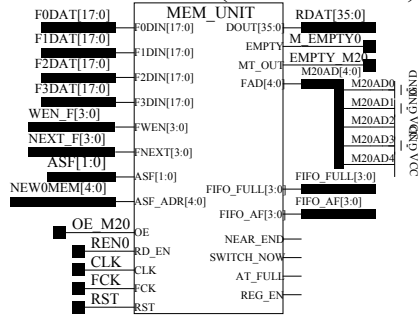
Corner0 FIFO 8* (FAD=0/1000)



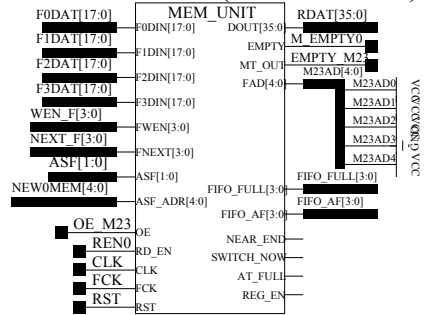
Corner1 FIFO 1 (FAD=1/0001)



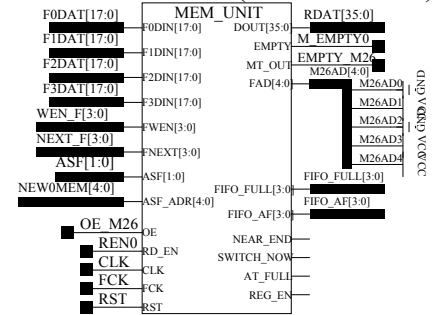
Corner1 FIFO 4 (FAD=1/0100)



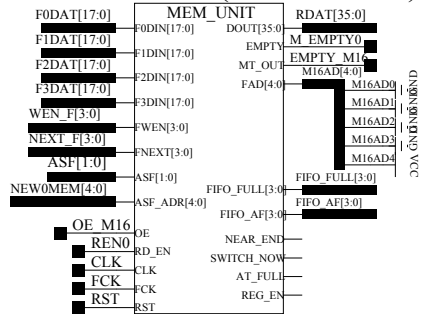
Corner1 FIFO 7 (FAD=1/0111)



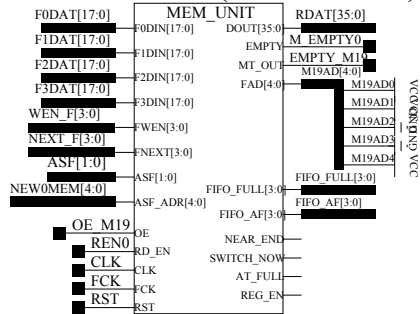
Corner1 FIFO 10 (FAD=1/1010)



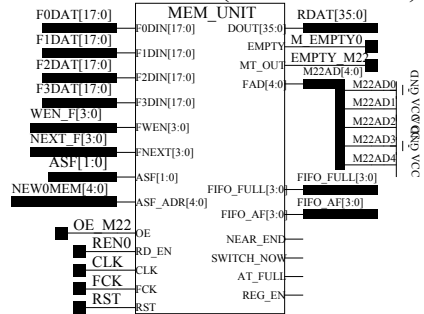
Corner1 FIFO 0 (FAD=1/0000)



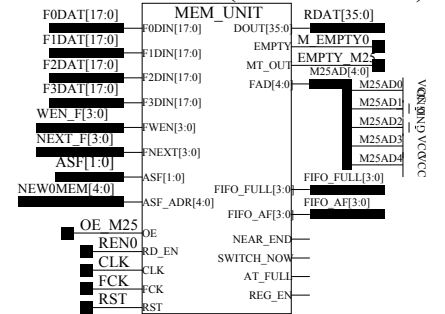
Corner1 FIFO 3 (FAD=1/0011)

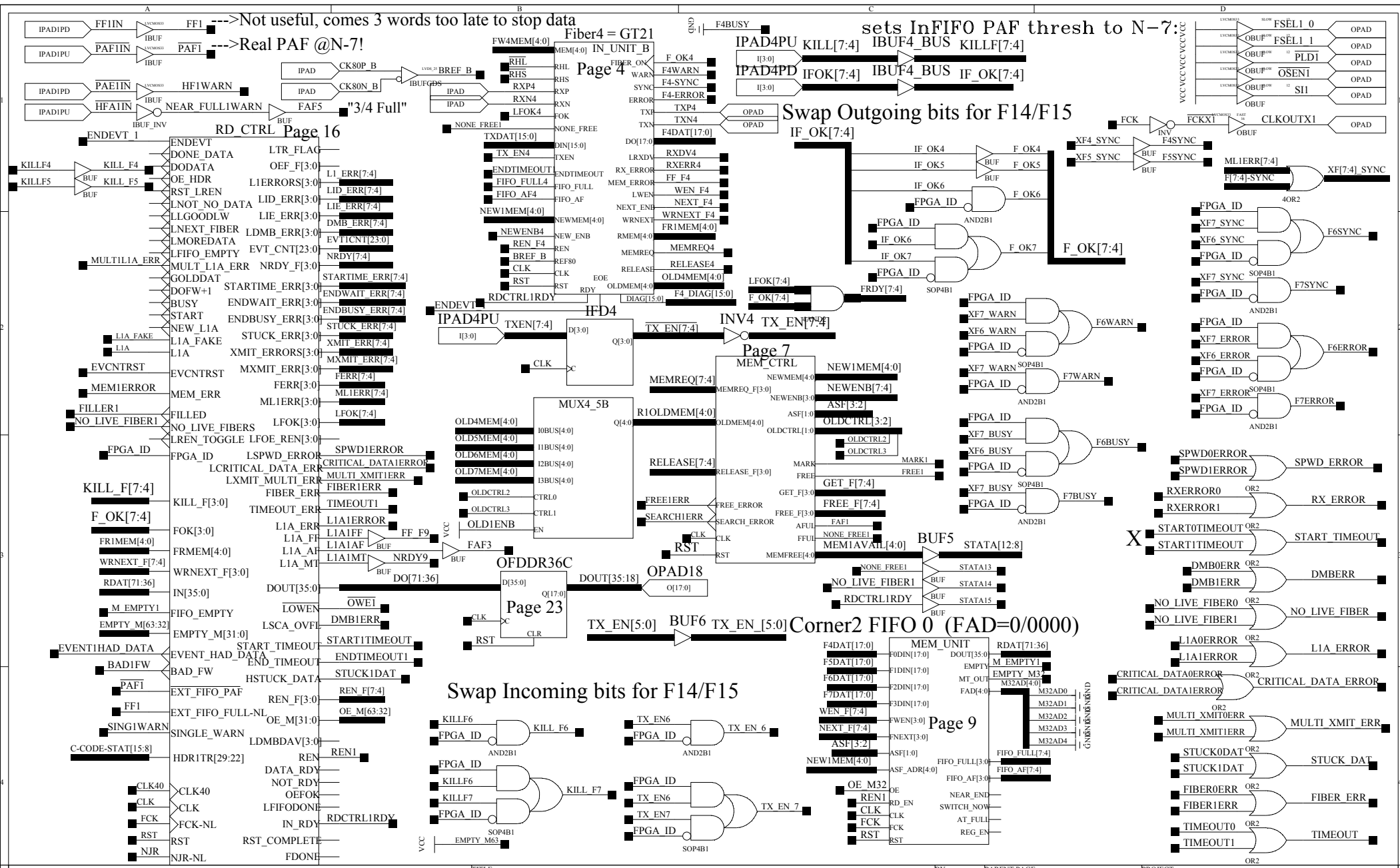


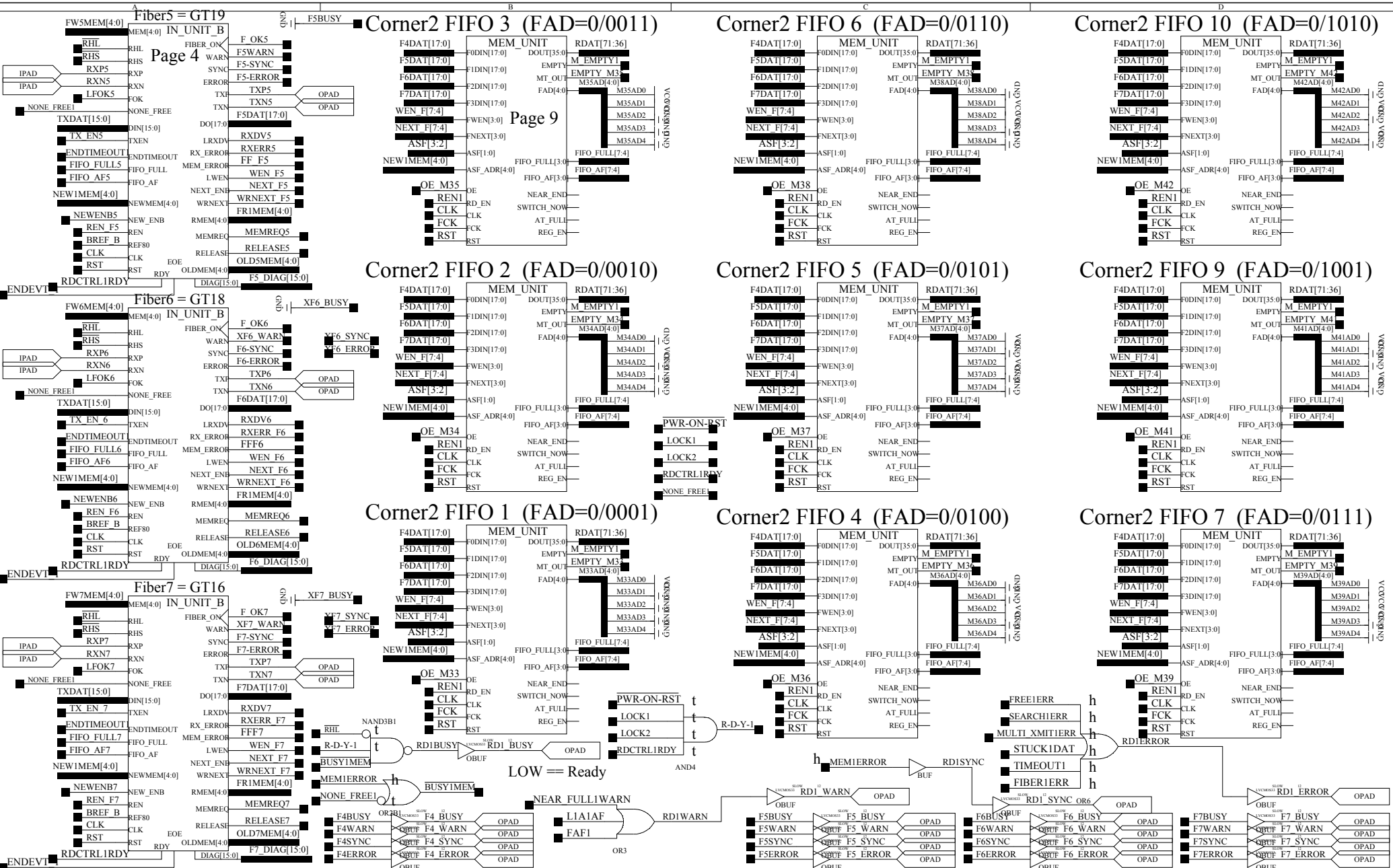
Corner1 FIFO 6 (FAD=1/0110)



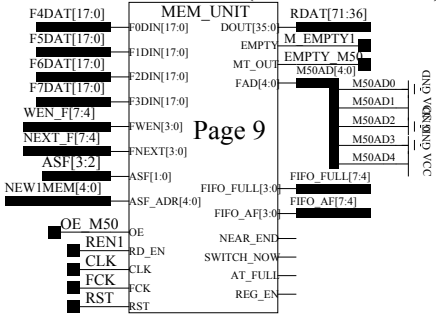
Corner1 FIFO 9 (FAD=1/1001)



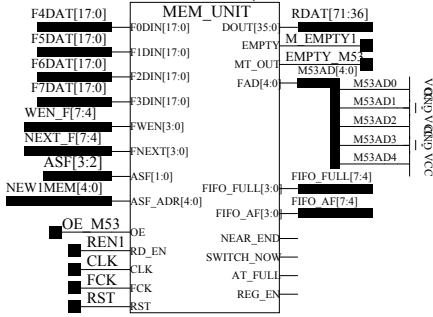




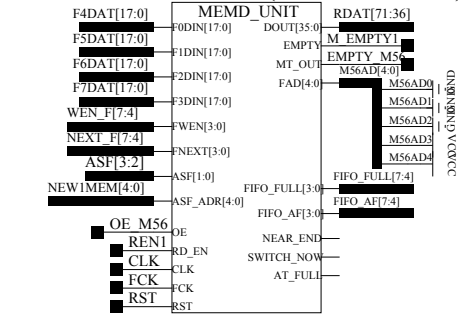
Corner3 FIFO 2 (FAD=1/0010)



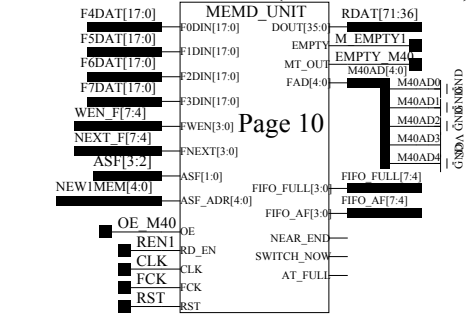
Corner3 FIFO 5 (FAD=1/0101)



Corner3 FIFO 8* (FAD=1/1000)

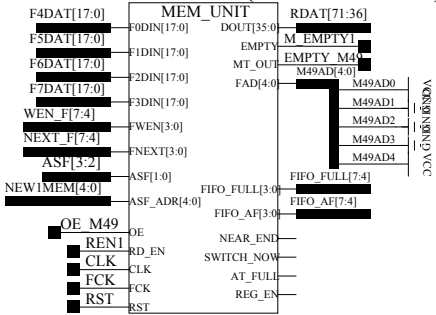


Corner2 FIFO 8* (FAD=1/1000)

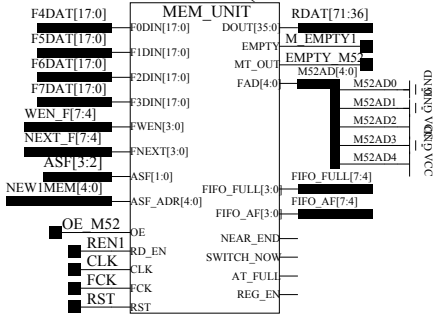


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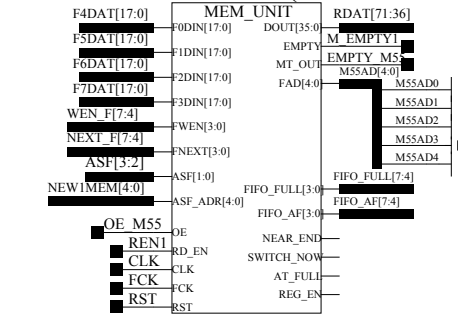
Corner3 FIFO 1 (FAD=1/0001)



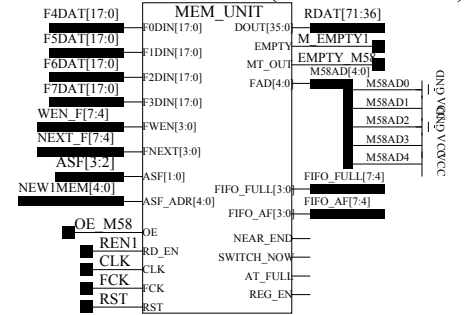
Corner3 FIFO 4 (FAD=1/0100)



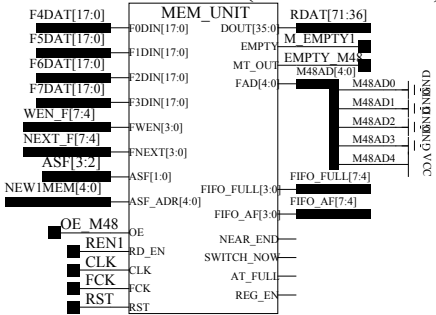
Corner3 FIFO 7 (FAD=1/0111)



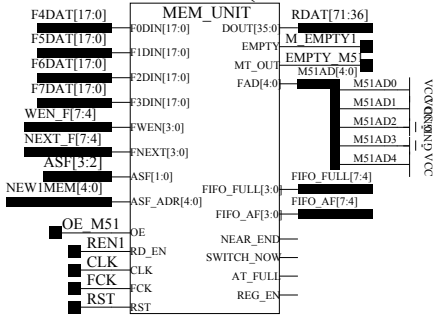
Corner3 FIFO 10 (FAD=1/1010)



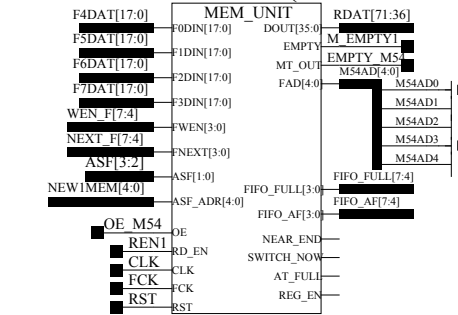
Corner3 FIFO 0 (FAD=1/0000)



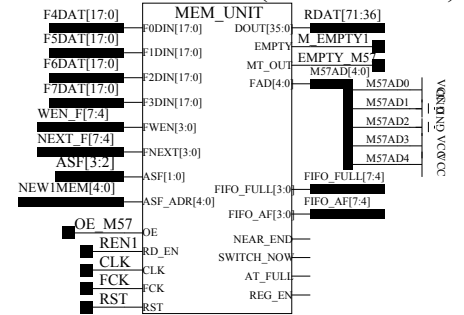
Corner3 FIFO 3 (FAD=1/0011)

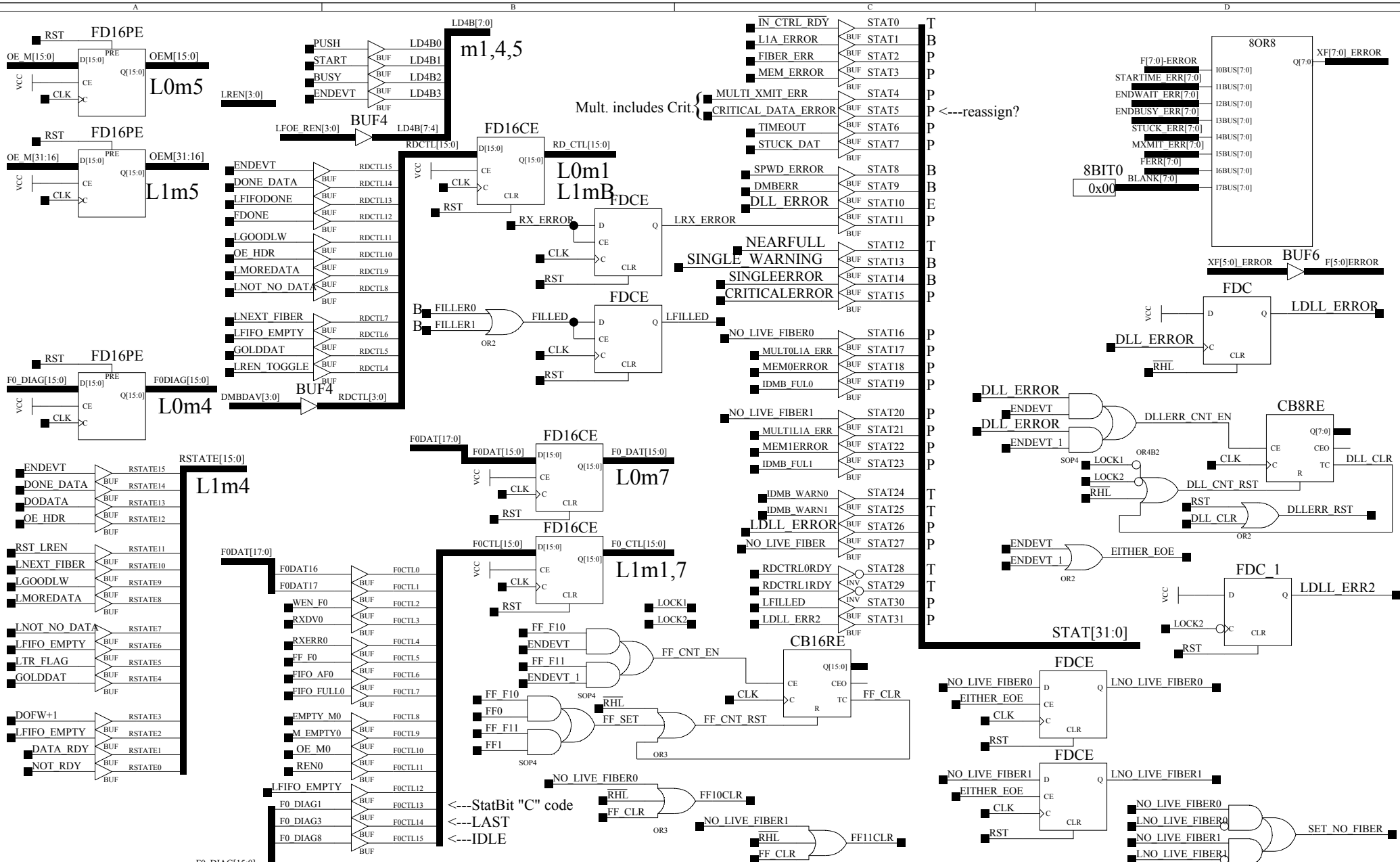


Corner3 FIFO 6 (FAD=1/0110)



Corner3 FIFO 9 (FAD=1/1001)

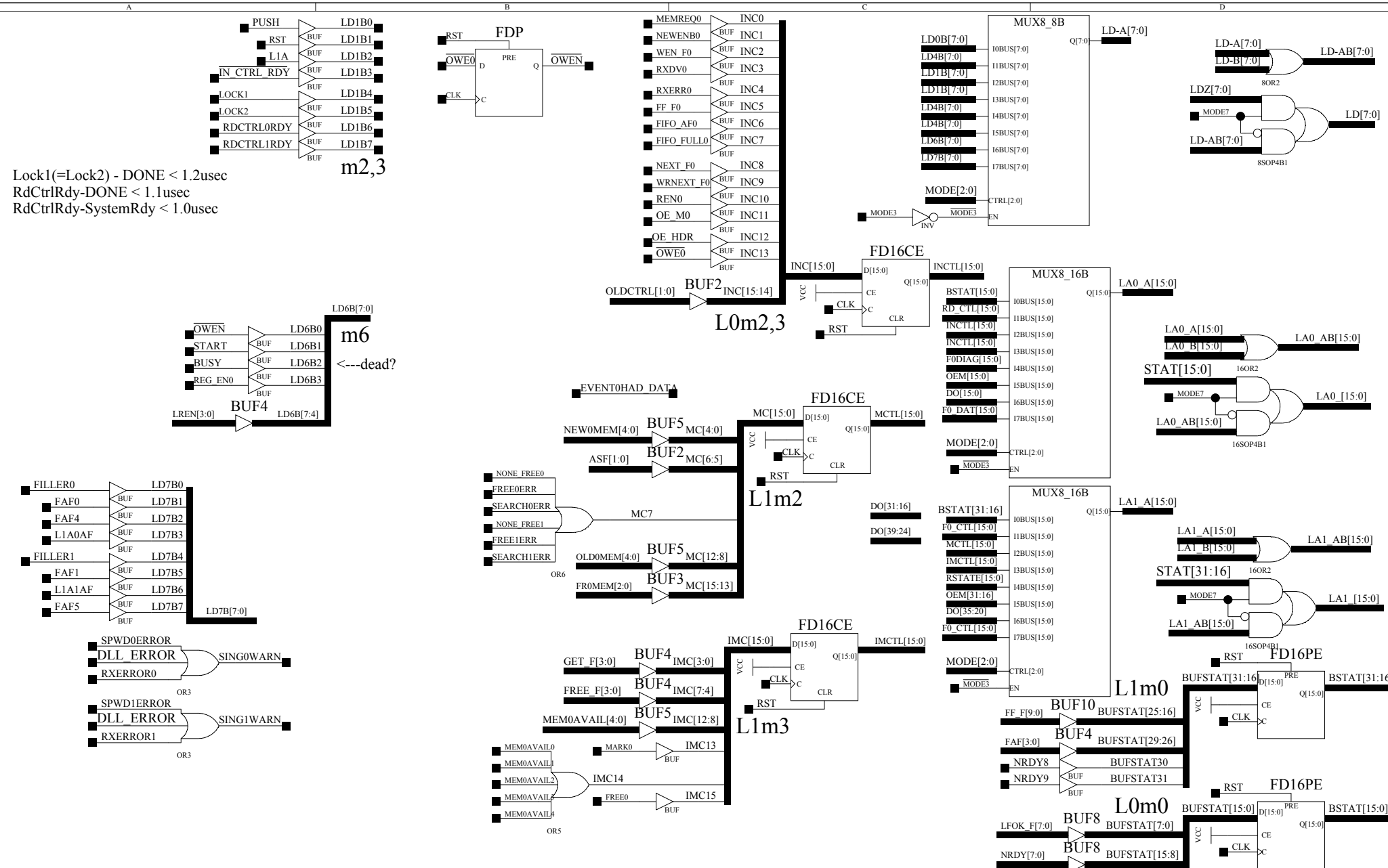




Mult. includes Crit {

----reassign?

<---StatBit "C" code
 <---LAST
 <---IDLE



Lock1(=Lock2) - DONE < 1.2usec
 RdCtrlRdy-DONE < 1.1usec
 RdCtrlRdy-SystemRdy < 1.0usec

m2,3

m6

<---dead?

L0m2,3

L1m2

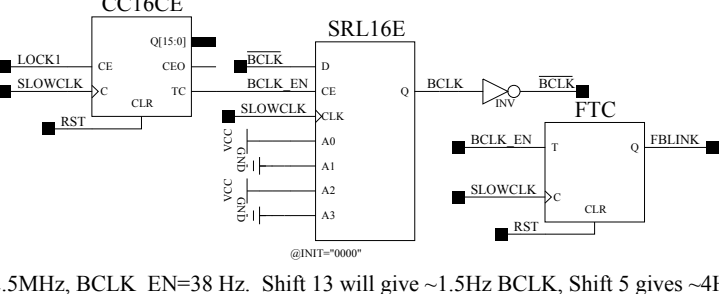
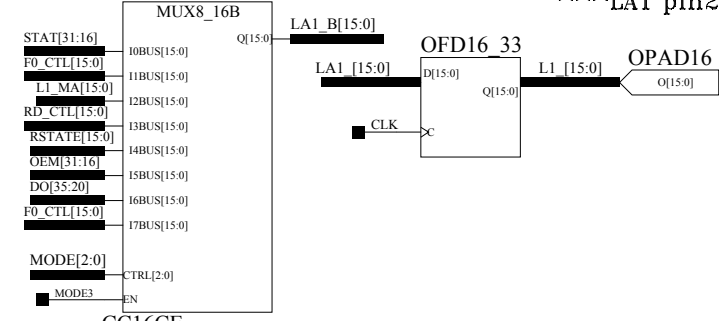
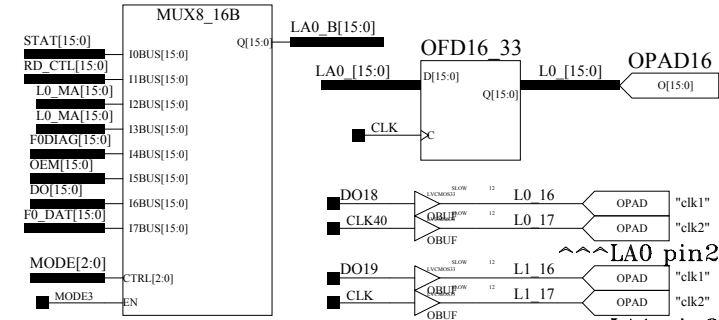
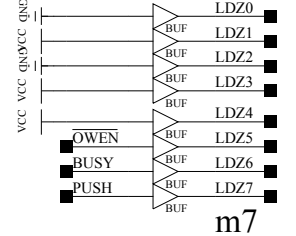
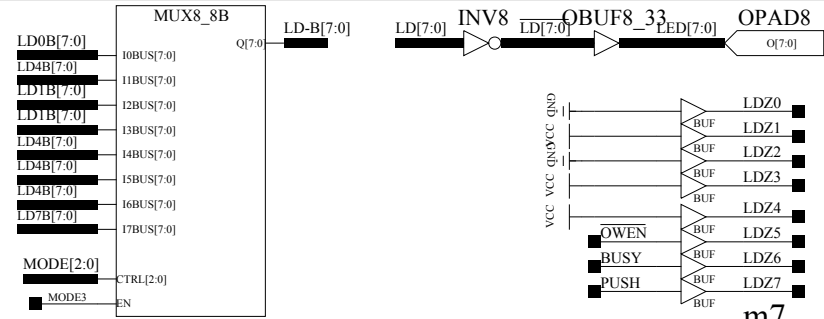
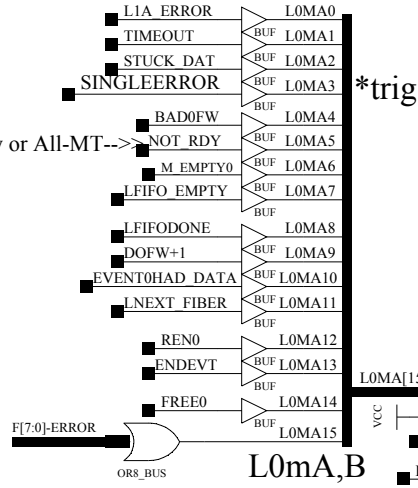
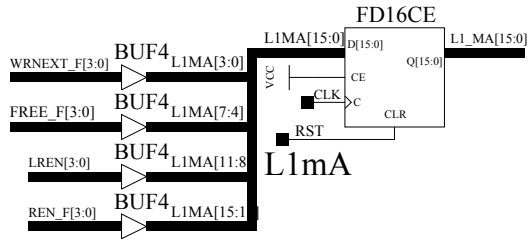
L1m3

L1m0

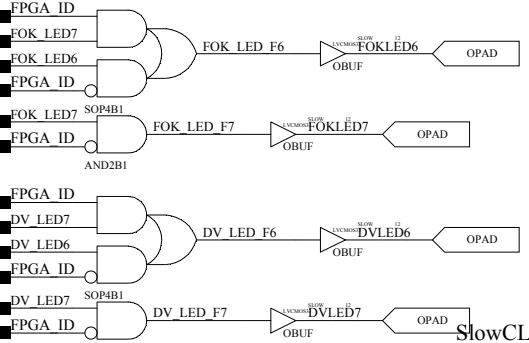
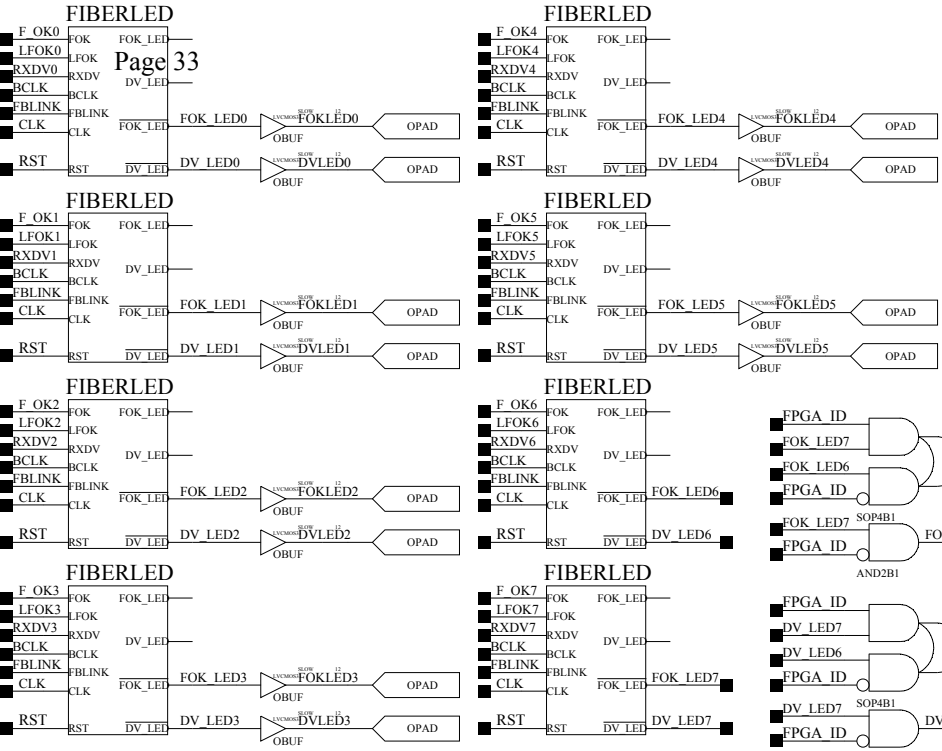
L0m0

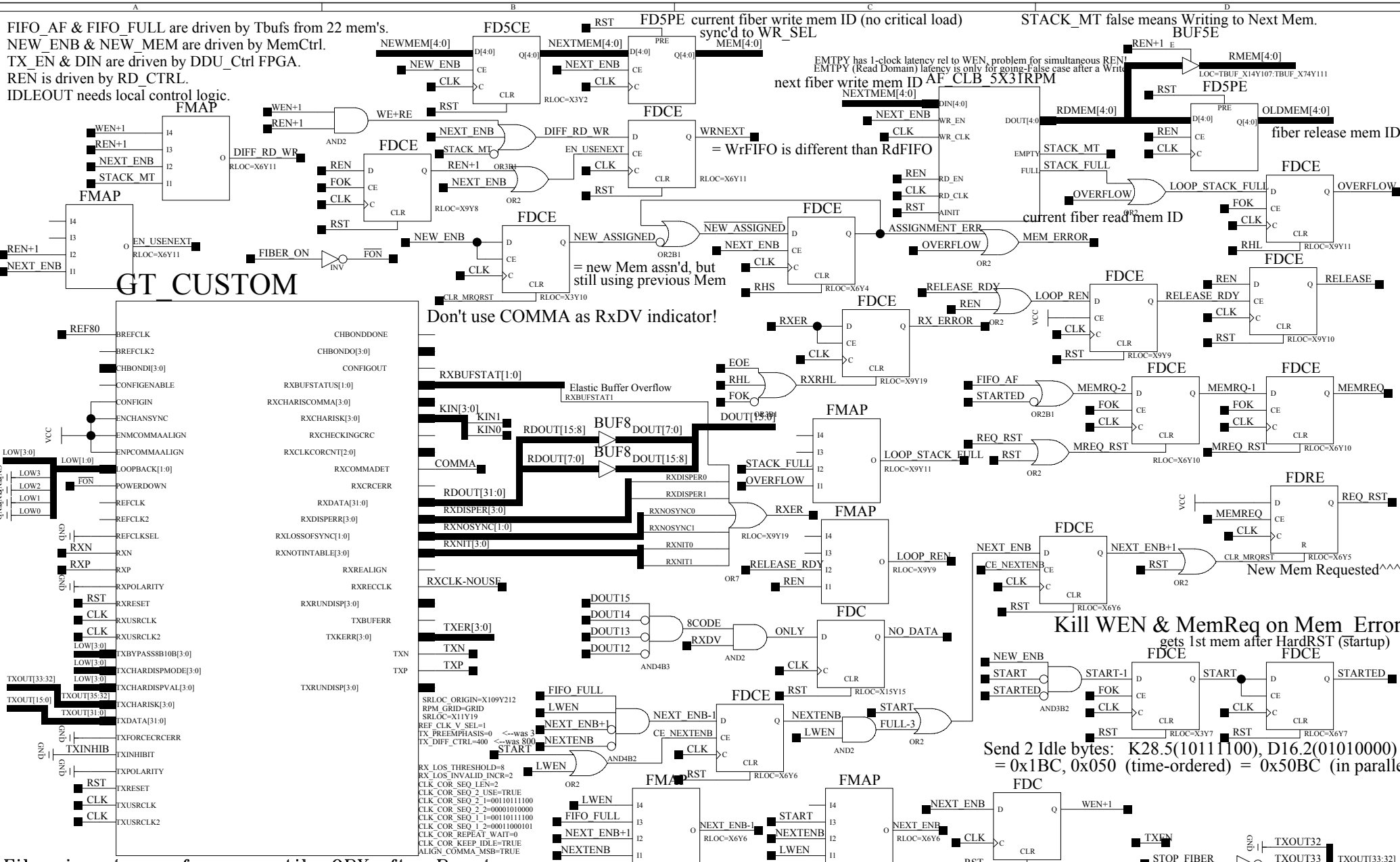
END

NotRdy False means AllRdy or All-MT-->



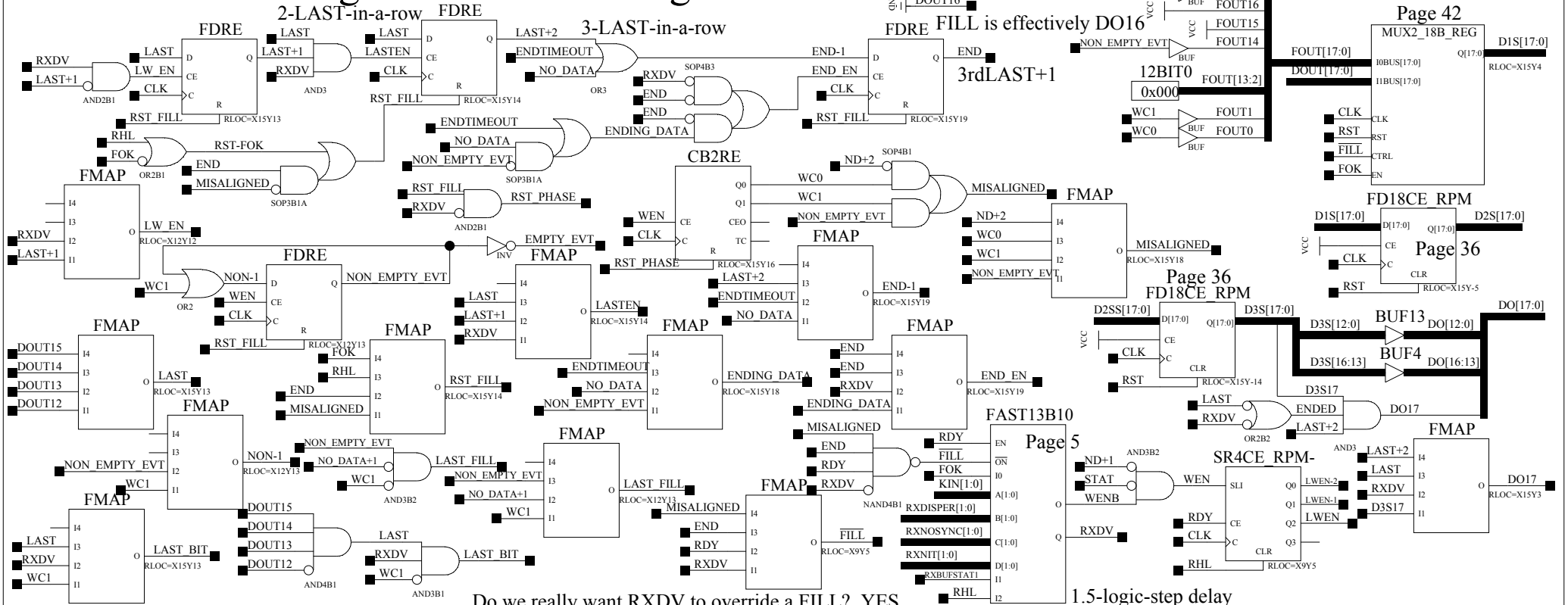
SlowCLK=2.5MHz, BCLK_EN=38 Hz. Shift 13 will give ~1.5Hz BCLK, Shift 5 gives ~4Hz.





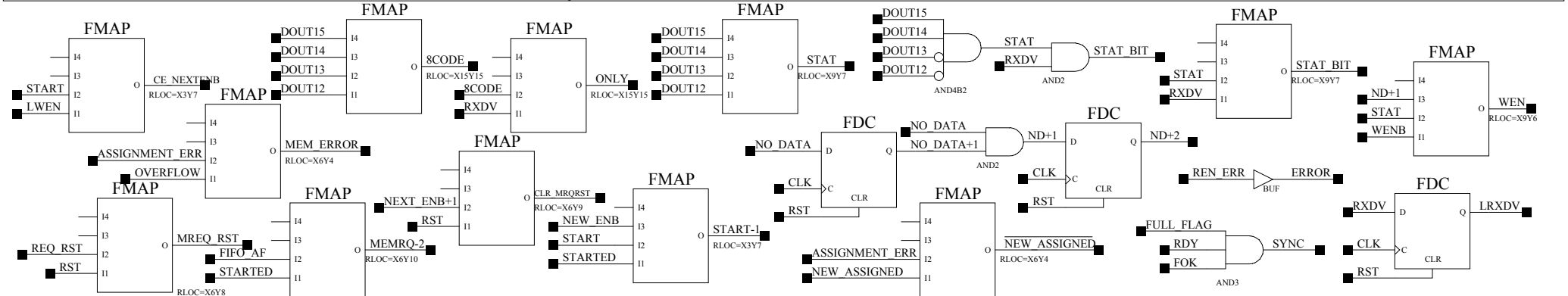
Fiber inputs are frozen until ~9BX after Reset goes away

FILL Logic for 2-4 word alignment

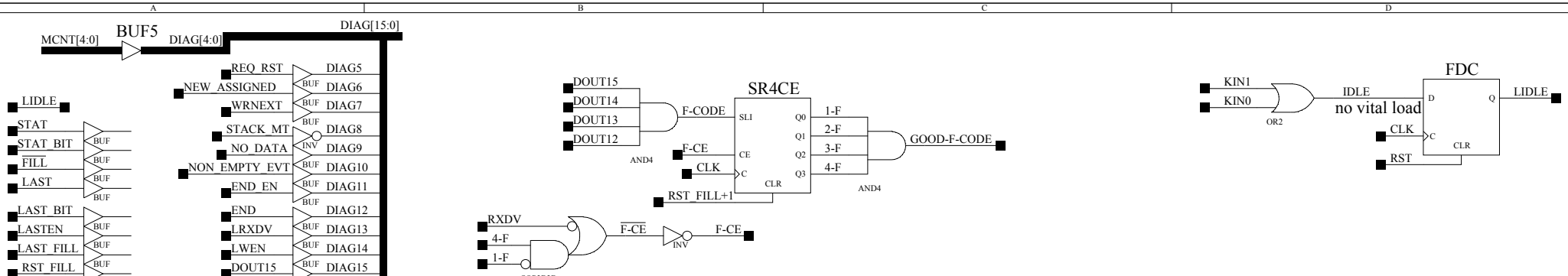


Do we really want RXDV to override a FILL? YES

1.5-logic-step delay



only keep first two 8-codes (L1A number)



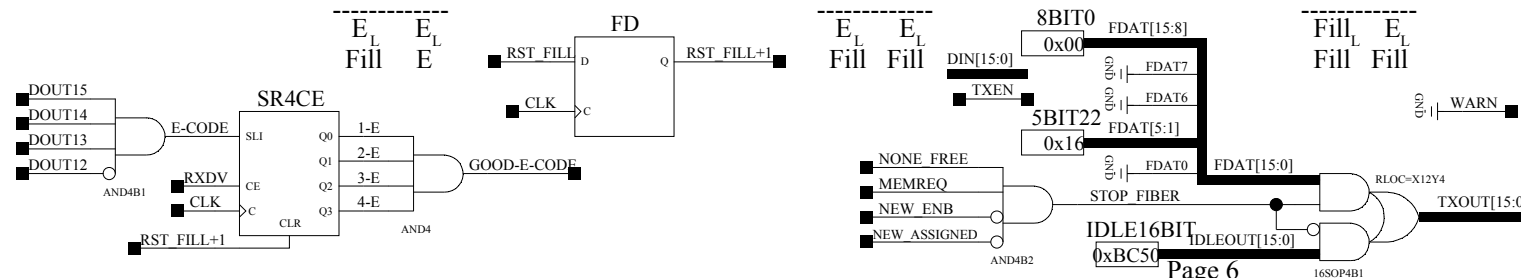
LAST Flag is insensitive to single-bit errors

LAST Flag Logic tables, checks for E-Codes in DMB Data (L means LAST Flag will be set for that word)

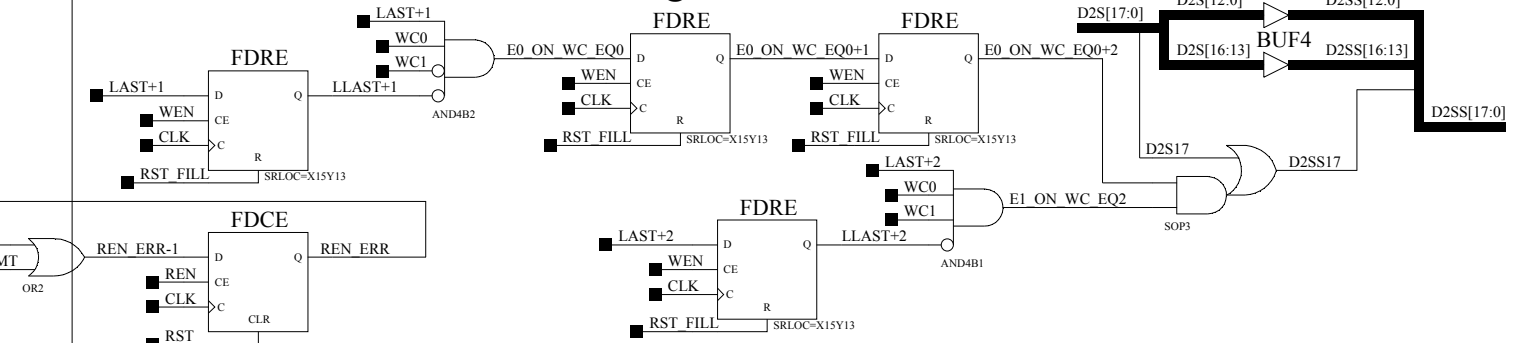
BRAM FIFO Output

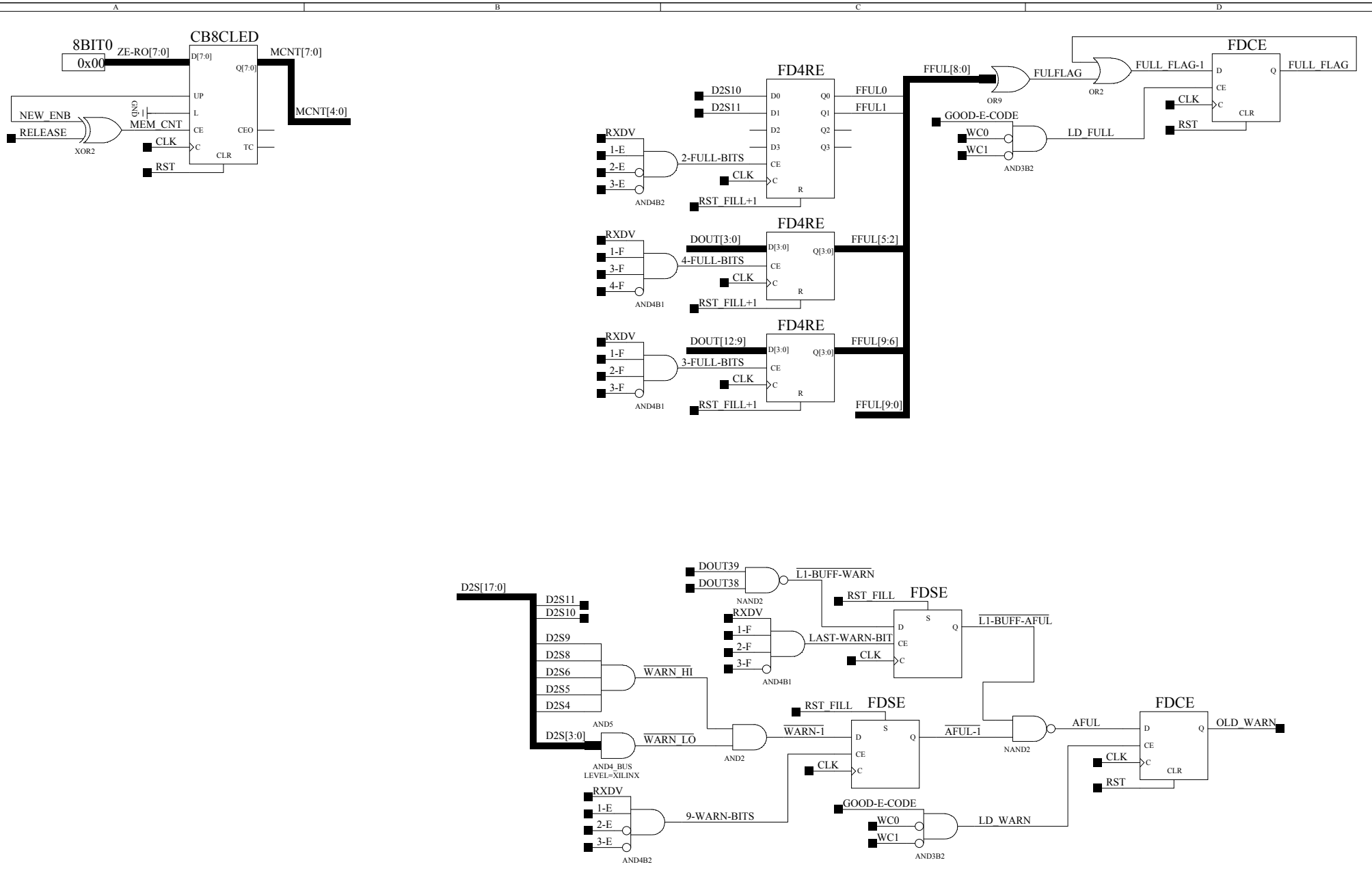
Assume 4 E-Codes at DMB End are sequential with no gaps

Normal event sync:	X	X
	X	X
<hr/>		
	E _L	E
	E	E
<hr/>		
Normal, but lose 1st E-Word: (or lose last E-Word)	X	X
	X	X
<hr/>		
	E _L	E _L
	Fill	E
<hr/>		
Normal, but lose 2nd E-Word: (or lose 3rd E-Word)	X	X
	X	X
<hr/>		
	E _L	E
	Fill	E
<hr/>		
Normal, but BAD 1st E-Code:	X	X
	X	X
<hr/>		
	E _L	X
	E	E
<hr/>		
Normal, but BAD 2nd E-Code:	X	X
	X	X
<hr/>		
	X _L	E
	E	E

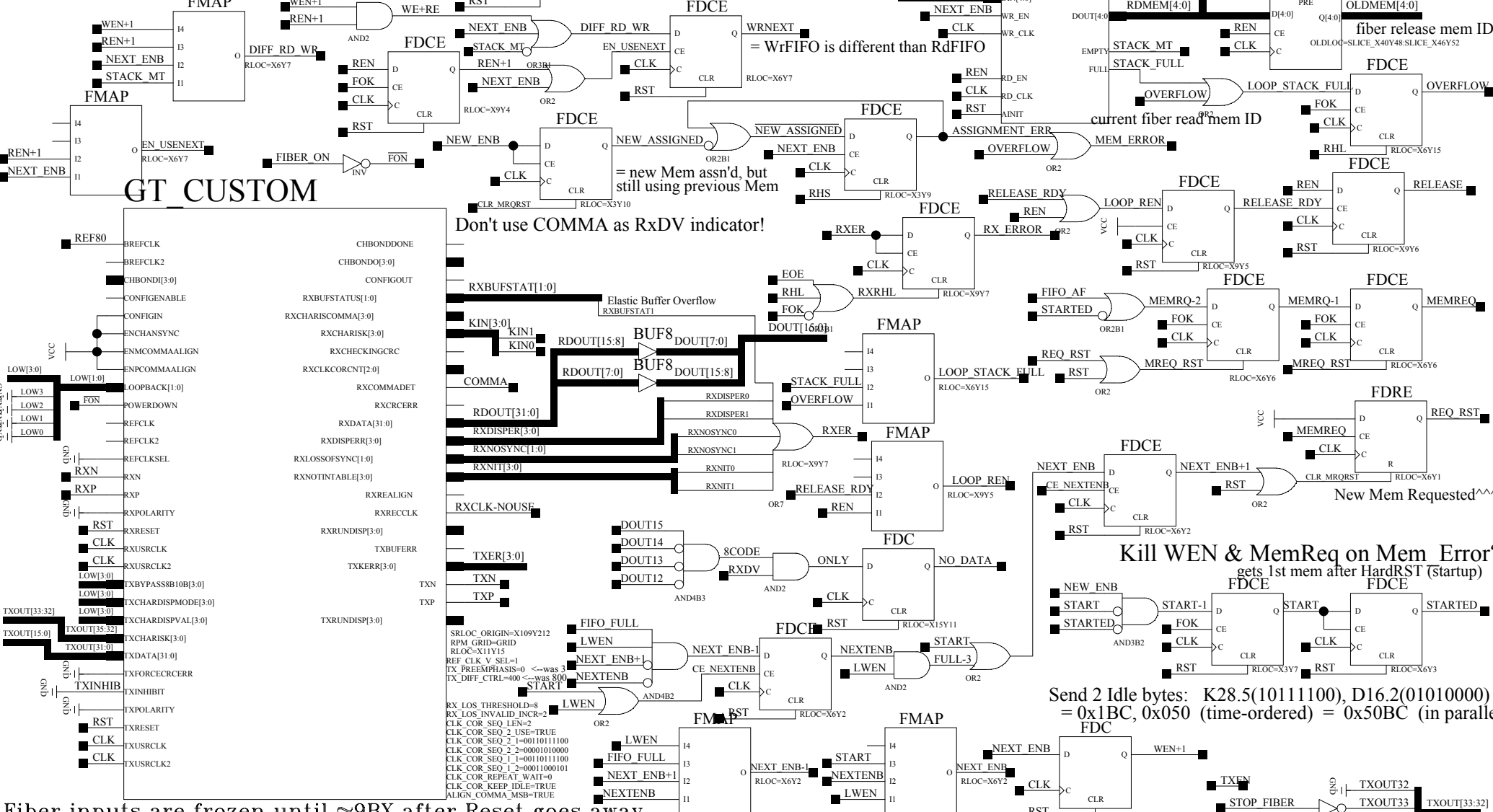


Set LAST Flag for Bad 2nd E-Code case



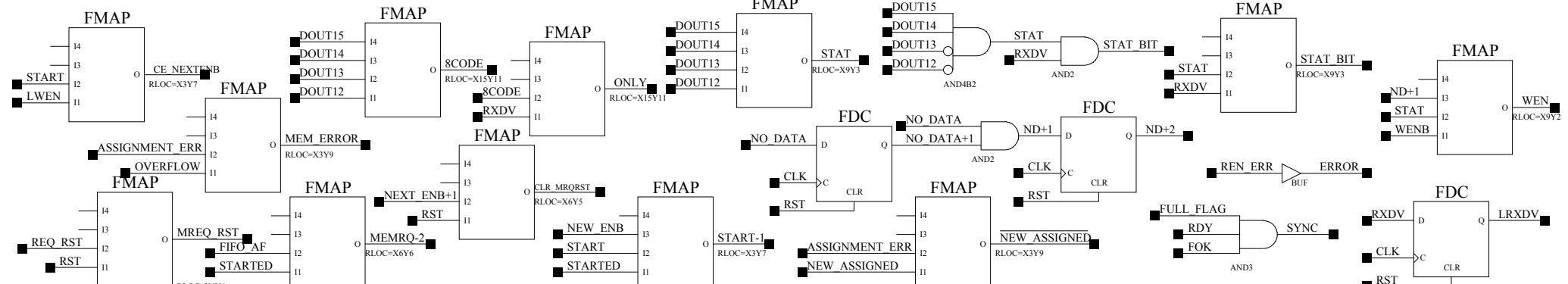
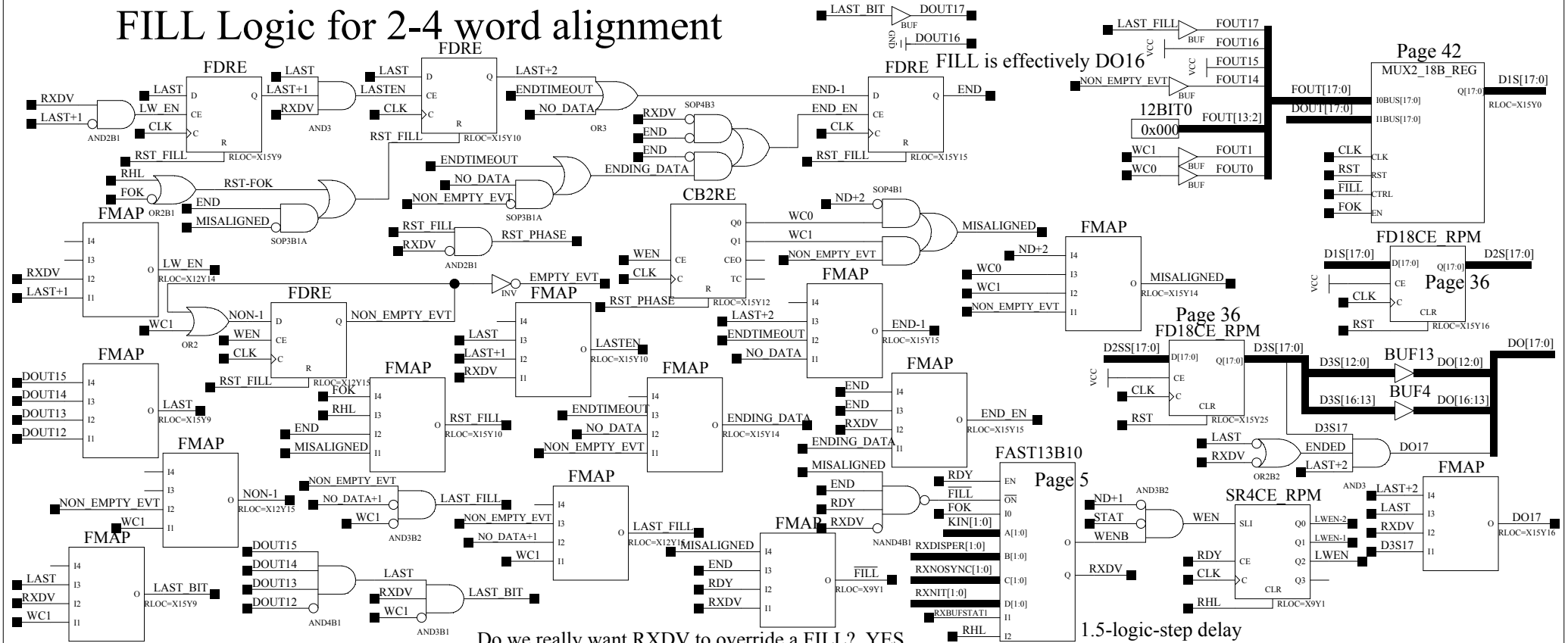


FIFO_AF & FIFO_FULL are driven by Tbufs from 22 mem's.
 NEW_ENB & NEW_MEM are driven by MemCtrl.
 TX_EN & DIN are driven by DDU_Ctrl FPGA.
 REN is driven by RD_CTRL.
 IDLEOUT needs local control logic.



Fiber inputs are frozen until ~9BX after Reset goes away

FILL Logic for 2-4 word alignment



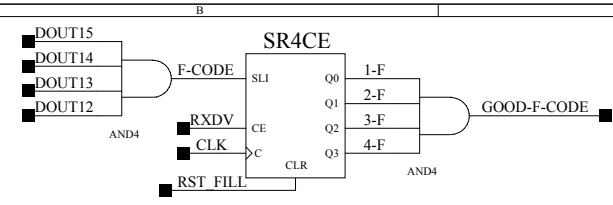
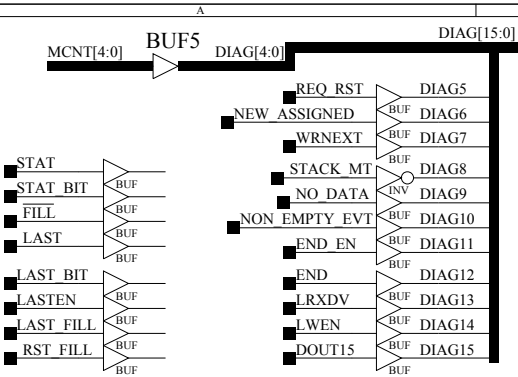
THE OHIO STATE UNIVERSITY
 PHYSICS DEPARTMENT ELECTRONICS LAB
 174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE **Input Unit**
 DDU Input Controller Logic
 CMS CSC Electronics

BY **JRG** PARENT PAGE **2D**
 DATE **4-23-2009_16:58**

PROJECT **D785D**
 FILE **IN UNIT B . 2** PAGE **4A**

only keep first two 8-codes (L1A number)



LAST Flag is insensitive to single-bit errors

LAST Flag Logic tables, checks for E-Codes in DMB Data (E_L means LAST Flag will be set for that word)
 BRAM FIFO Output

Assume 4 E-Codes at DMB End are sequential with no gaps

Normal event sync:	X	X
	X	X

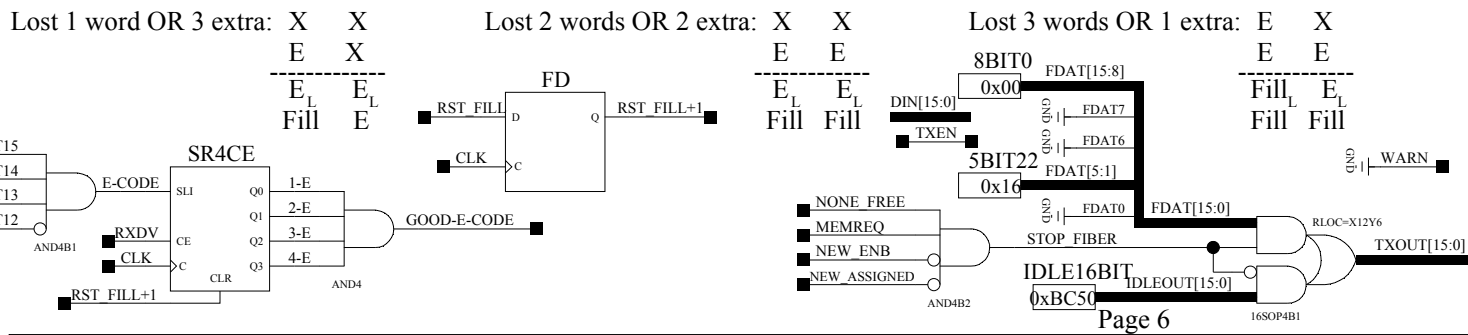
	E _L	E
	E	E
Normal, but lose 1st E-Word: (or lose last E-Word)	X	X
	X	X

	E _L	E _L
	Fill	E
Normal, but lose 2nd E-Word: (or lose 3rd E-Word)	X	X
	X	X

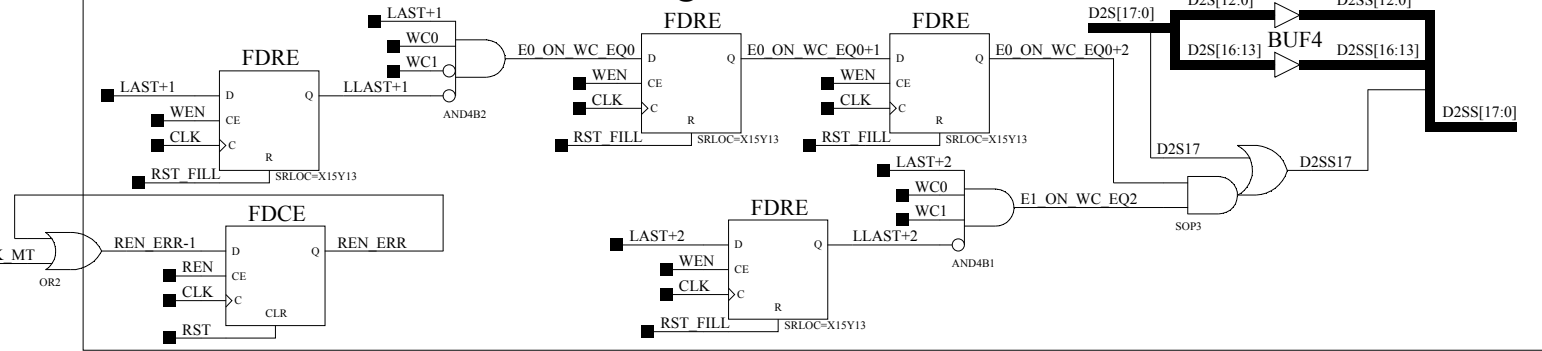
	E _L	E
	Fill	E
Normal, but BAD 1st E-Code:	X	X
	X	X

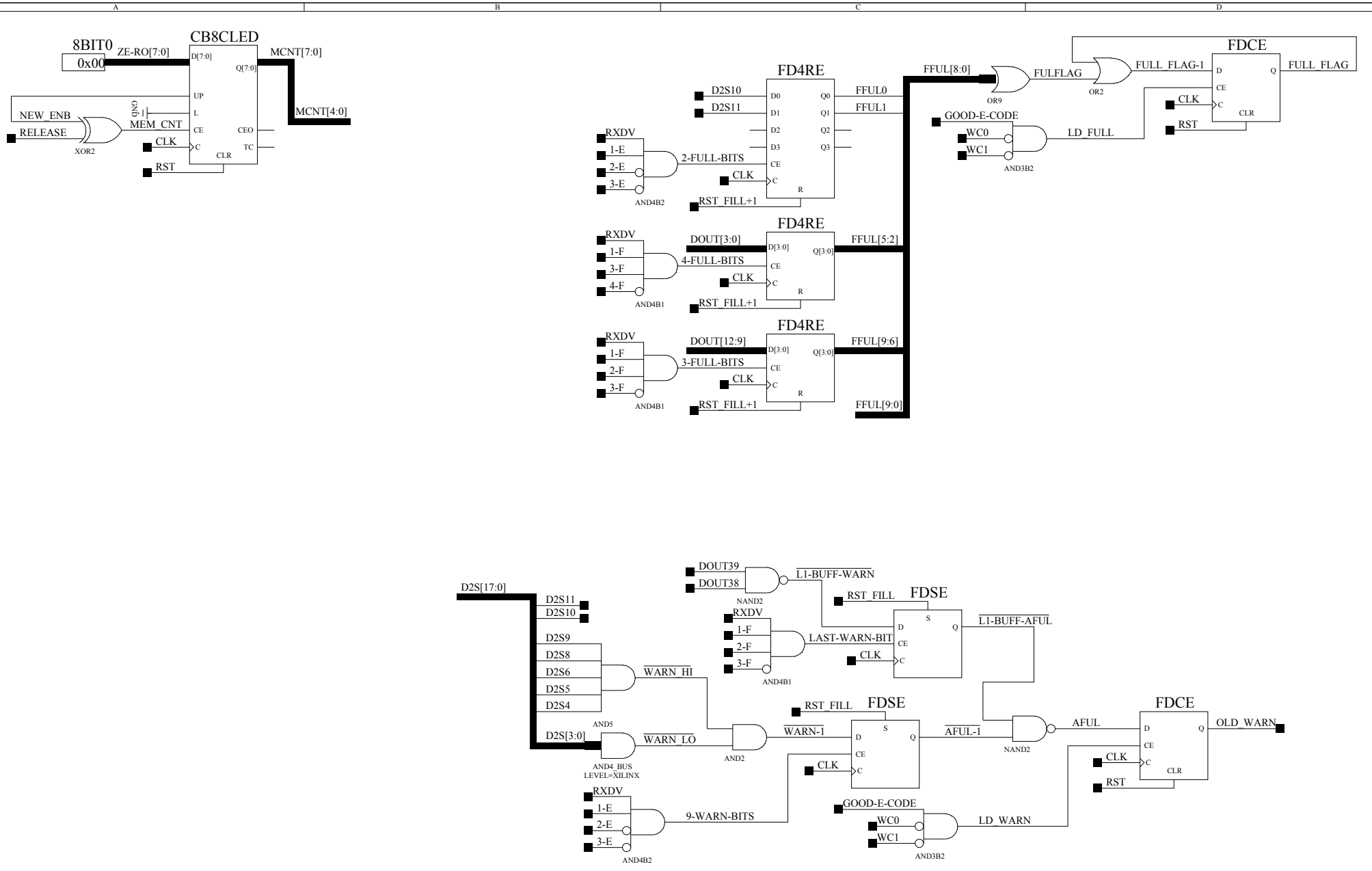
	E _L	X
	E	E
Normal, but BAD 2nd E-Code:	X	X
	X	X

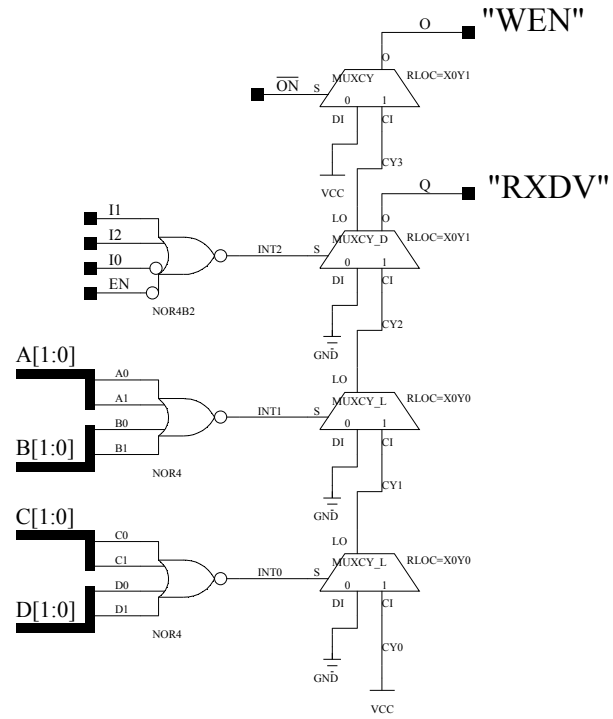
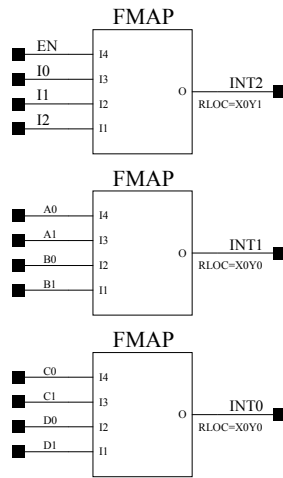
	X _L	E
	E	E
BAD 3rd or 4th E-Code is no problem		



Set LAST Flag for Bad 2nd E-Code case





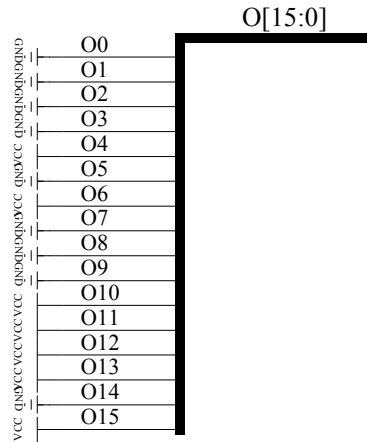


JRG

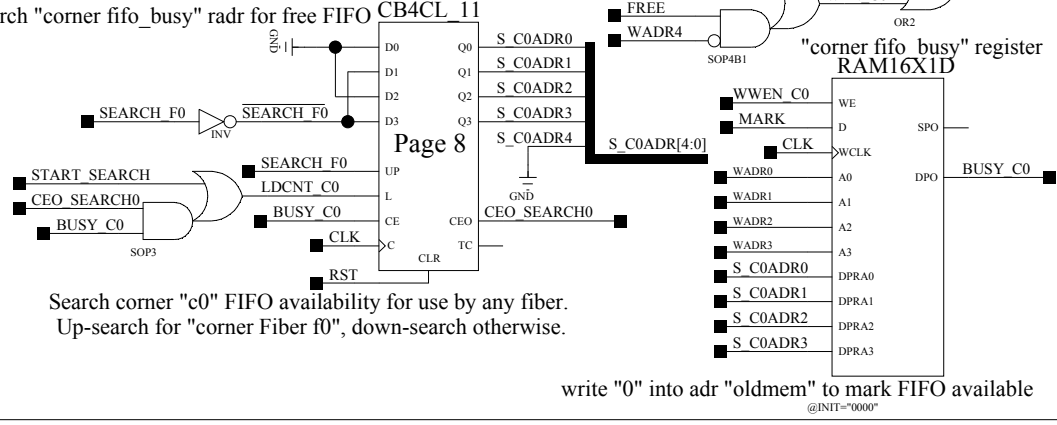
Title:	FAST13B10	
Comments:	Custom Logic for DDU similar to: AND12B10 with an OR2 (allows ON to override)	
Date:	19th December 2003	Ver: 1
Sheet Size:	B	Rev: A

Send 2 Idle bytes:

$K28.5(10111100)+D16.2(01010000)$
= 0x1BC + 0x050 (time-ordered)
= 0xBC50 (in parallel)

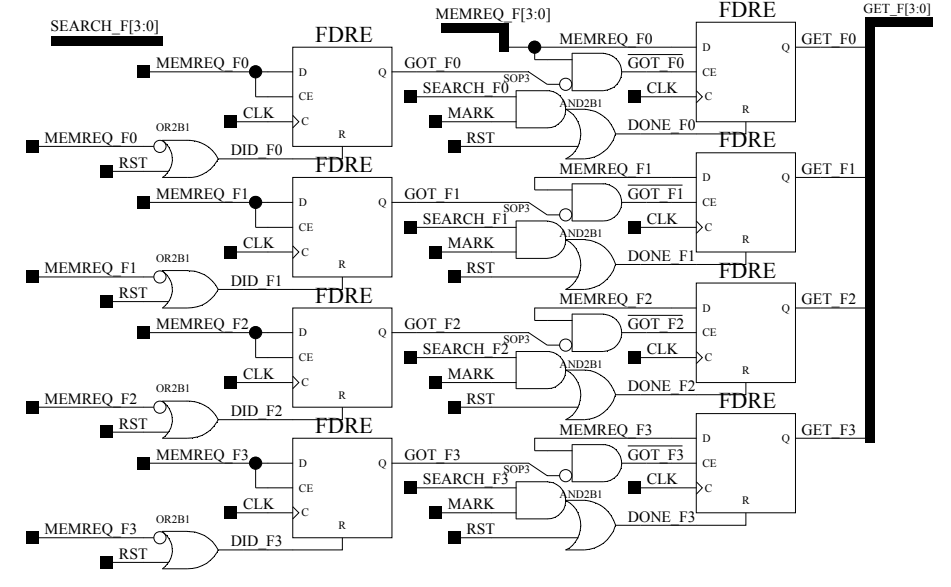


Corner 0 FIFO usage

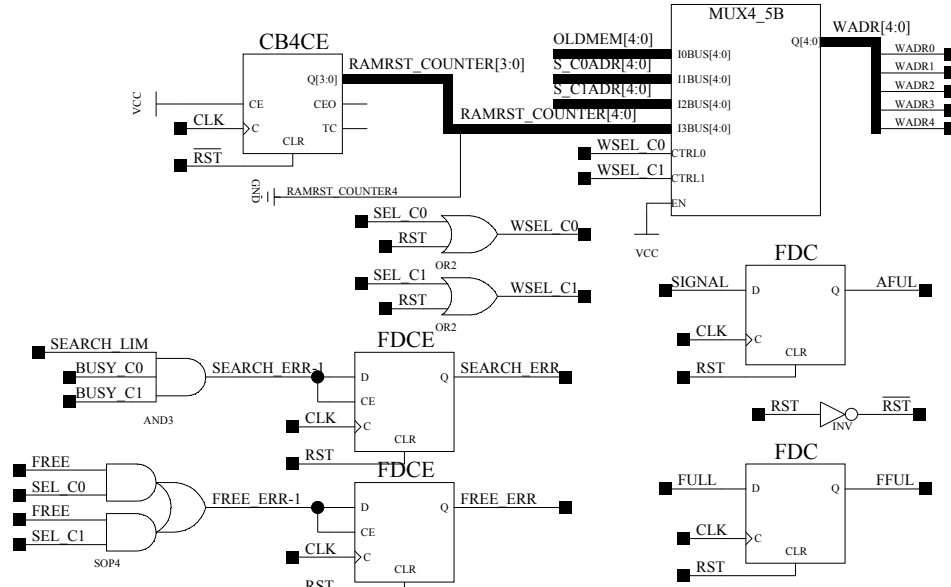
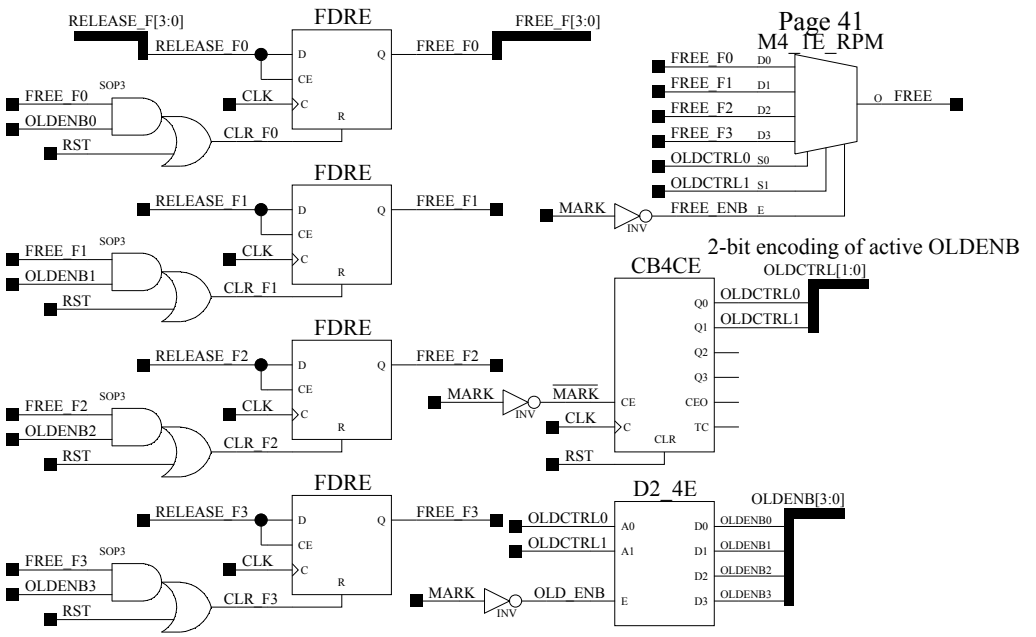


Search corner "c0" FIFO availability for use by any fiber.
Up-search for "corner Fiber f0", down-search otherwise.

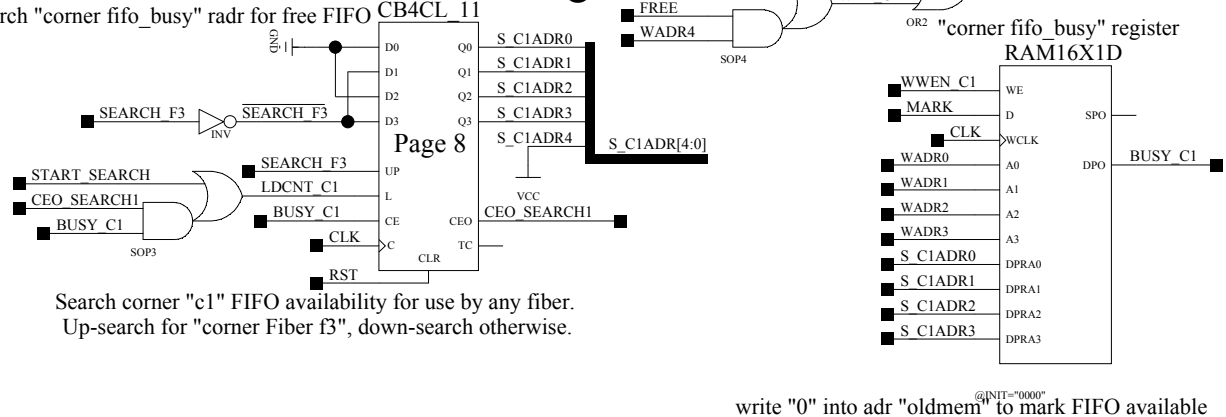
Which Fibers need a new FIFO?



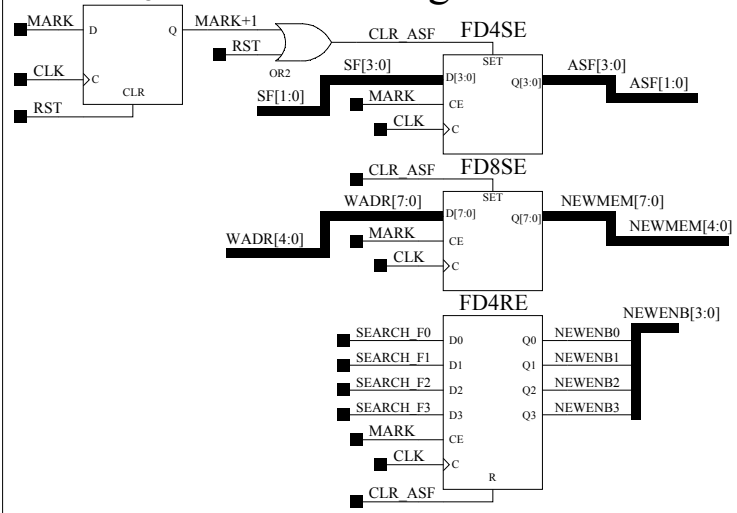
FIFO Release Control



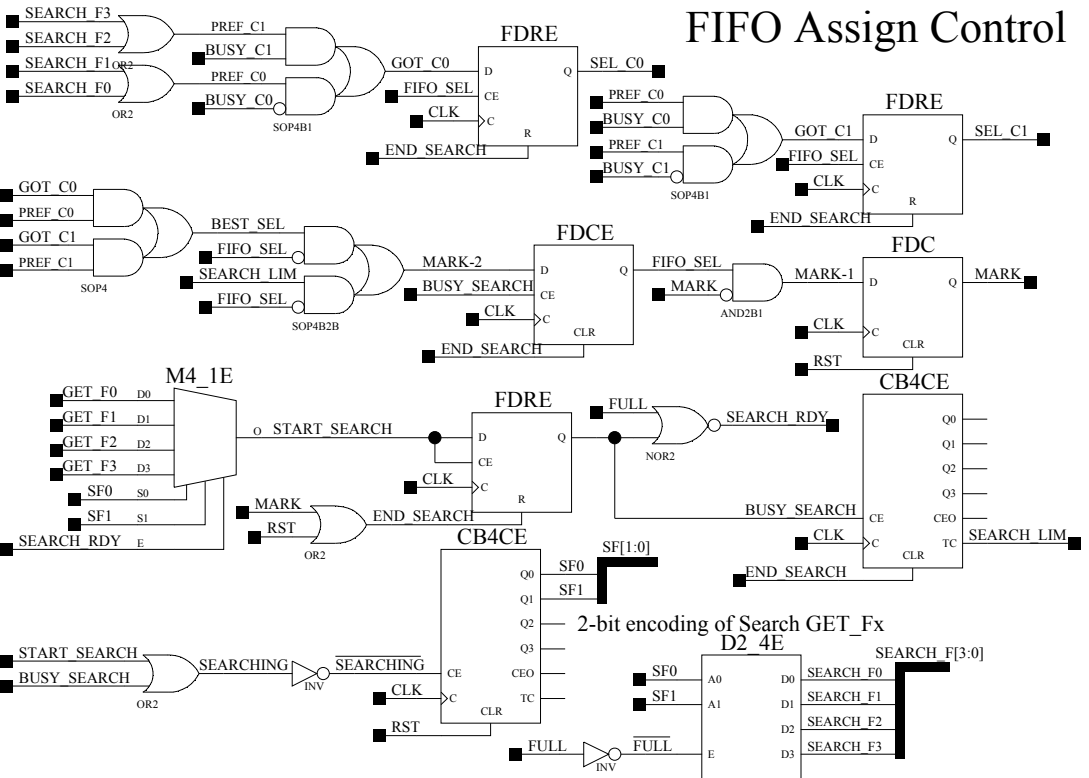
Corner 1 FIFO usage



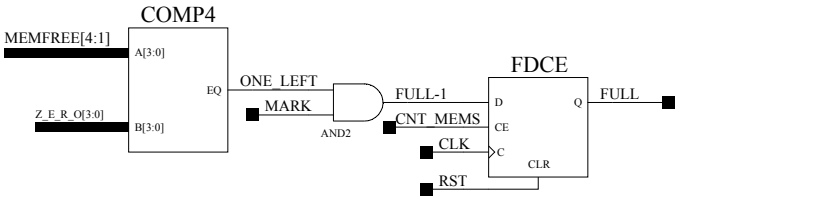
Assign Fiber to FIFO & Assign FIFO to Fiber



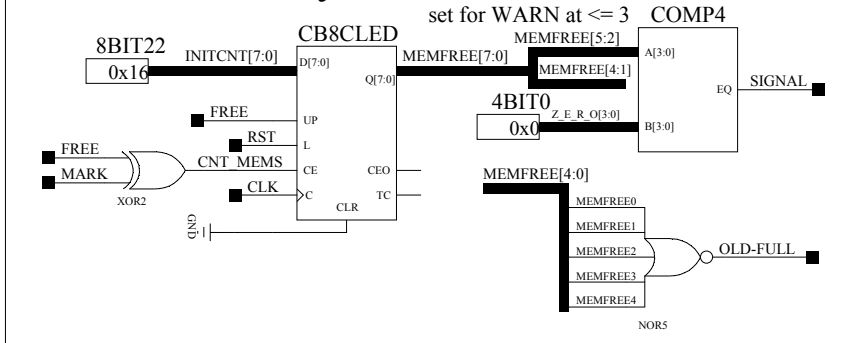
FIFO Assign Control

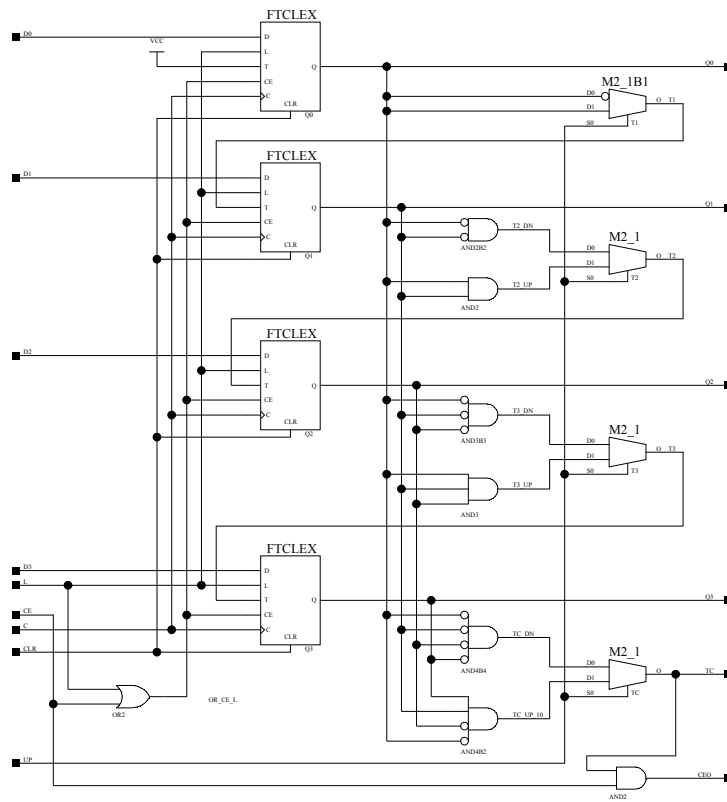


PREF C[1:0]
 BUSY C[1:0]
 GOT C[1:0]



How many of 22 FIFOs are free?





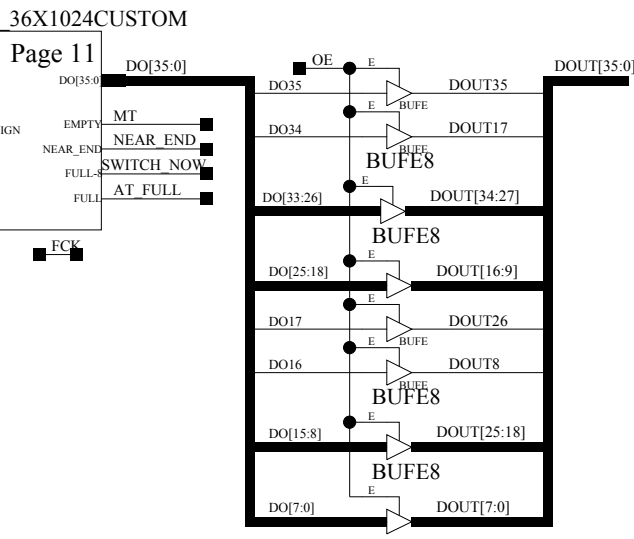
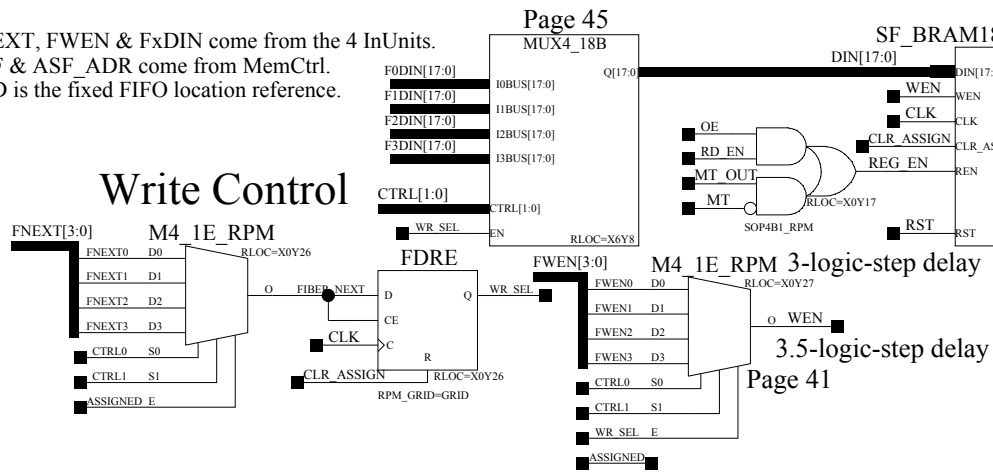
Title: VIRTEx Family CHOKLED Macro
 Comments: 4-Bit Latchable Counter (Design)

JRG

Date: 21st August 2003
 Sheet Size: C

Ver: 1
 Rev: A

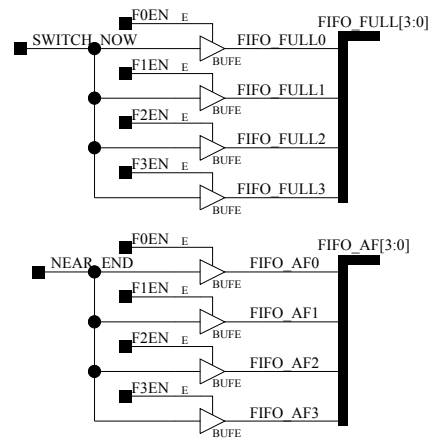
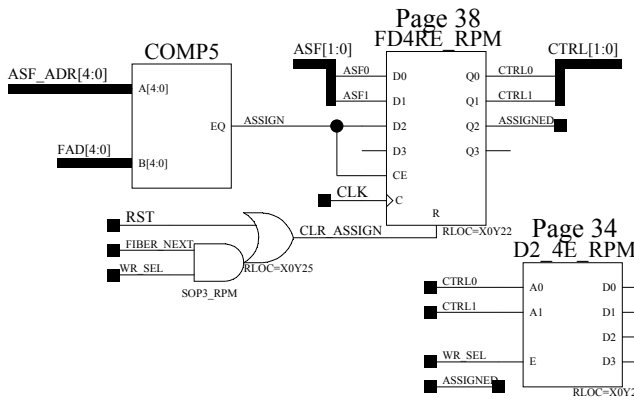
FNEXT, FWEN & FxDIN come from the 4 InUnits.
 ASF & ASF_ADR come from MemCtrl.
 FAD is the fixed FIFO location reference.



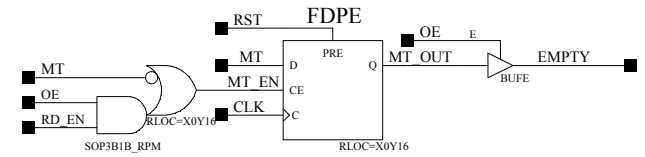
MemIn-MemOut Mapping:

DO35	Dout35
DO34	Dout17
DO33-26	Dout34-27
DO25-18	Dout16-9
DO17	Dout26
DO16	Dout8
DO15-8	Dout25-18
Din7-0	Dout7-0

MT == less than 36-bits of data are available



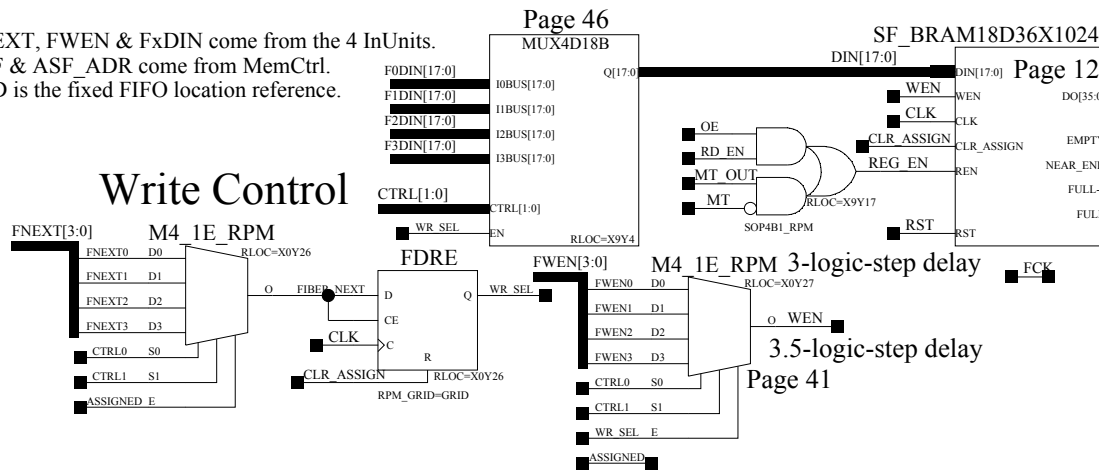
First Word Fall Through logic:



Not Used: REN = OE * RD_EN

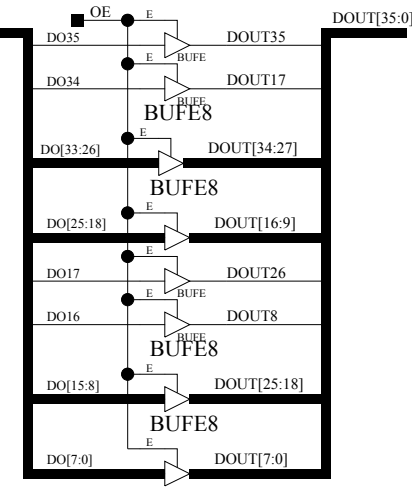
FNEXT, FWEN & FxDIN come from the 4 InUnits.
 ASF & ASF_ADR come from MemCtrl.
 FAD is the fixed FIFO location reference.

Write Control

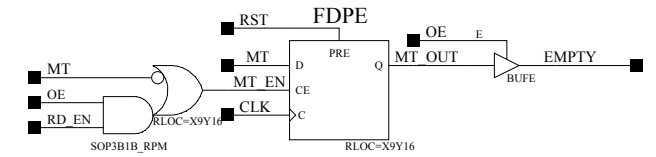


MemIn-MemOut Mapping:

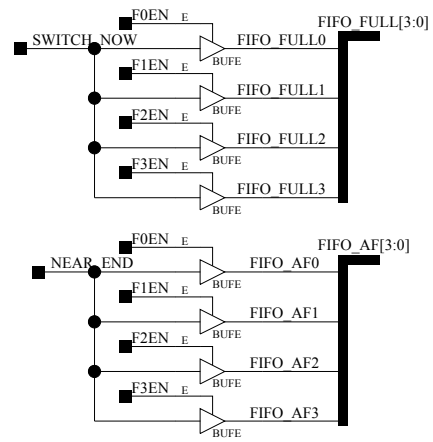
DO35	Dout35
DO34	Dout17
DO33-26	Dout34-27
DO25-18	Dout16-9
DO17	Dout26
DO16	Dout8
DO15-8	Dout25-18
Din7-0	Dout7-0



First Word Fall Through logic:

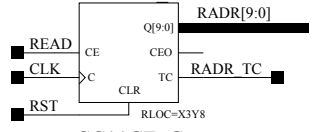


Not Used: $REN = OE * RD_EN$

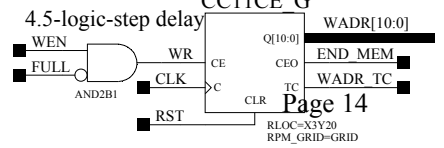


sfifo18_36x1024

Page 13
CC10CE G

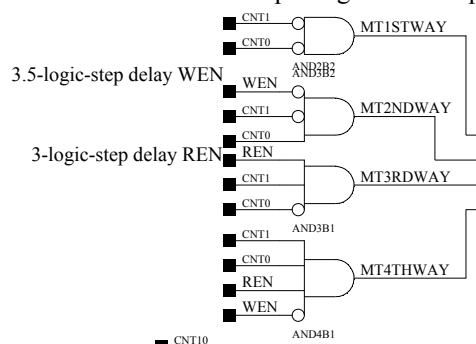


CC11CE G



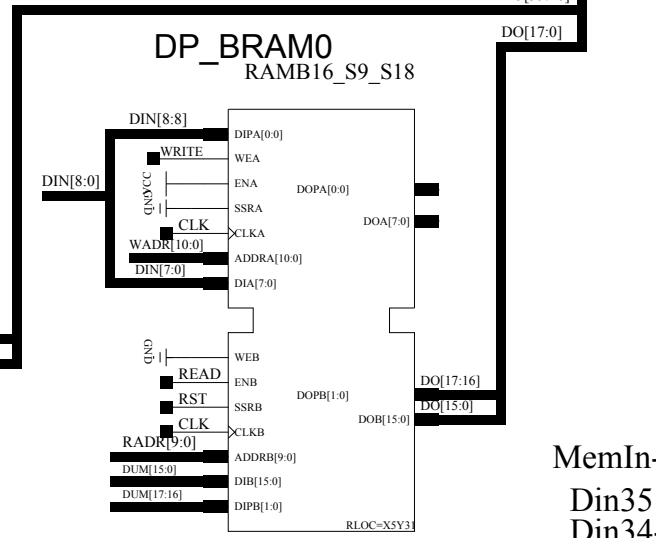
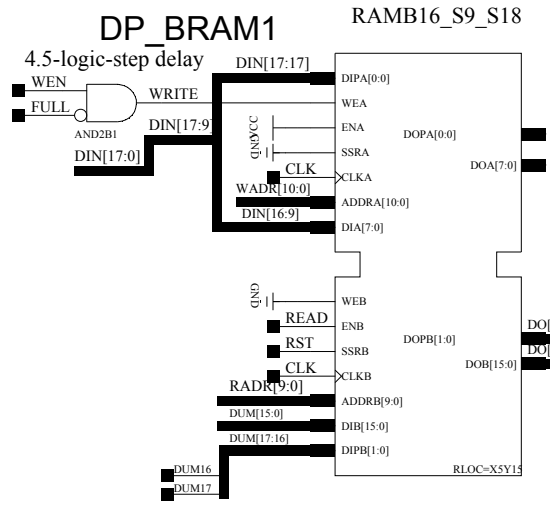
5.5-logic-step delay...

but 4 input logic should optimize to 1 LUT=4.5 step delay.



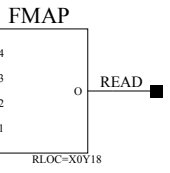
^^^Nearly Empty gives CE for Empty Reg.

EMPTY == less than 36-bits of data are available



MemIn-MemOut Mapping:

Din35	Din35
Din34-27	Din33-26
Din26	Din17
Din25-18	15-8
Din17	Din34
Din16-9	Din25-18
Din8	Din16
Din7-0	Din7-0

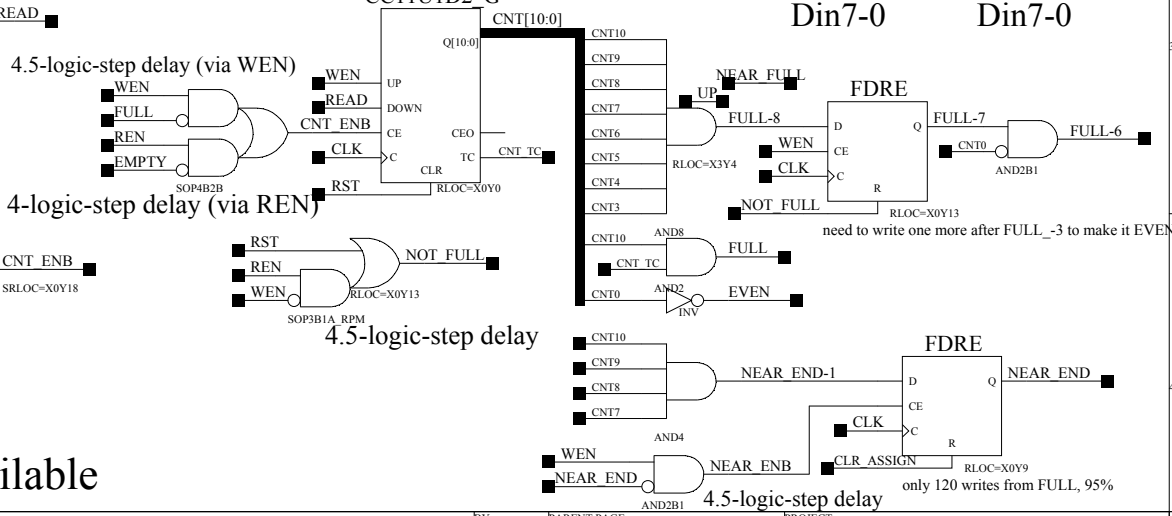


Page 15
CC11U1D2 G

4.5-logic-step delay (via WEN)

4-logic-step delay (via REN)

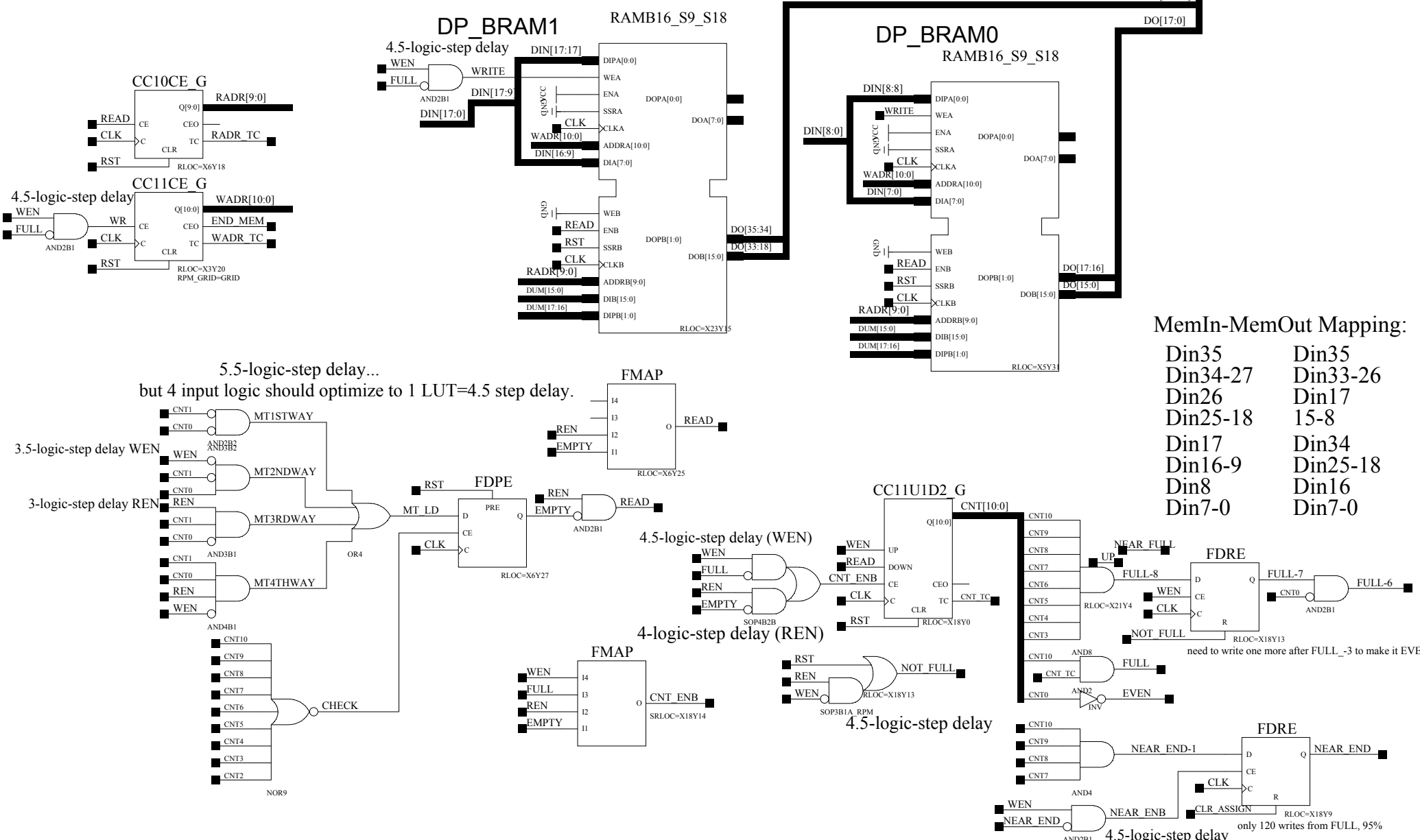
4.5-logic-step delay



need to write one more after FULL_-3 to make it EVEN

only 120 writes from FULL, 95%

sfifo18_36x1024_diagonal



MemIn-MemOut Mapping:

Din35	Din35
Din34-27	Din33-26
Din26	Din17
Din25-18	15-8
Din17	Din34
Din16-9	Din25-18
Din8	Din16
Din7-0	Din7-0

5.5-logic-step delay...
but 4 input logic should optimize to 1 LUT=4.5 step delay.

4.5-logic-step delay (WEN)

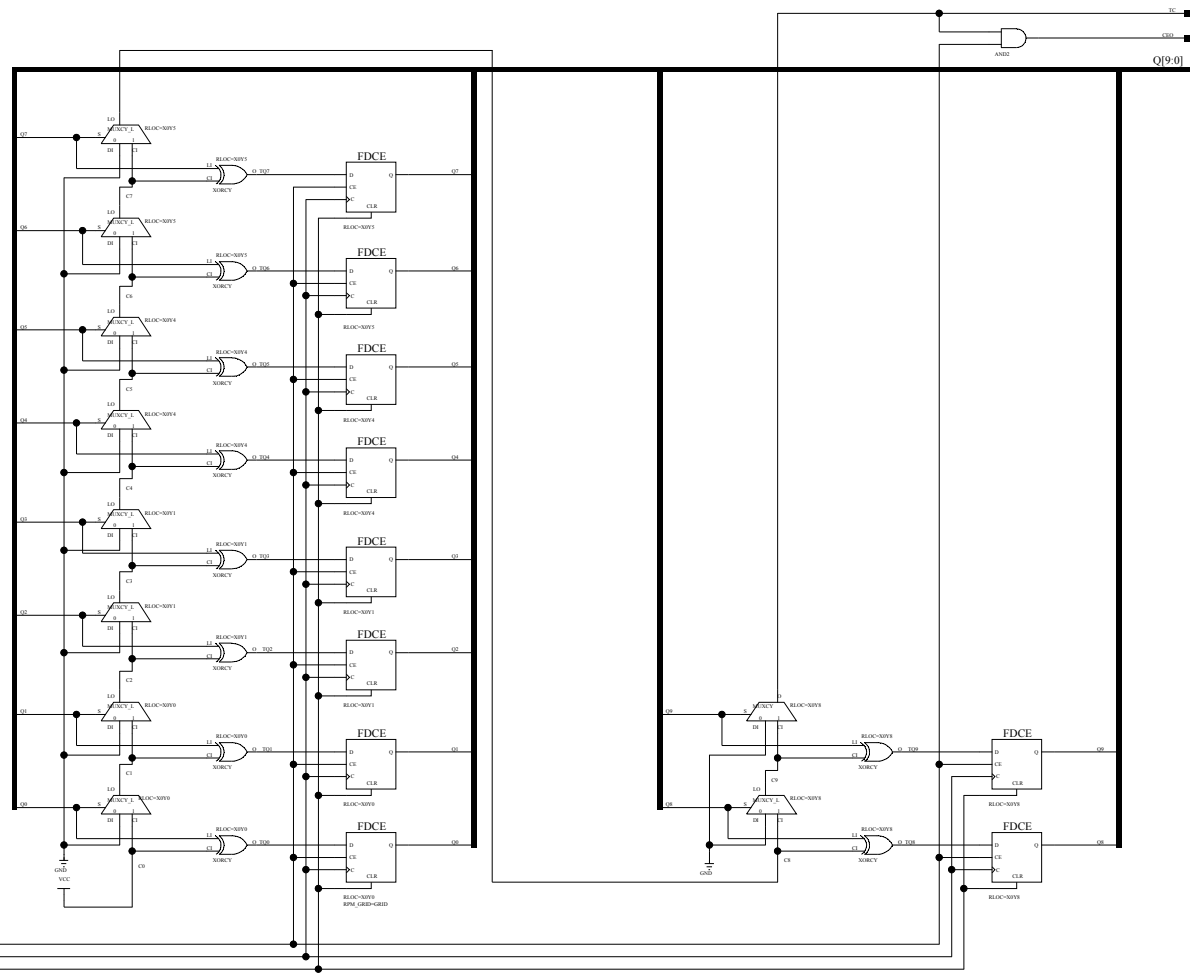
4-logic-step delay (REN)

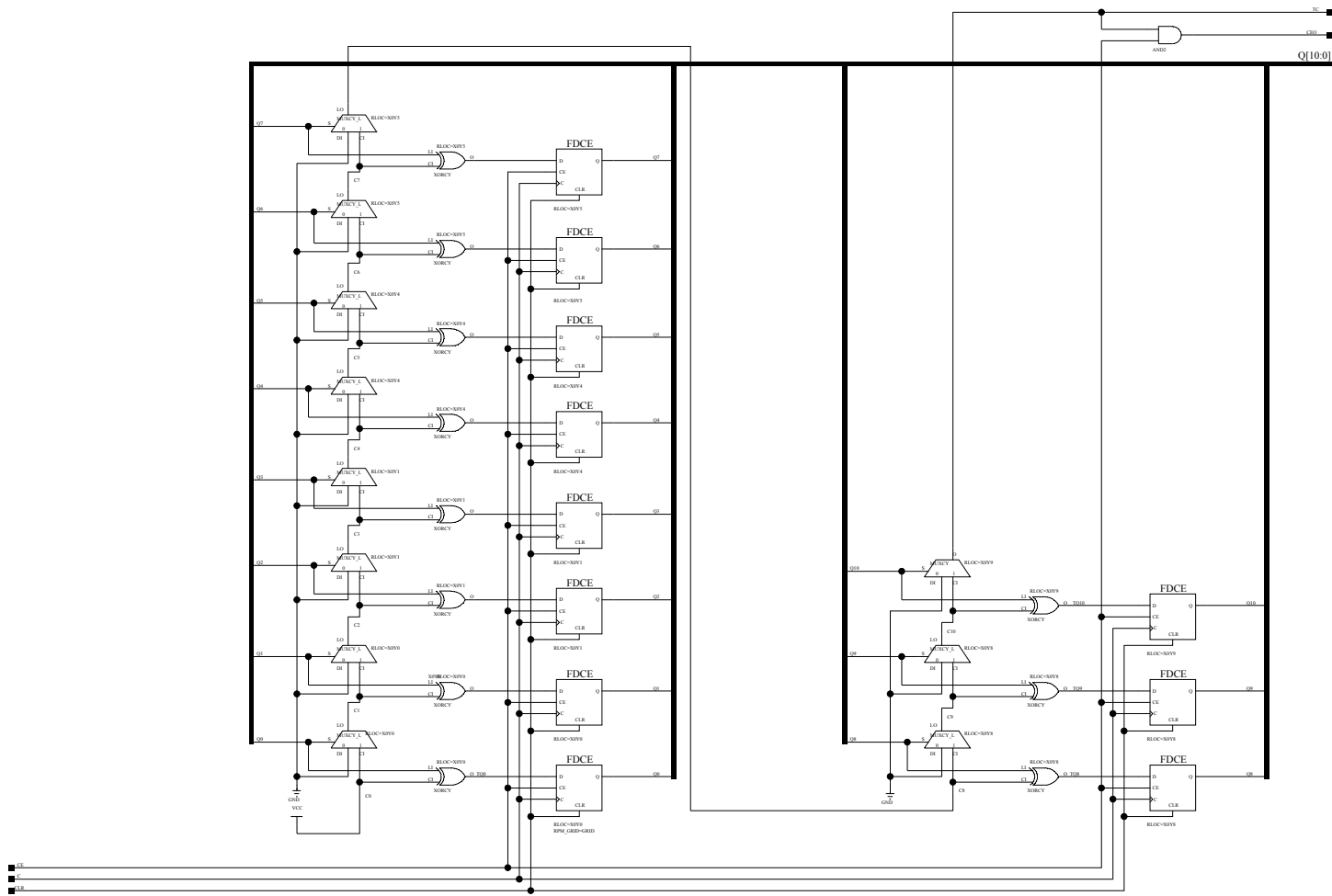
4.5-logic-step delay

4.5-logic-step delay

need to write one more after FULL_-3 to make it EVEN

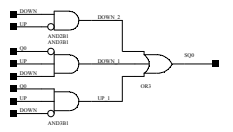
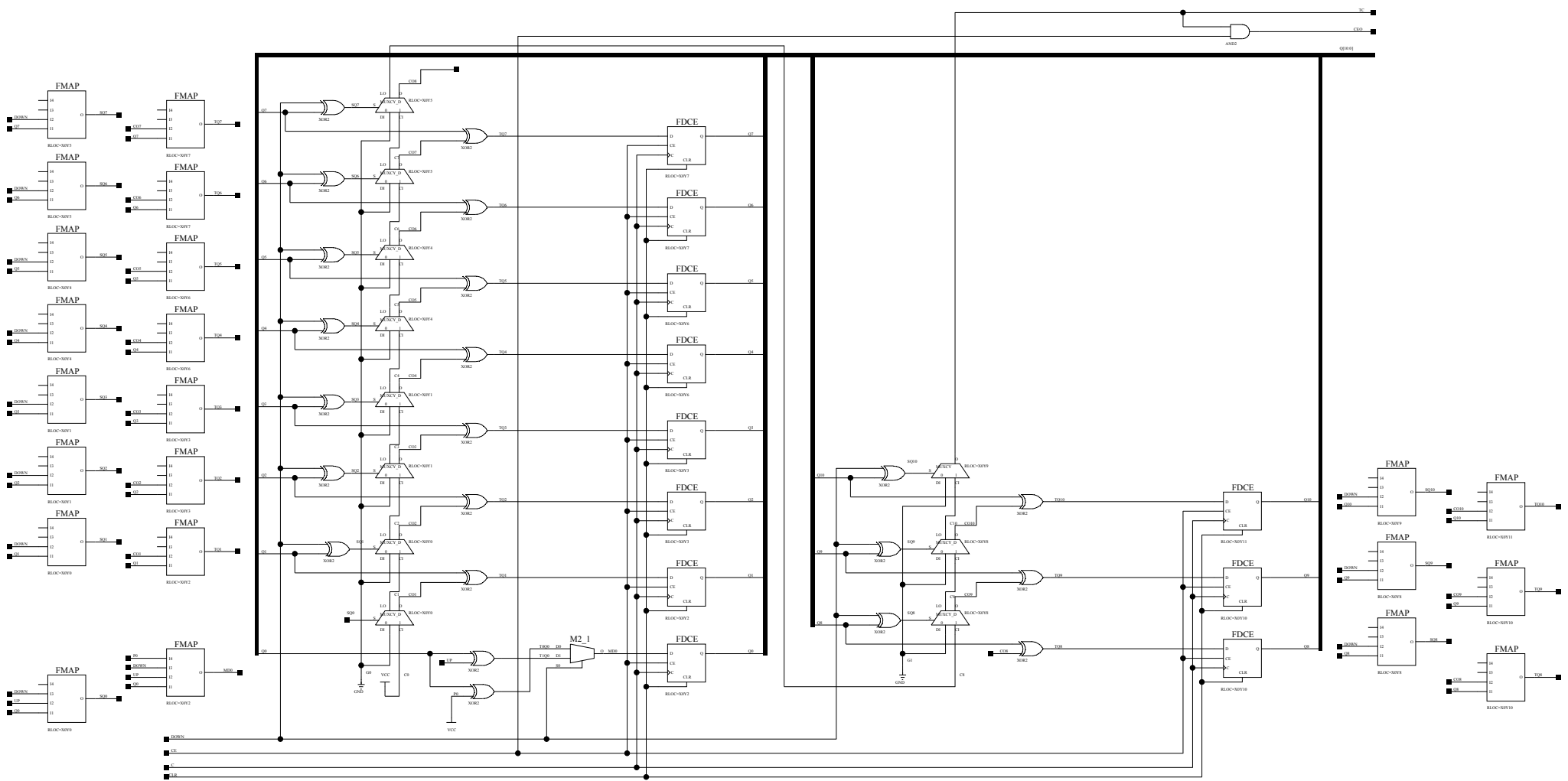
only 120 writes from FULL, 95%

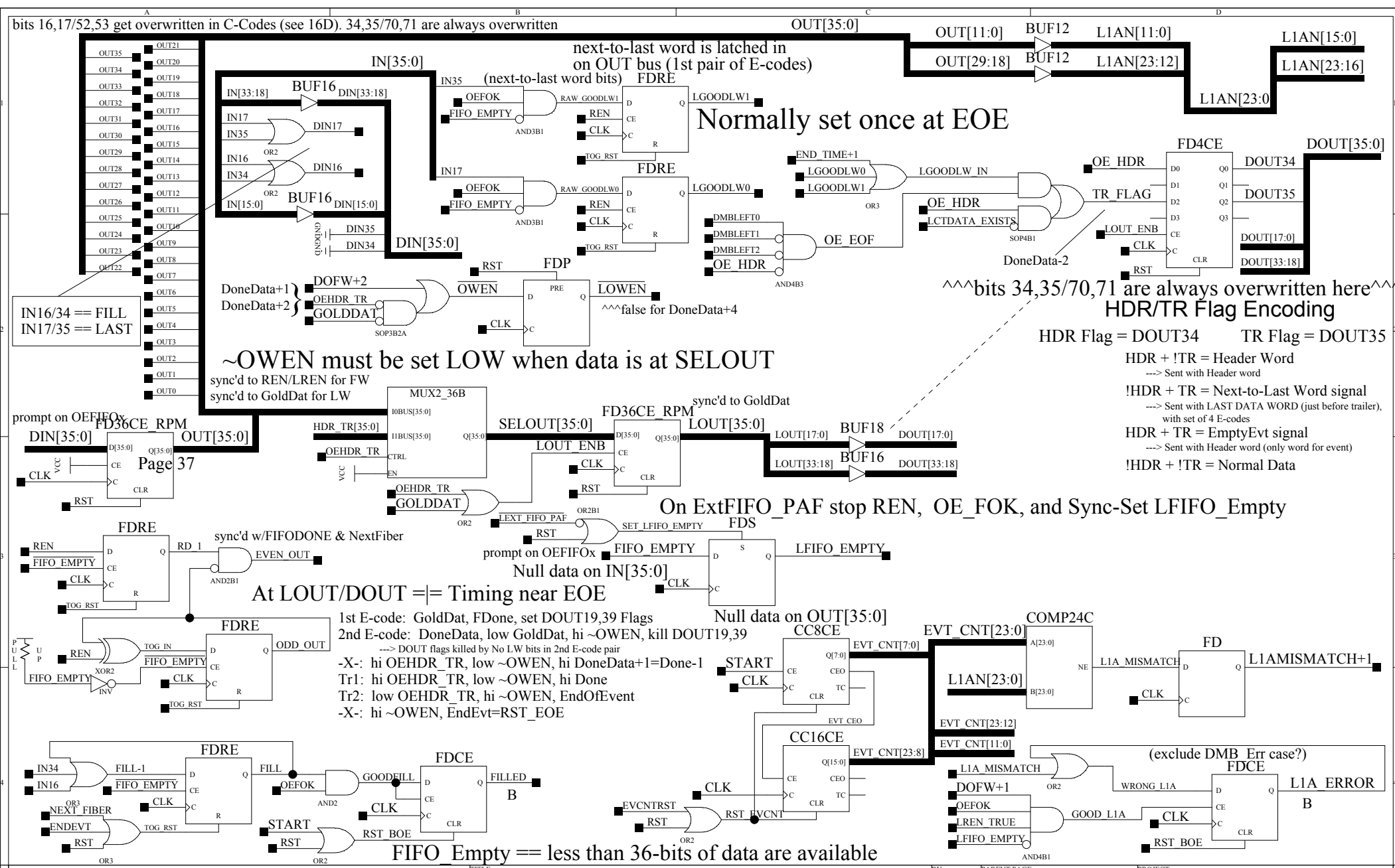




■ CIN
■ C
■ CLR

UP = Increment 1
 UP.DOWN = Decrement 1
 DOWN = Decrement 2
 Assume that CE includes DOWN+UP





IN16/34 == FILL
 IN17/35 == LAST

prompt on OE_FIFOX
 DIN[35:0]
 FD36CE RPM
 Page 37

sync'd w/FIFODONE & NextFiber
 EVEN OUT

sync'd to REN/LREN for FW
 sync'd to GoldDat for LW

sync'd to GoldDat
 LOUT ENB

On ExtFIFO_PAF stop REN, OE_FOK, and Sync-Set LFIFO_Empty

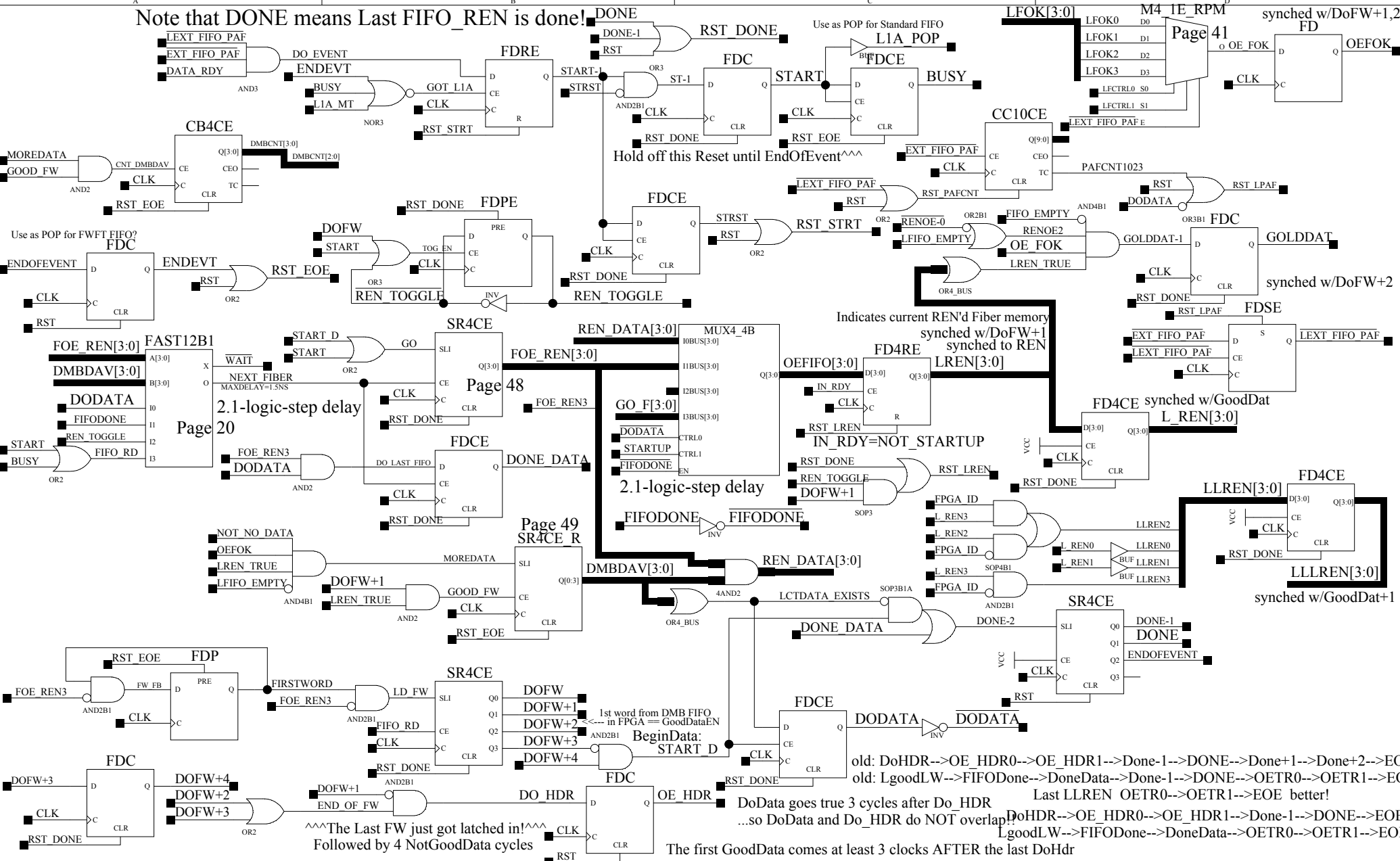
THE OHIO STATE UNIVERSITY
 PHYSICS DEPARTMENT ELECTRONICS LAB
 174 WEST 18TH AVE, COLUMBUS OH 43210

TITLE Read Control
 DDU Input Controller Logic
 CMS CSC Electronics

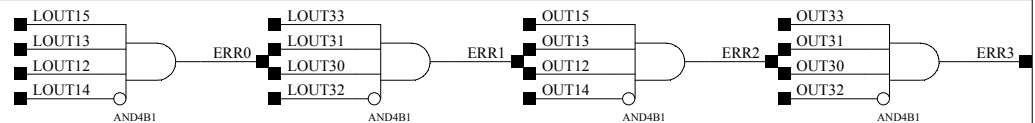
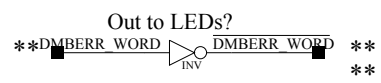
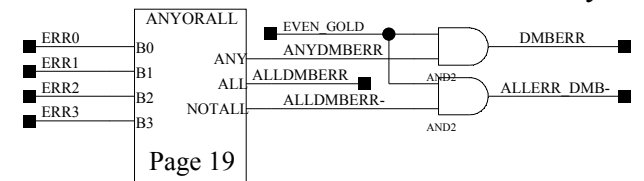
BY JRG
 DATE 10-17-2013_17:59

PARENT PAGE 2, 2D
 PROJECT D785D
 FILE RD CTRL .1
 PAGE 16

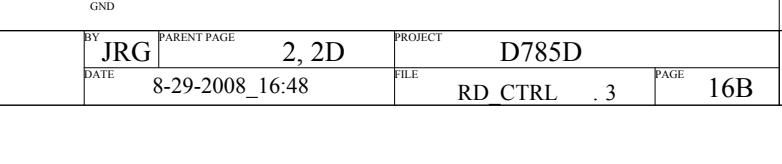
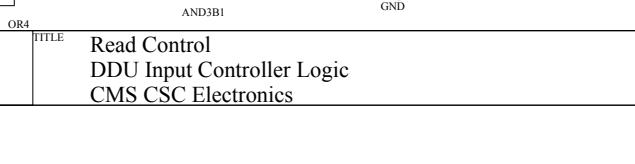
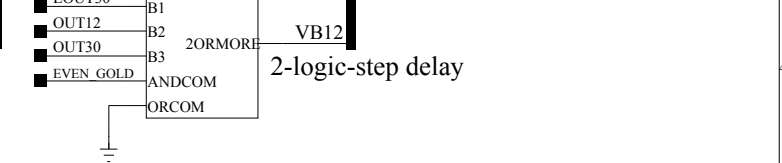
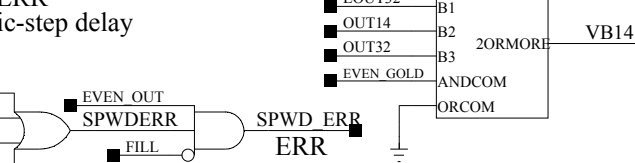
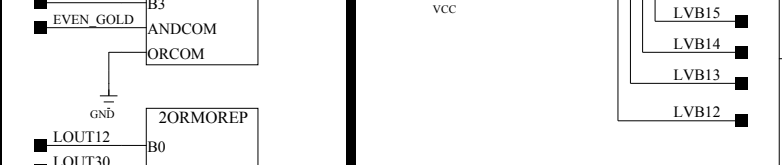
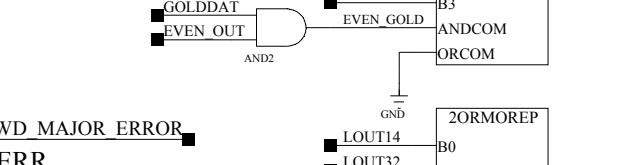
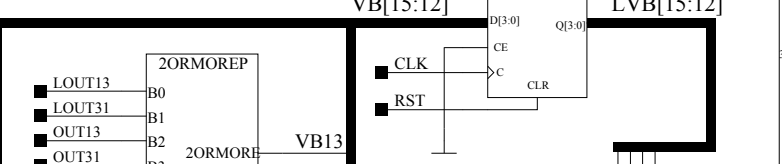
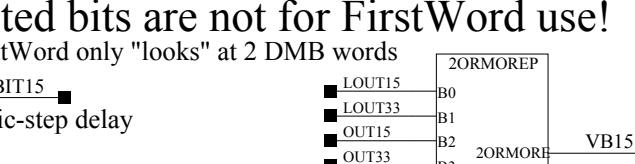
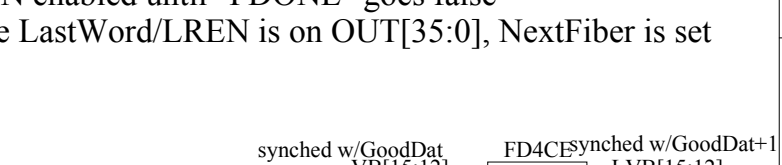
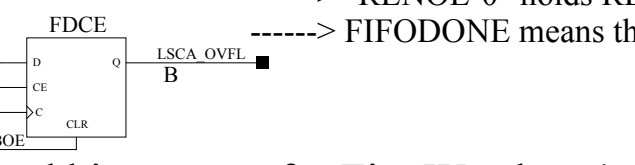
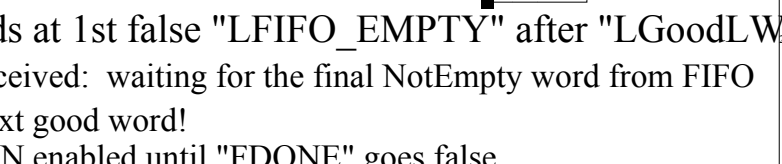
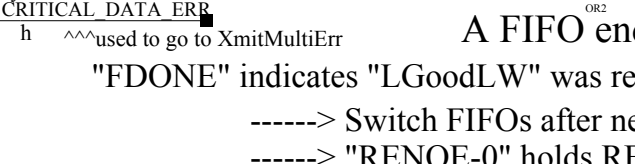
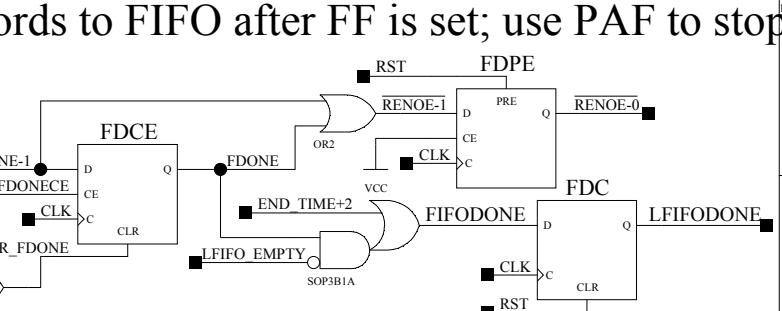
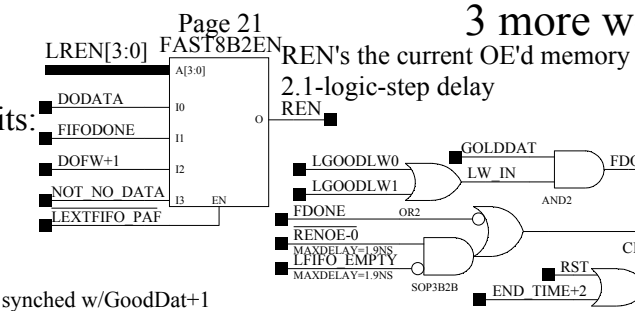
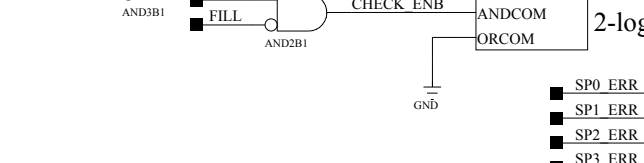
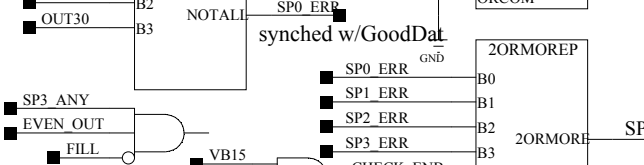
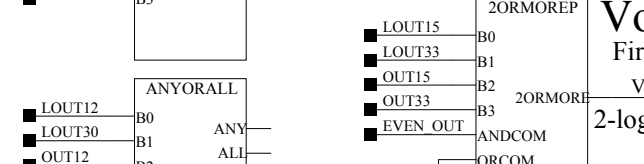
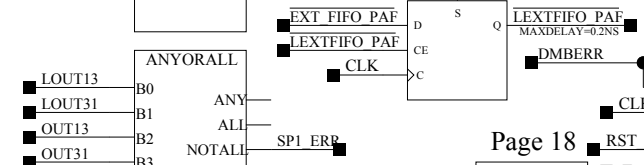
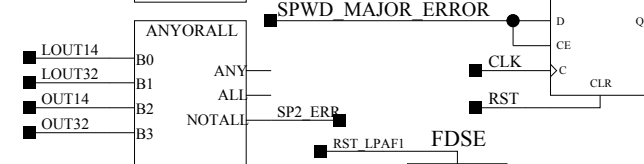
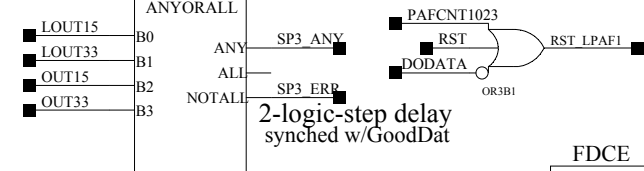
3 more words to FIFO after FF is set; use LEXT FIFO PAF to stop REN/OWEN!



Check for DMB Error Word and consistency:



Check consistency of the four "Special Word" bits:



3 more words to FIFO after FF is set; use PAF to stop

A FIFO ends at 1st false "LFIFO_EMPTY" after "LGoodLW"

"FDONE" indicates "LGoodLW" was received: waiting for the final NotEmpty word from FIFO

-----> Switch FIFOs after next good word!

-----> "RENOE-0" holds REN enabled until "FDONE" goes false

-----> FIFODONE means the LastWord/LREN is on OUT[35:0], NextFiber is set

Voted bits are not for FirstWord use!

FirstWord only "looks" at 2 DMB words

2-logic-step delay

2-logic-step delay

2-logic-step delay

2-logic-step delay

2-logic-step delay

2-logic-step delay

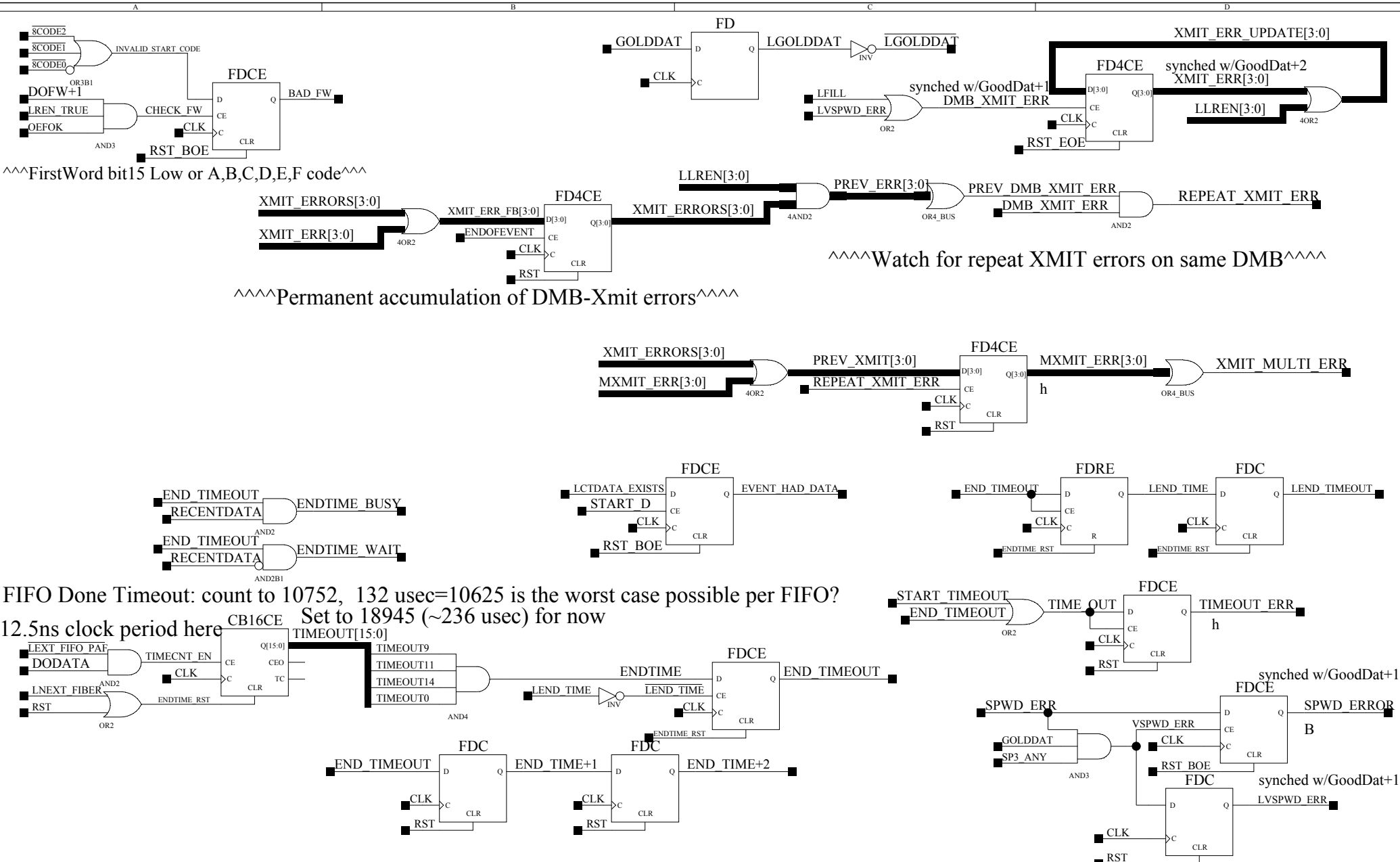
2-logic-step delay

2-logic-step delay

2-logic-step delay

2-logic-step delay

2-logic-step delay

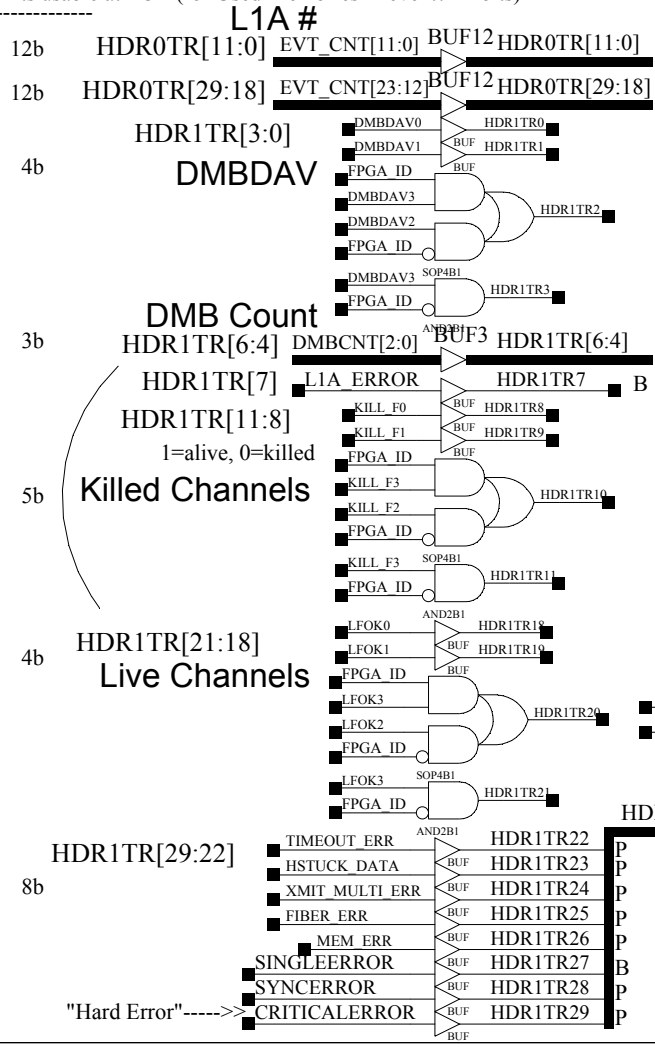


FIFO Done Timeout: count to 10752, 132 usec=10625 is the worst case possible per FIFO?
 12.5ns clock period here Set to 18945 (~236 usec) for now

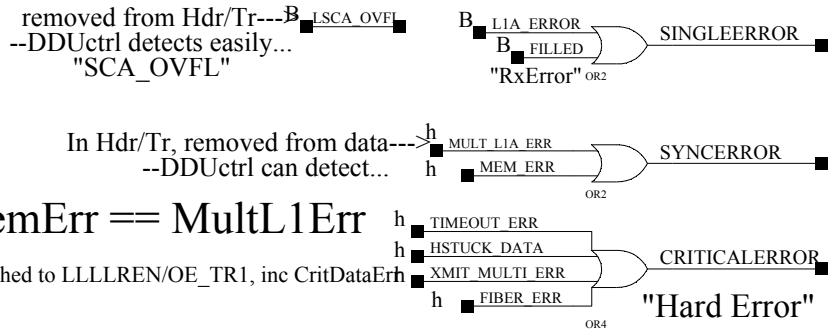
Status Monitor

Pick 8 Status signals, include in DAQ HDR/TR
 -create logic for OEHDR/TR and their format
 Also set 4 FMM bits for each input channel

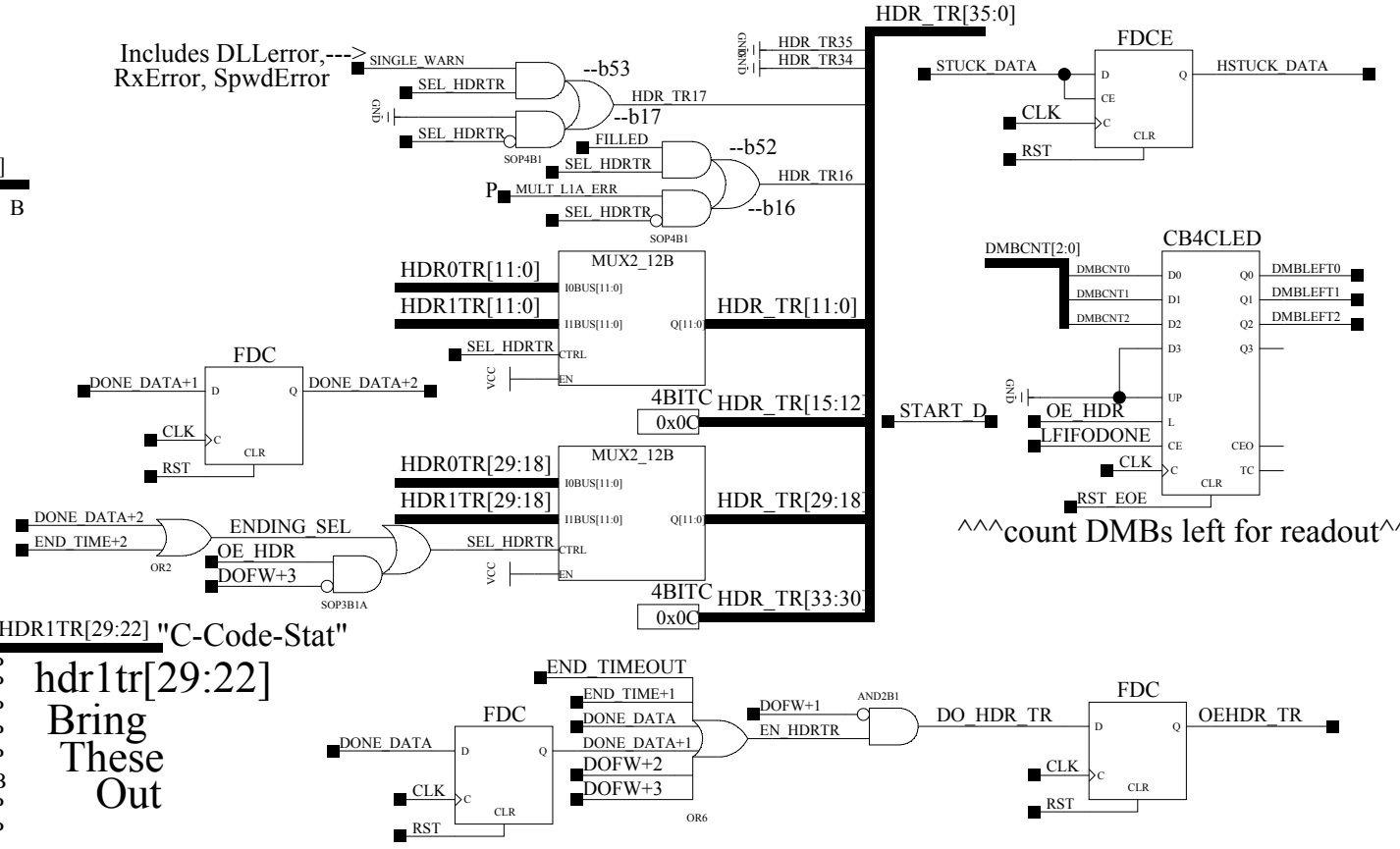
#Bits usable at EOE (for Used Memories in event? 22 bits)



SyncErr AND ~MemErr == MultL1Err
 synced to LLLLREN/OE_TR1, inc CritDataErh

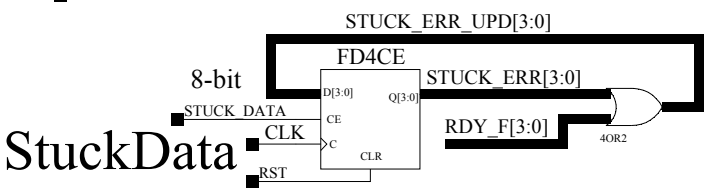
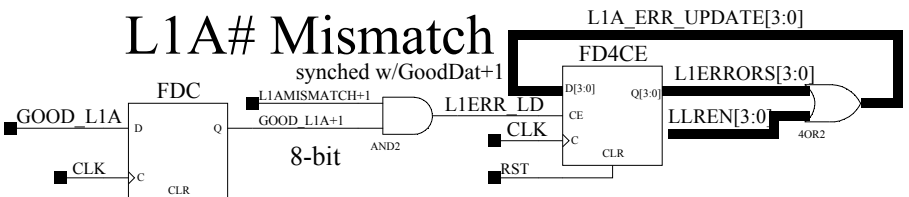


Includes DLLerror, RxError, SpwdError

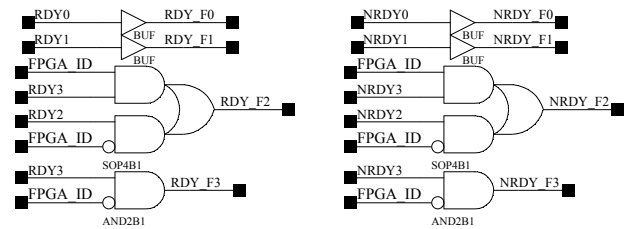


HDR1TR[29:22] "C-Code-Stat"
 Bring These Out

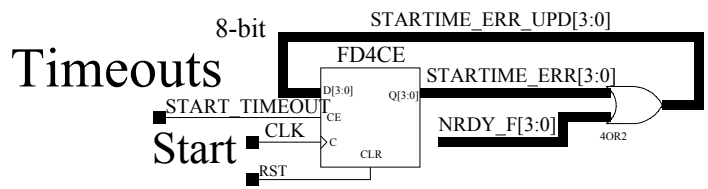
L1A# Mismatch



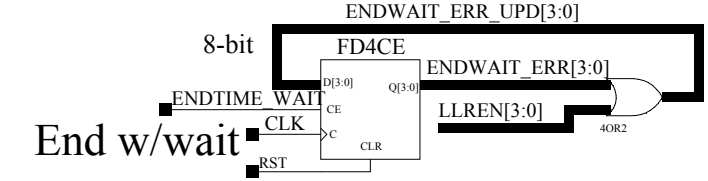
StuckData



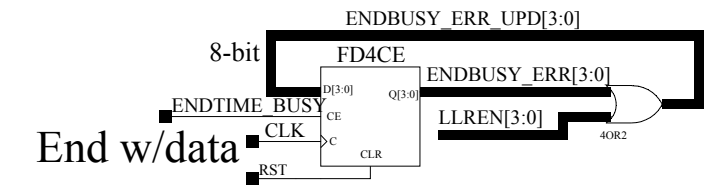
Timeouts



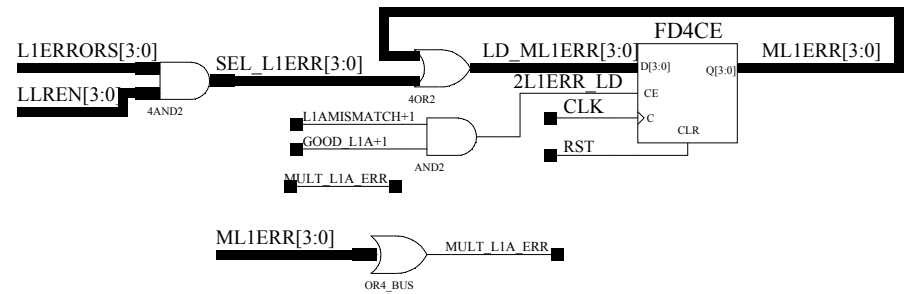
End w/wait



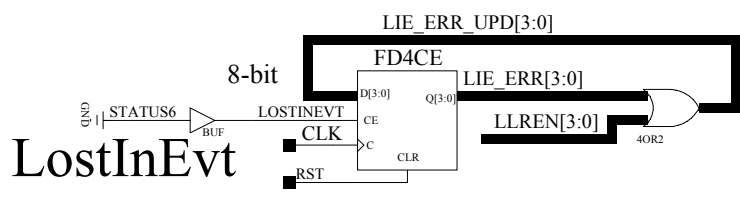
End w/data



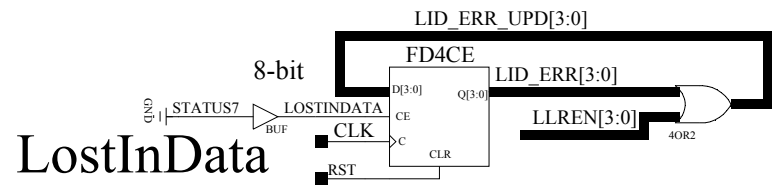
Multi-L1A# Mismatch



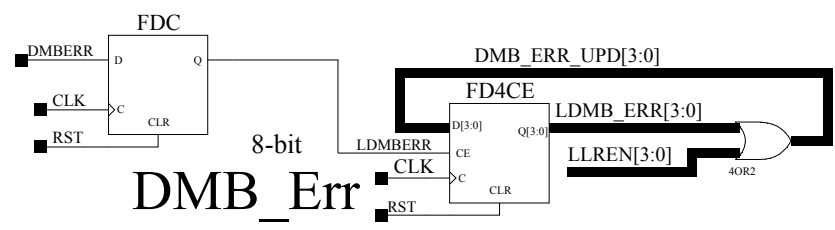
LostInEvt



LostInData



DMB_Err



H1: 0x/5T/NN.NNNN/XXX/I.II/VK

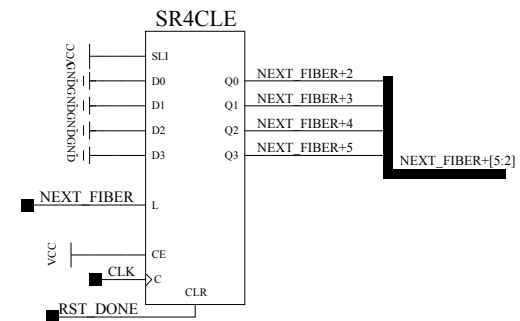
H2: 0x/8000/0001/8000/HHHH

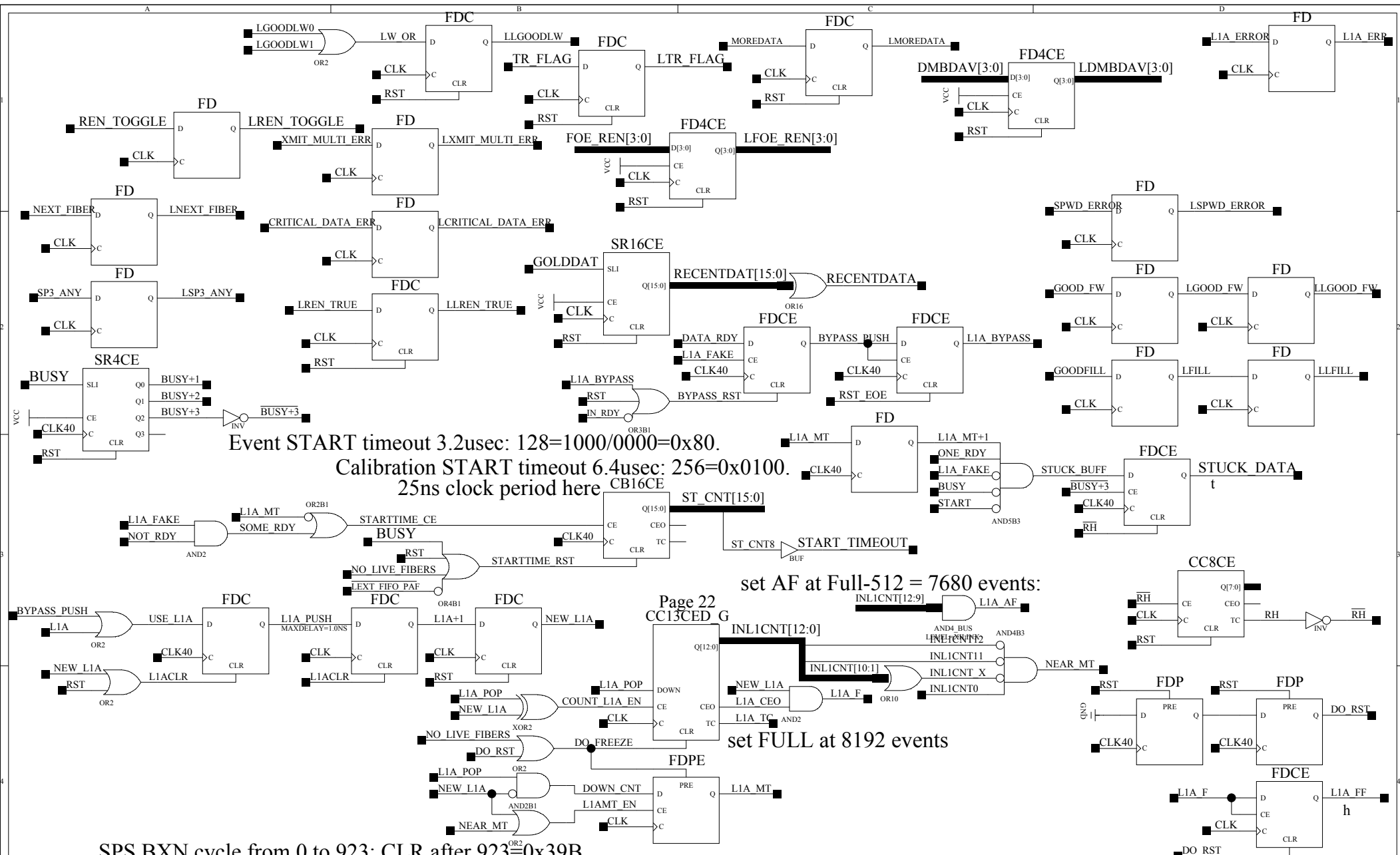
H3: 0x/LLLL/oooo/ZZZZ/GGMY

T-2: 0x/8000/FFFF/8000/8000

T-1: 0x/SSSS.SSSS/QQQQ/PPPP

TR: 0x/A/?/WW.WWWW/RRRR/UUMK





Event START timeout 3.2usec: 128=1000/0000=0x80.

Calibration START timeout 6.4usec: 256=0x0100.

25ns clock period here

set AF at Full-512 = 7680 events:

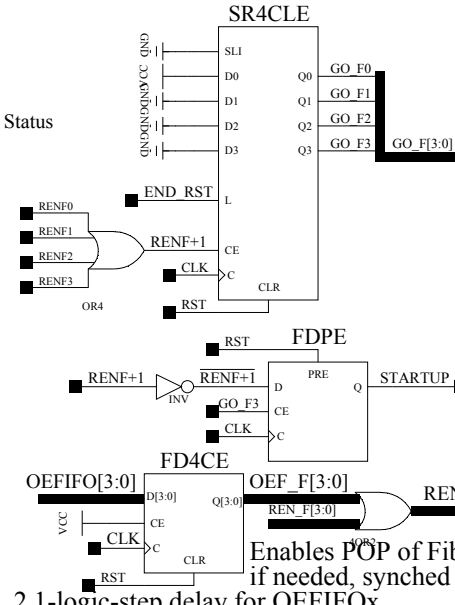
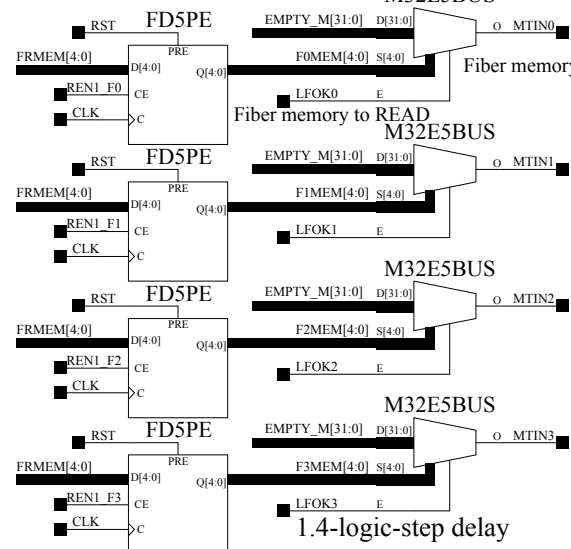
set FULL at 8192 events

SPS BXN cycle from 0 to 923: CLR after 923=0x39B.

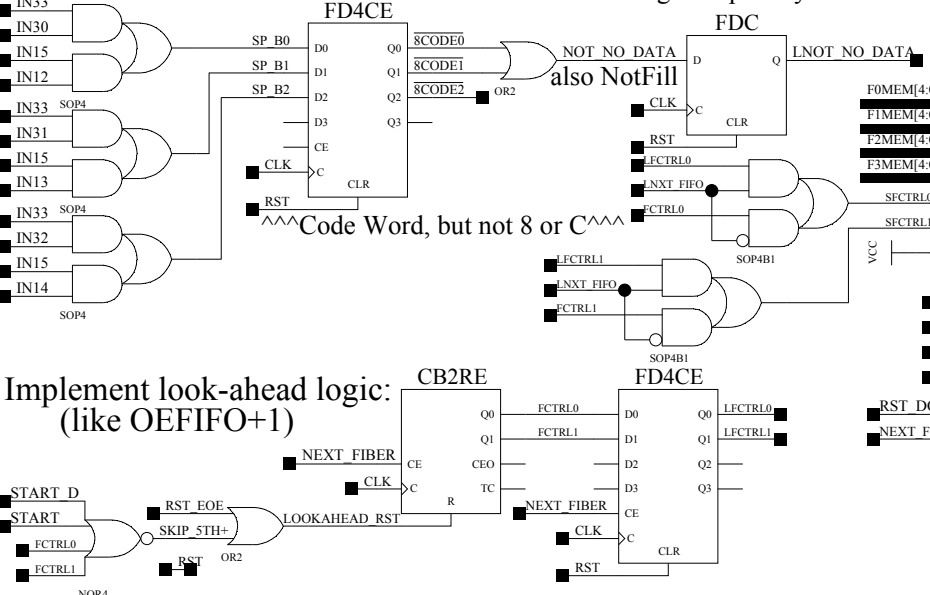
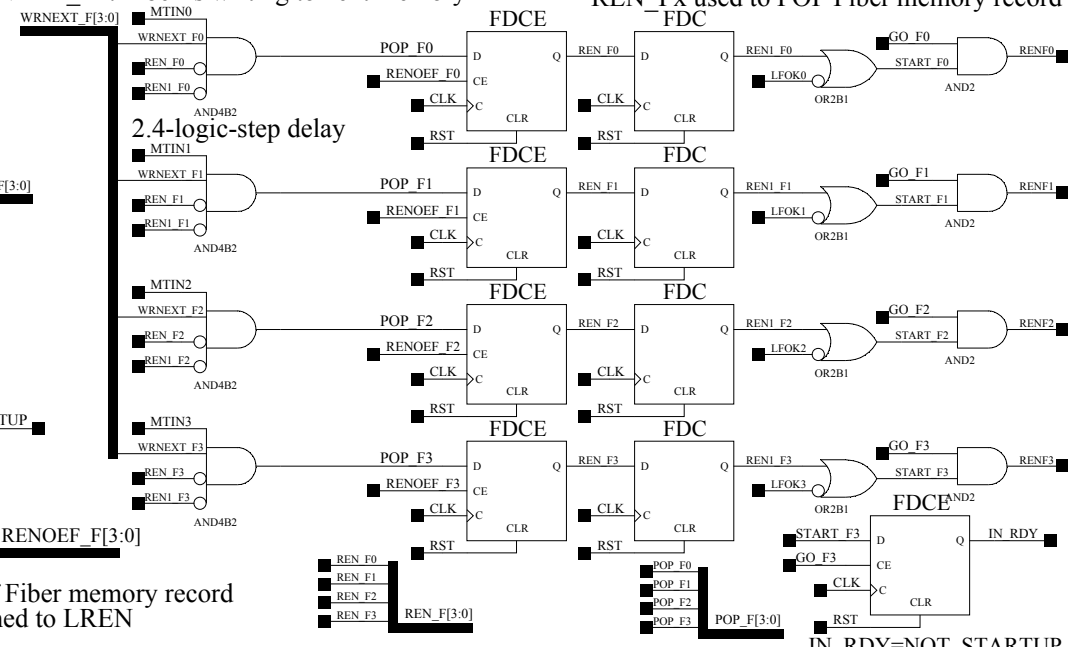
Page 22
CC13CED G

END

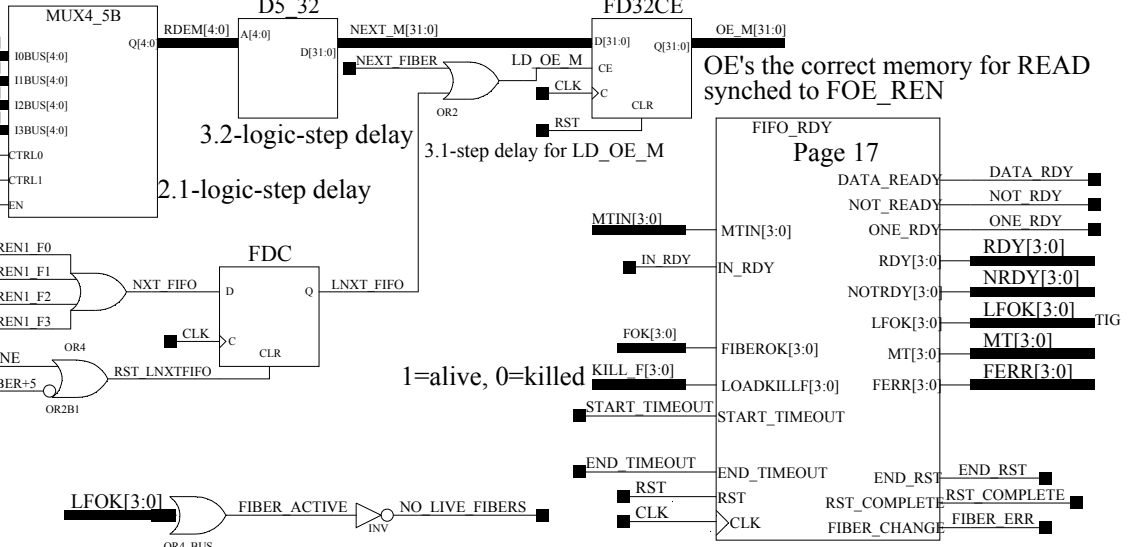
Page 25
M32E5BUS

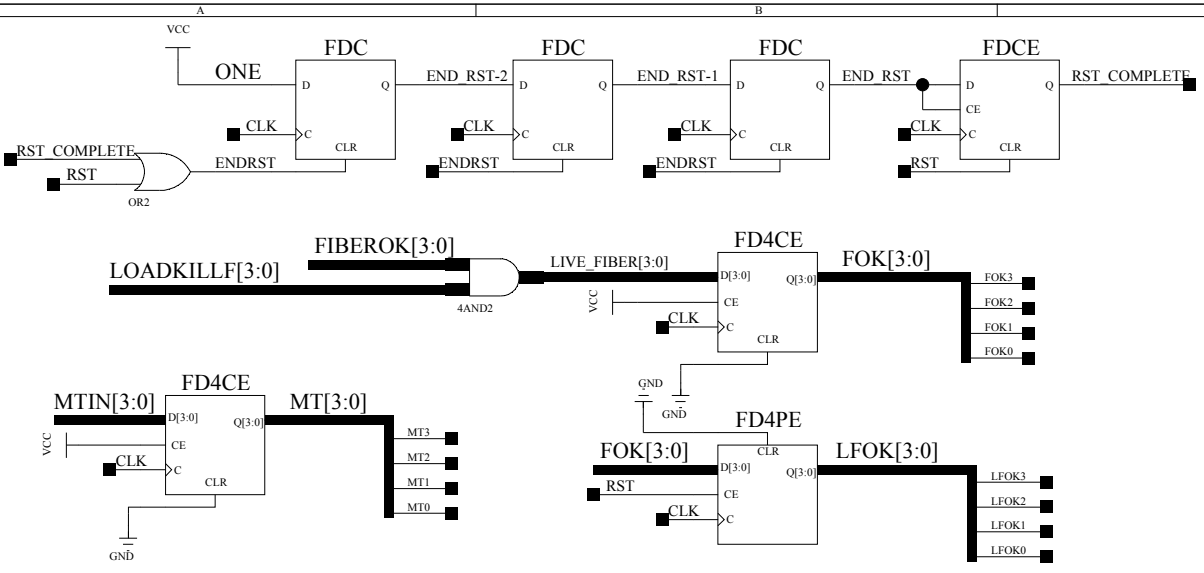


WRNEXT_Fx: Fiber is writing to next memory

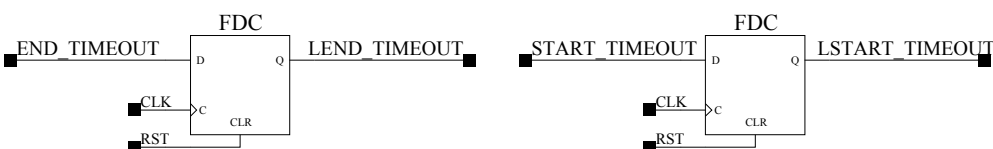
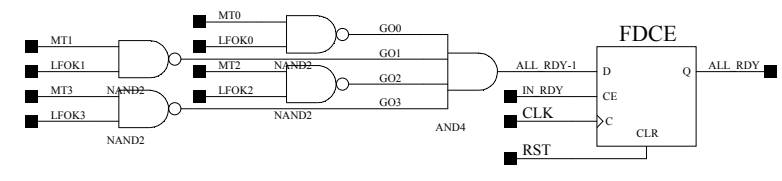


Page 35 D5 32 2.1-logic-step delay for NEXT_FIBER

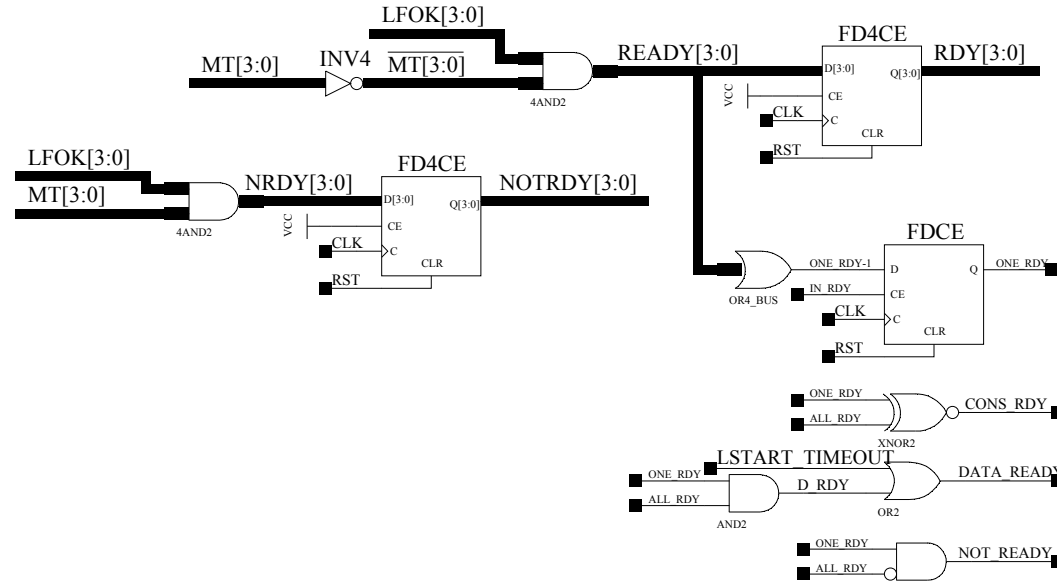


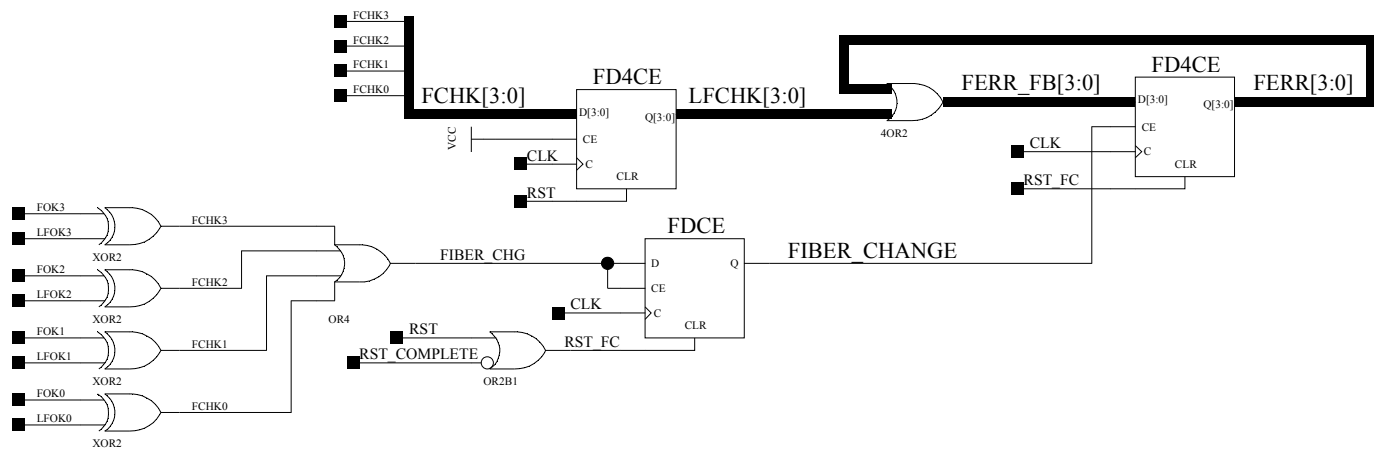


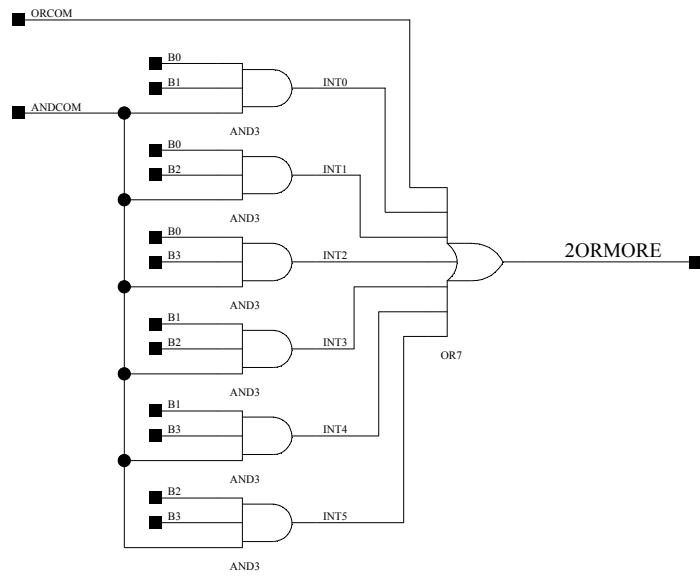
Access FIBEROK from JTAG as a fiber check.
 ---> RESET required after fiber status change for now...
 Change in FIBEROK is BAD! Set error code.
 ...notify FMM and maybe set STATUS bit, but
 ...data is OK until FIFO read time-out occurs.
 ...but how to know WHEN the bad-data comes out?
 ---> timeout will probably occur for that event

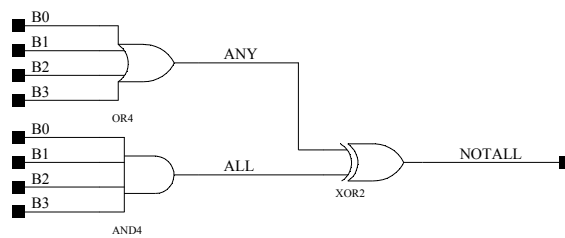


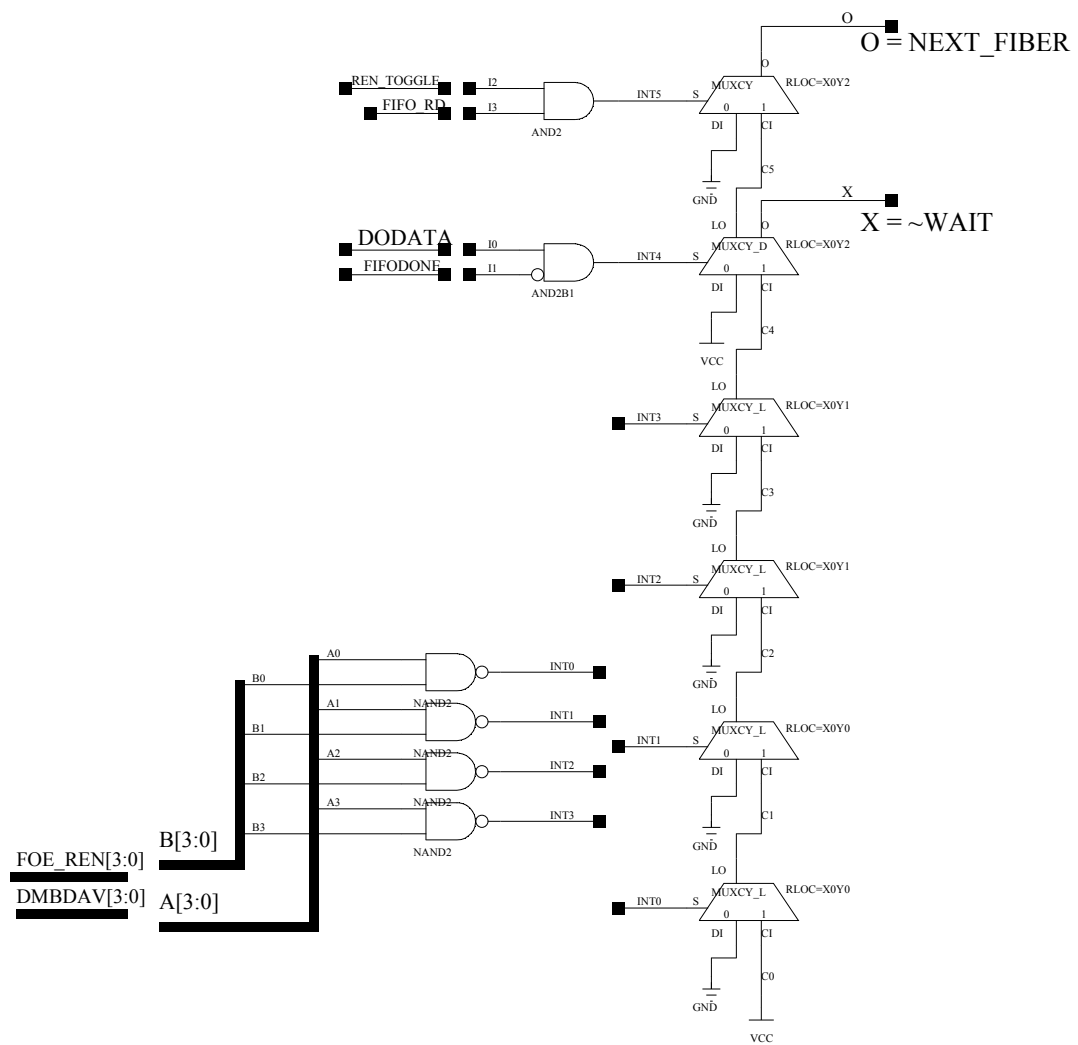
MASK fiber on Start/End TIMEOUT? Kill it in LFOK...



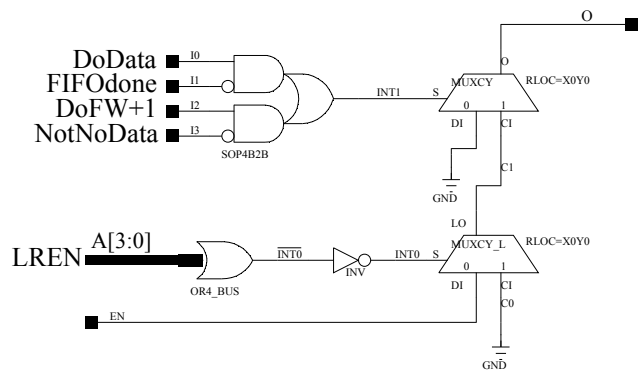








		JRG
Title:	FAST12B1	
Comments:	Custom Fast, Complex Logic for DDU, use 4 MUXCY as OR, 2 as AND similar to: OR of 4 AND2, AND, AND2B1, AND, AND2	
Date:	15th October 2003	Ver: 1
Sheet Size:	B	Rev: A

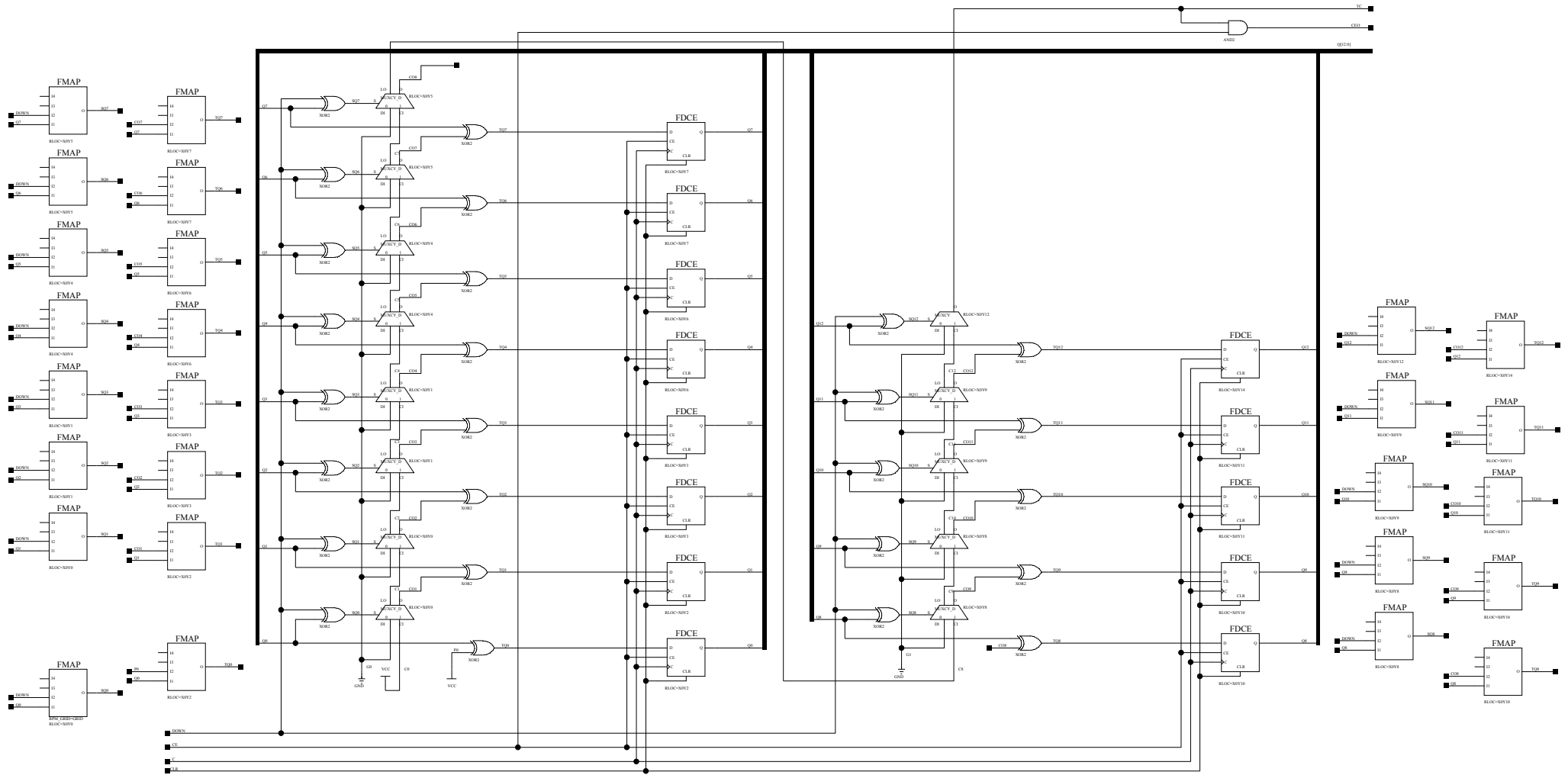


JRG

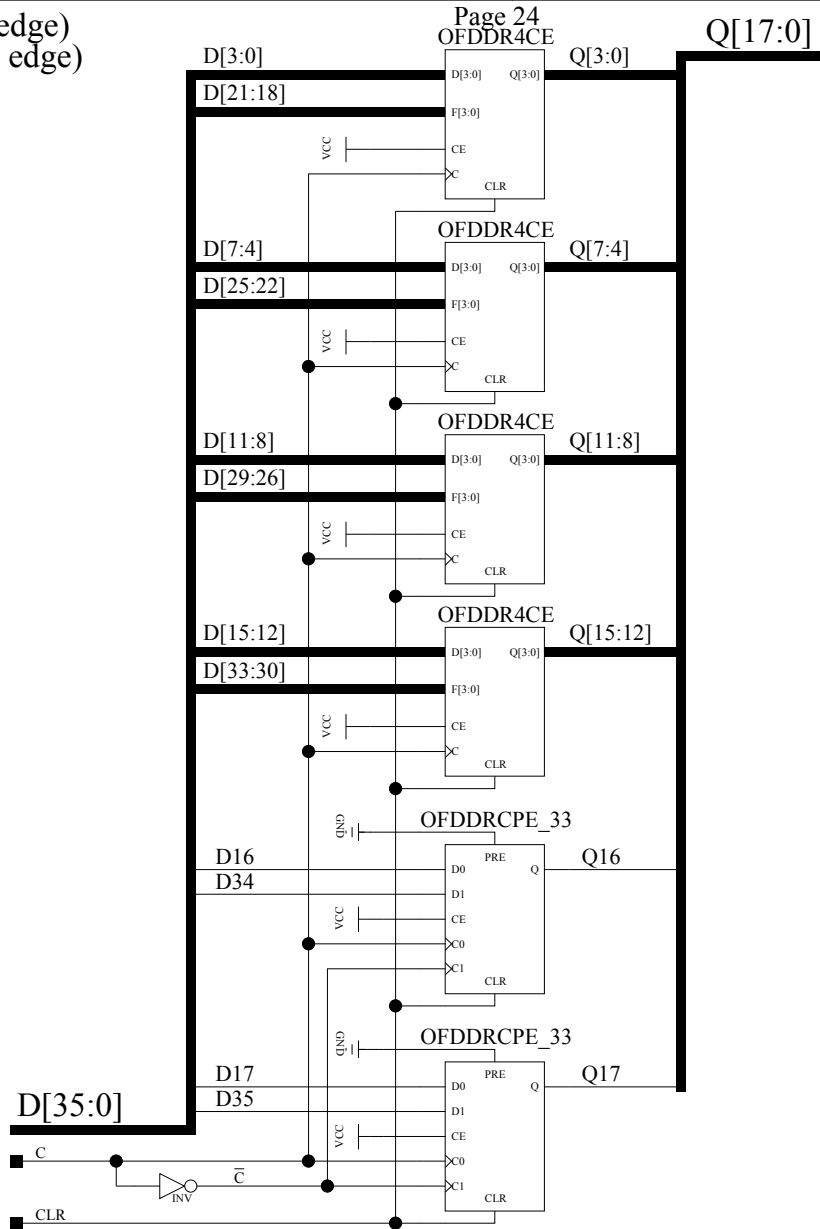
Title:	FAST8B2EN	
Comments:	Custom Fast Complex Logic for DDU, use 2 MUXCY as AND similar to: OR4 AND SOP4B2b	
Date:	14th September 2004	Ver: 1
Sheet Size: B		Rev: A

DOWN = Decrement 1

Assume that CE includes DOWN+UP

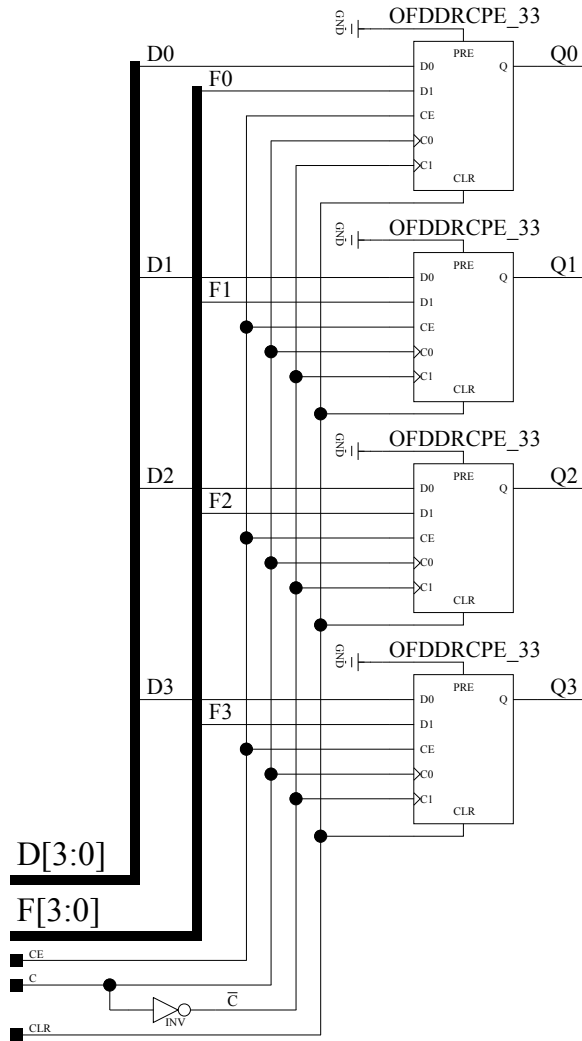


the D byte goes out last (on C rising edge)
 the F byte goes out first (on C falling edge)

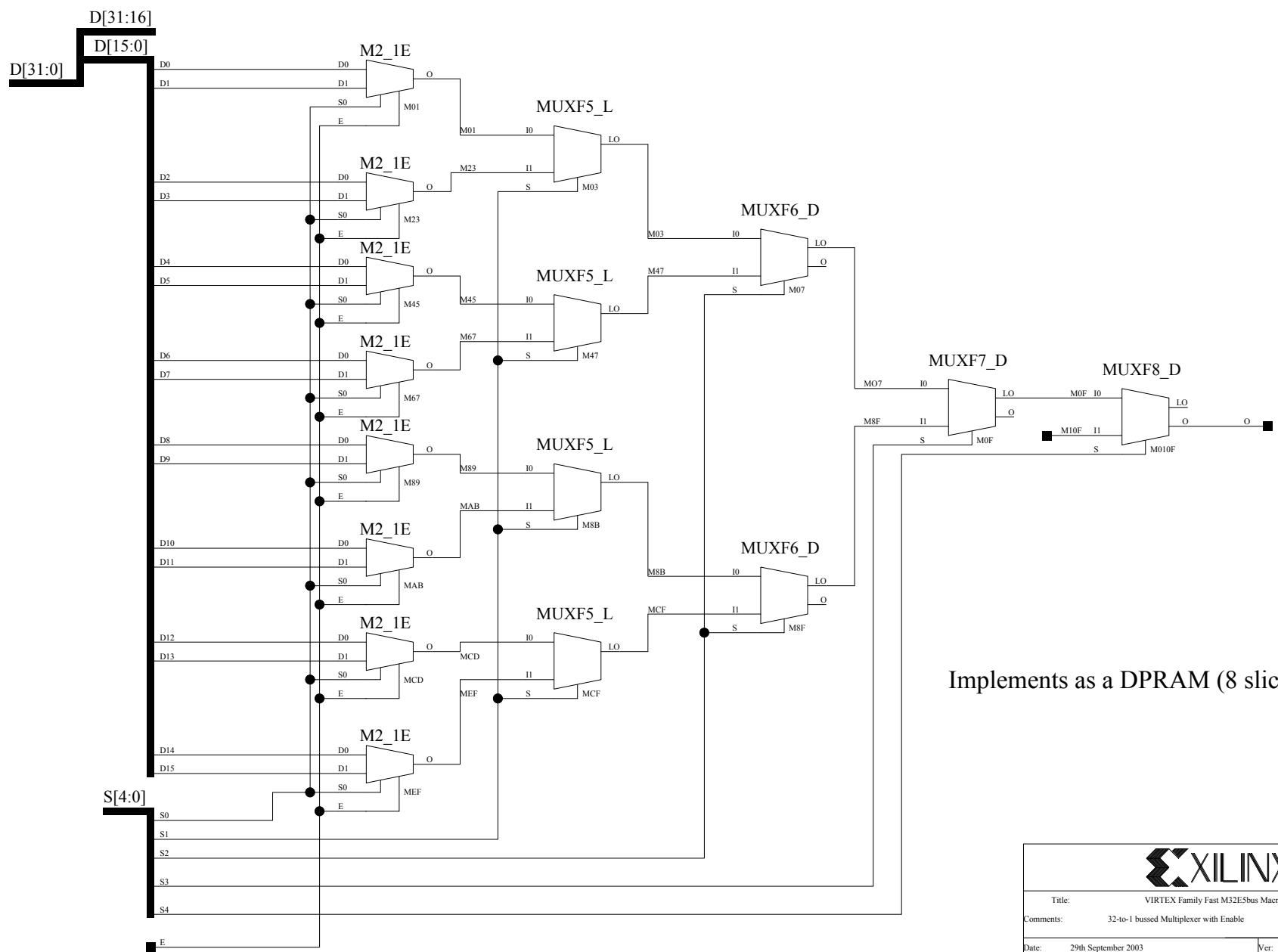


the D byte goes out last (on C rising edge)
 the F byte goes out first (on C falling edge)

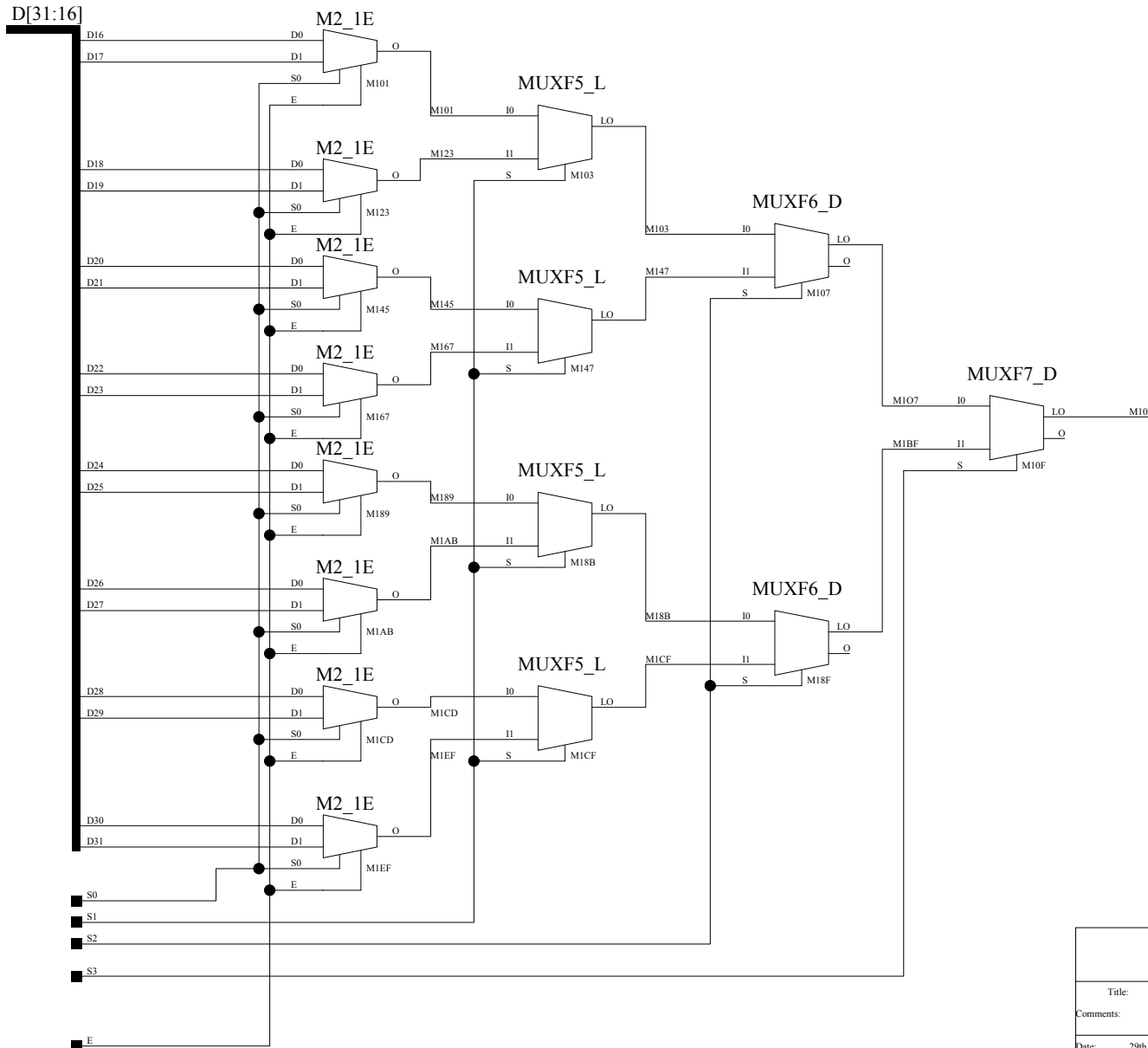
Q[3:0]




Title: VIRTEX Family OFDDR4 Macro	
JRG	
Comments: 4-Bit Output DDR Flip-Flop w/Asynchronous Clear and Clock Enable	
Date: 16th December 2003	Ver: 1
Sheet Size: B	Rev: A



Implements as a DPRAM (8 slices)

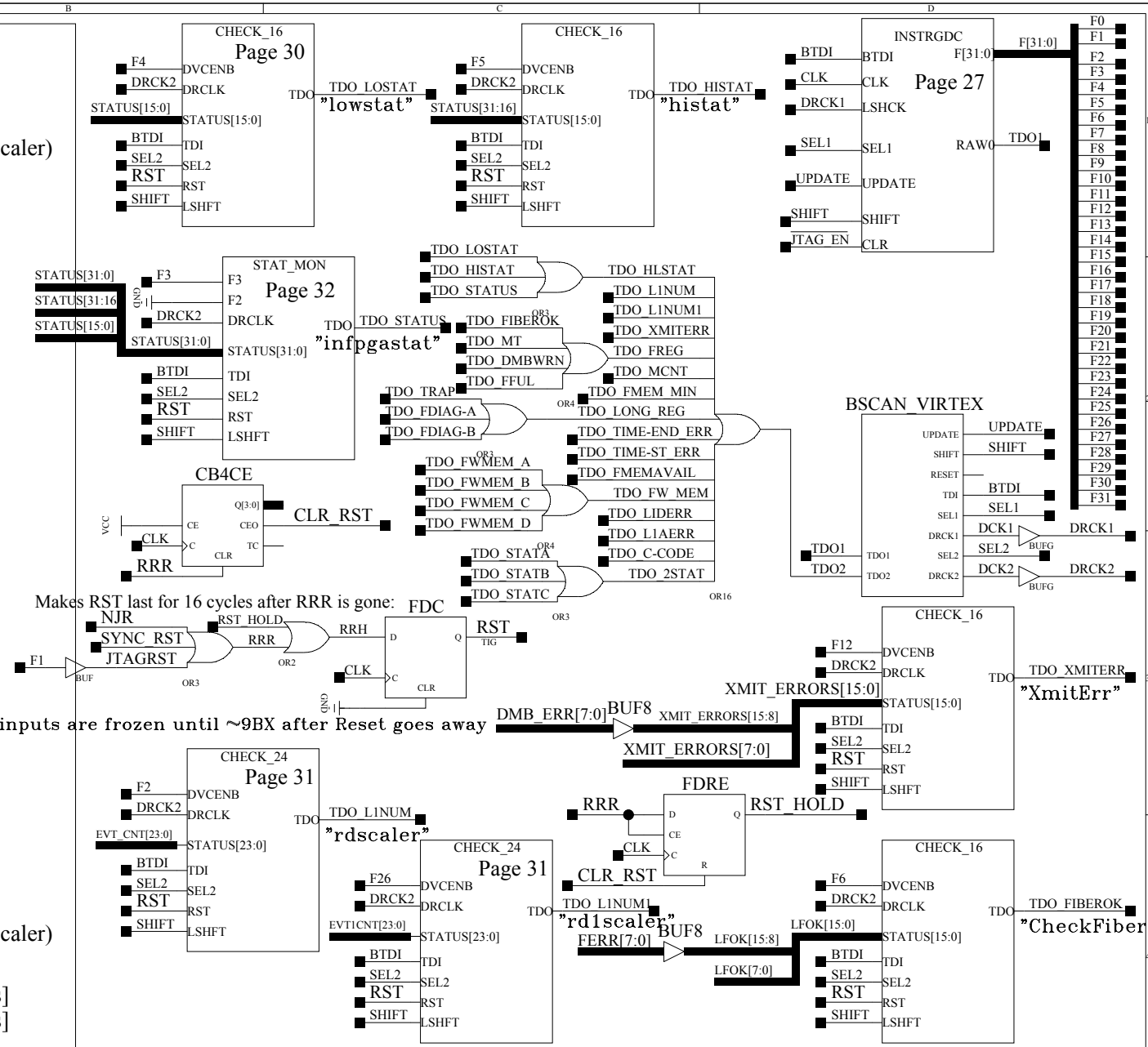


drawn by KS
Copyright (c) 1993, Xilinx Inc.

		JRG
Title:		VIRTEX Family Fast M32ESbus Macro
Comments:		32-to-1 bussed Multiplexer with Enable
Date:	29th September 2003	Ver: 1
Sheet Size:	B	Rev: A

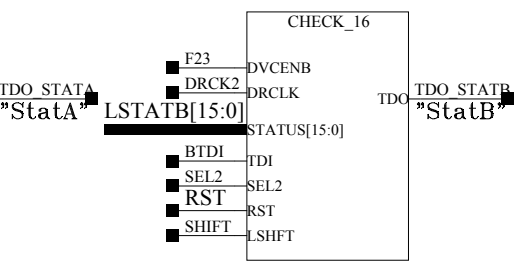
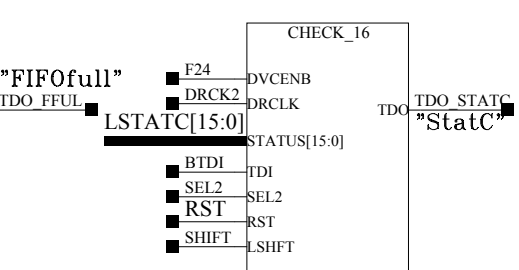
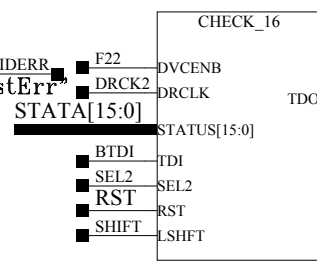
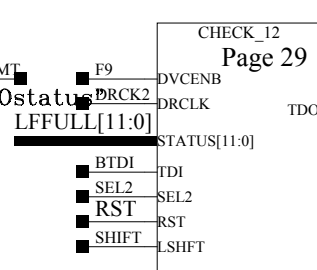
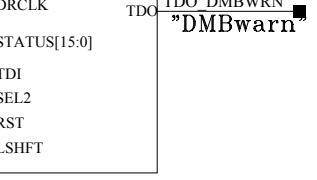
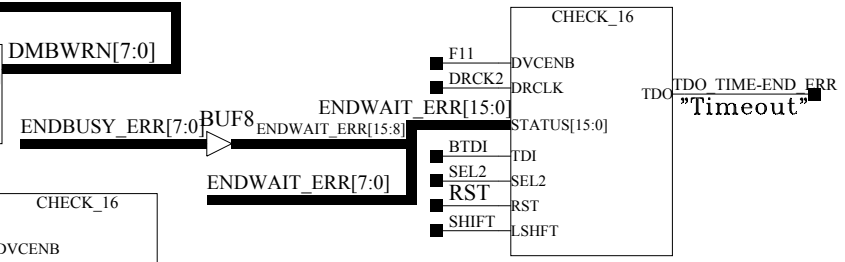
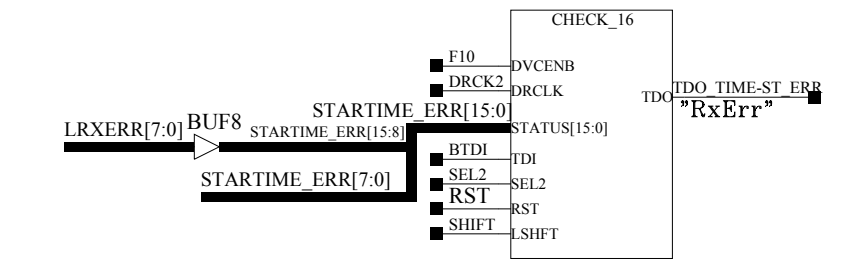
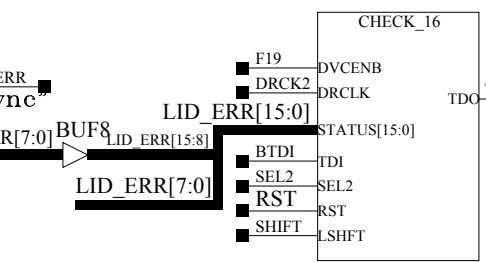
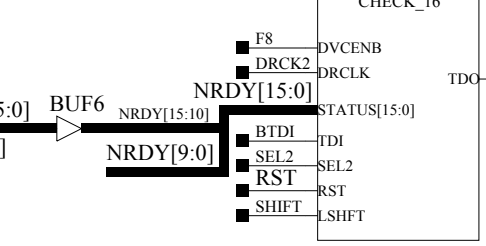
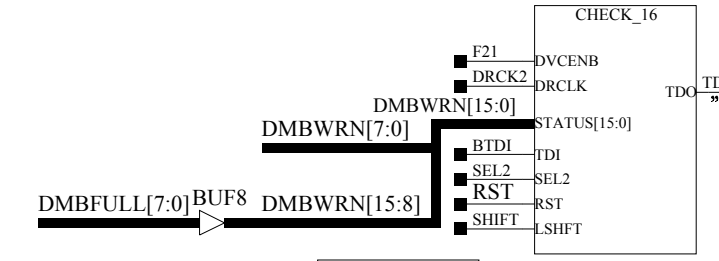
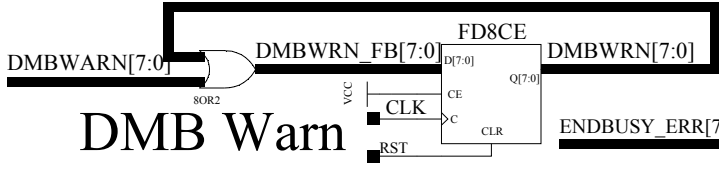
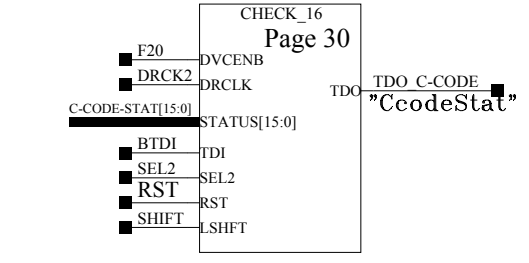
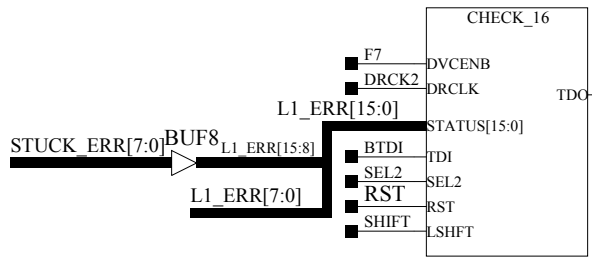
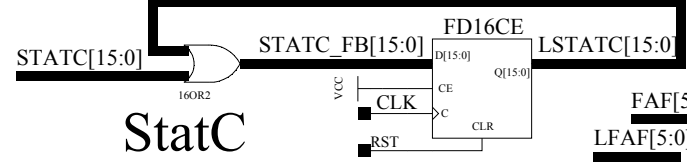
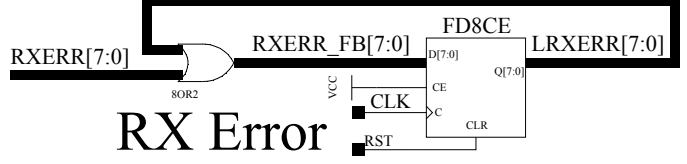
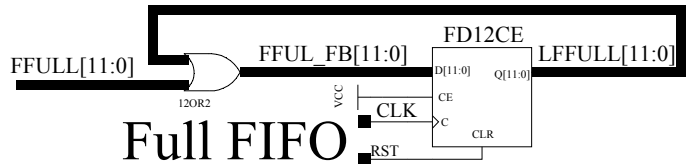
JTAG Instruction Decode

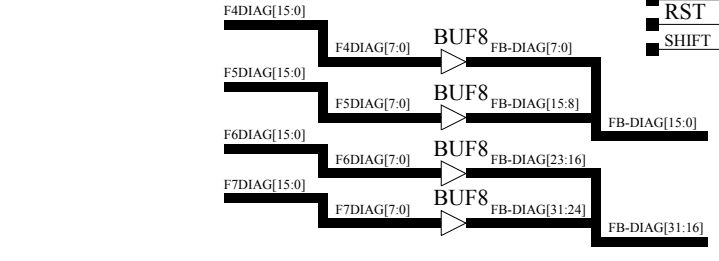
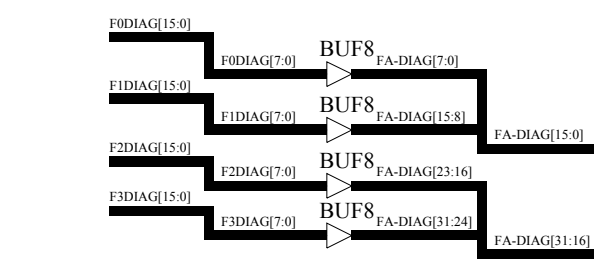
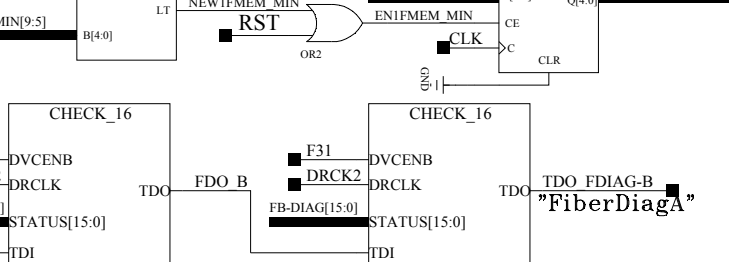
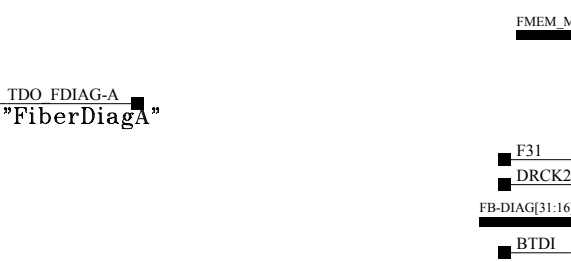
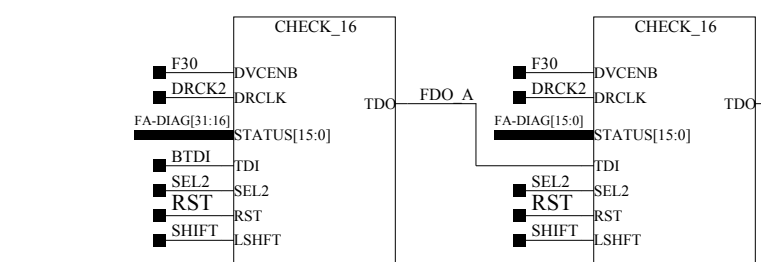
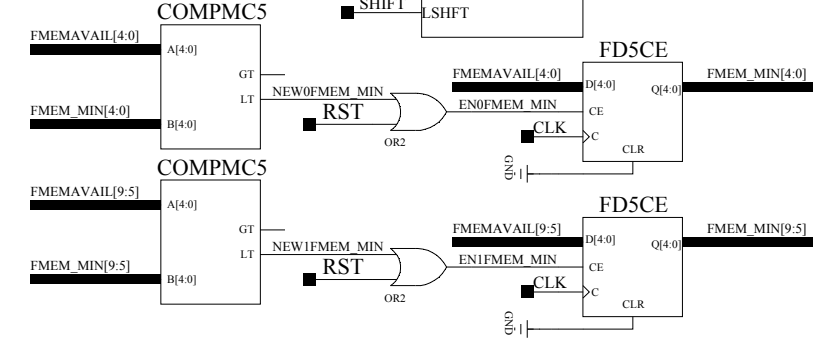
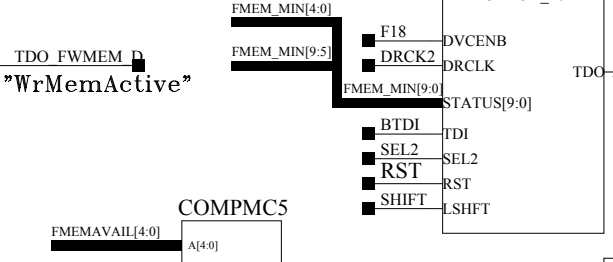
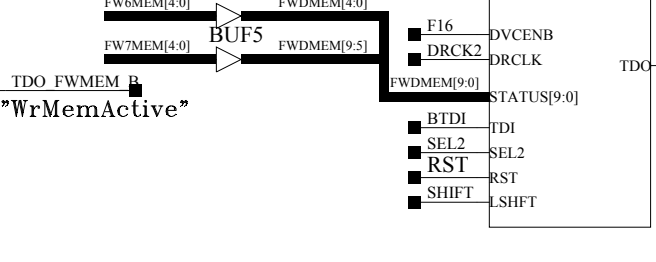
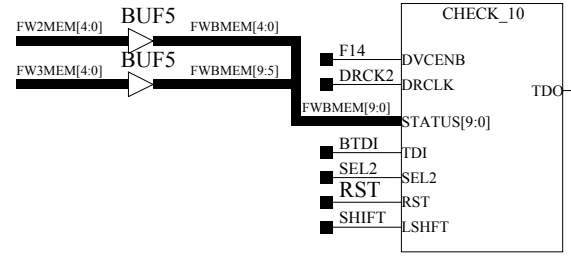
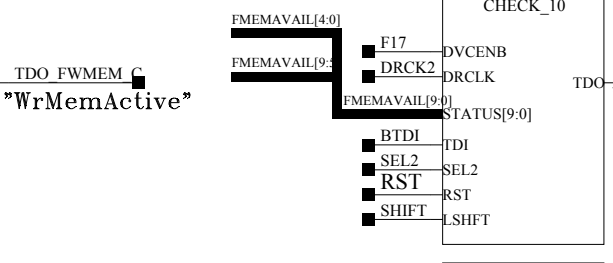
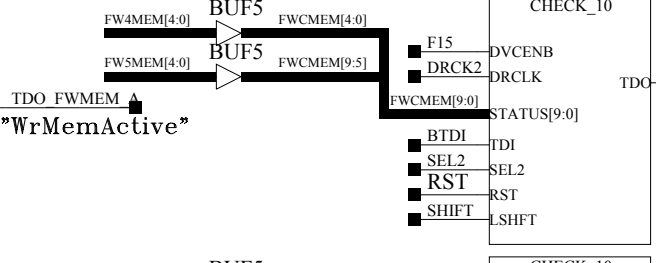
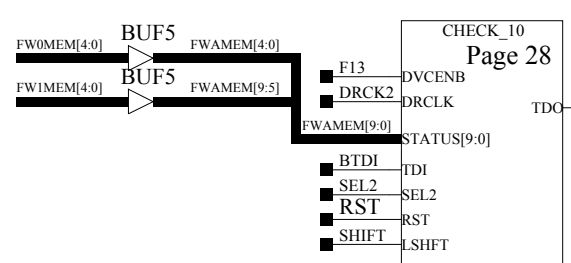
OpCode	Function [OpName]
0	No Operation [NOOP]
1	FPGA Reset [toggle]
2	RdCtrl0 Current DDU L1A Number (24-bit scaler)
3	Check status (capture and shift) [32 bits]
4	Check status, low-word [16 bits]
5	Check status, high-word [16 bits]
7	6a Check FiberOK status (Check_FOK) [8 bits]
6	6b Check FiberErr status (Check_Ferr) [8 bits]
11	7a L1A Mismatch [8-bits]
26	7b Stuck Buffer Errors [8-bits]
25	8a FIFO Empty Status [10-bits]
20	8b Almost Full FIFOs [6-bits]
21	9 Full FIFOs [12-bits]
13	10a Timeout: start [8-bits]
17	10b RX Errors [8-bits]
14	11a Timeout: end-wait [8-bits]
15	11b Timeout: end-active [8-bits]
12	12a Data Xmit Errors [8-bits]
16	12b DMB Errors [8-bits]
13	Fiber 1 & 0 Write Memory [10-bits]
14	Fiber 3 & 2 Write Memory [10-bits]
15	Fiber 5 & 4 Write Memory [10-bits]
16	Fiber 7 & 6 Write Memory [10-bits]
17	FIFO Mem Available 1 & 0 [10-bits]
18	FIFO Mem Min Available 1 & 0 [10-bits]
19	*19a Lost In Data [8-bits]
18	*19b Lost In Event [8-bits]
20	C-Code Status [16-bits]
21	DMB Warn/Full Status [16-bits]
22	Status Register A [16-bits]
23	Status Register B [16-bits]
24	Status Register C [16-bits]
25	Diagnostic Trap [192-bits]
26	RdCtrl1 Current DDU L1A Number (24-bit scaler)
*28	# Mem assigned to Fibers 2-0 [16-bits]
*30	Fiber 3-0 Mem Diagnostic [InRD0, 4 * 8-bits]
*31	Fiber 7-4 Mem Diagnostic [InRD1, 4 * 8-bits]

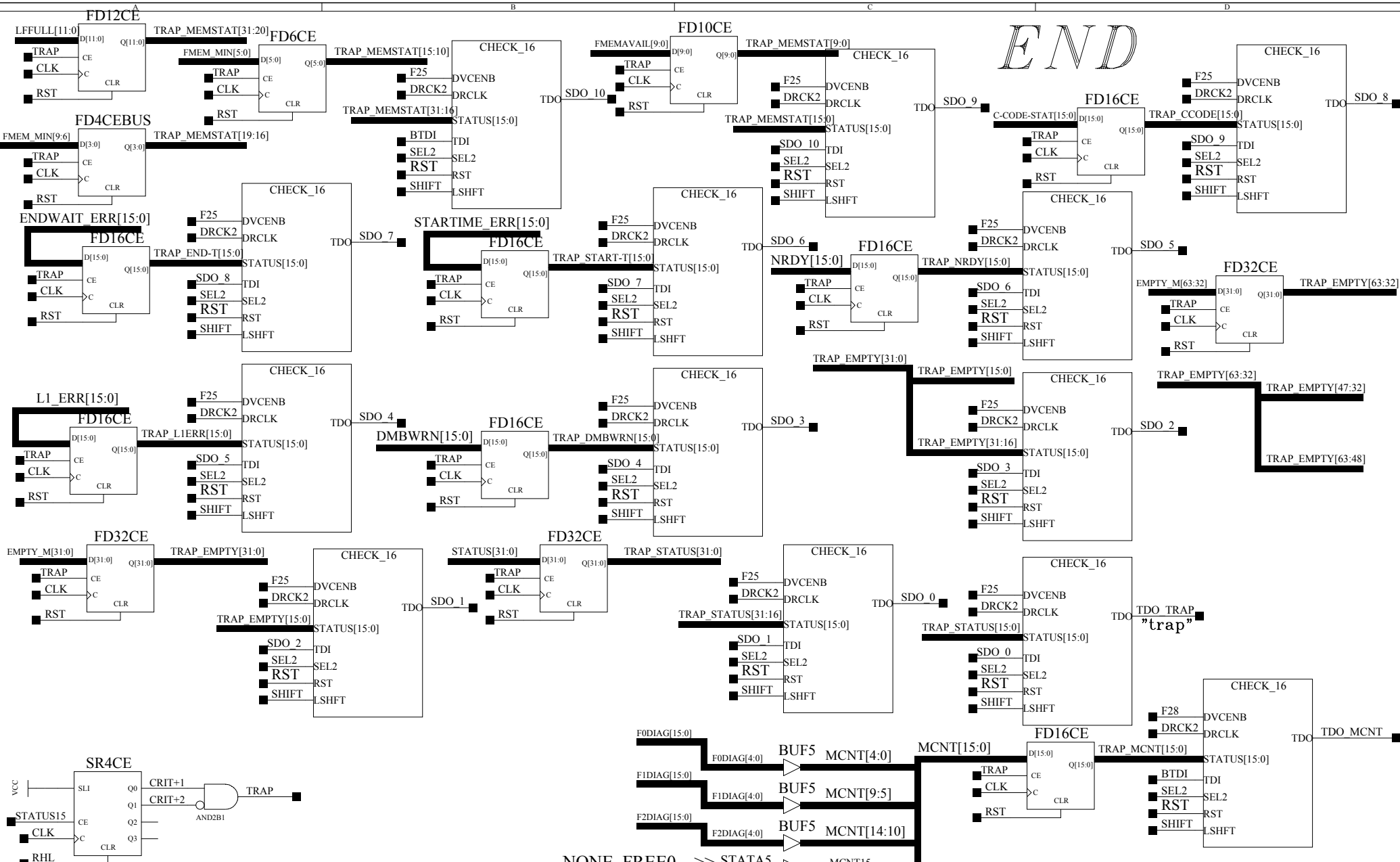


Fiber inputs are frozen until ~9BX after Reset goes away

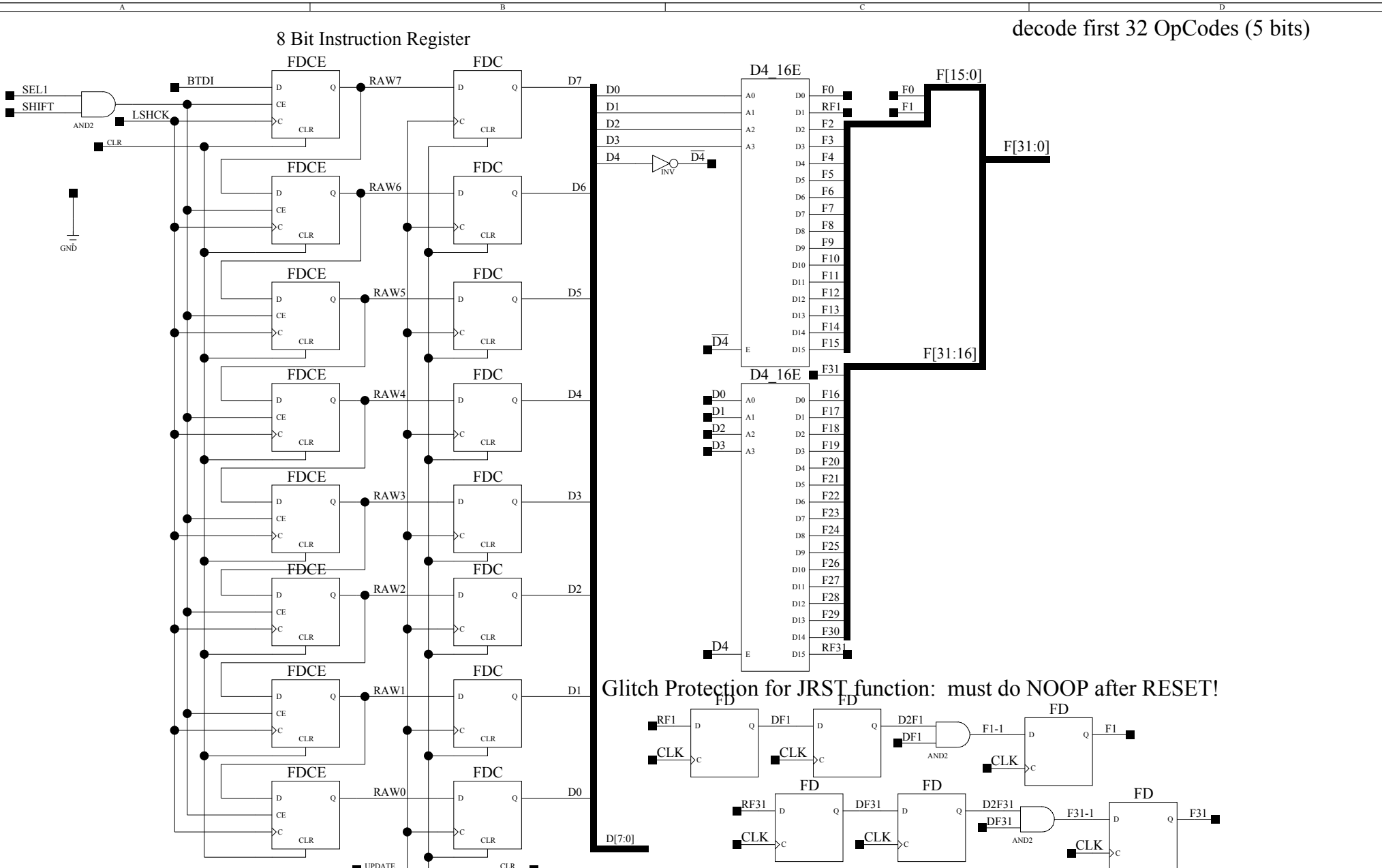
Makes RST last for 16 cycles after RRR is gone:



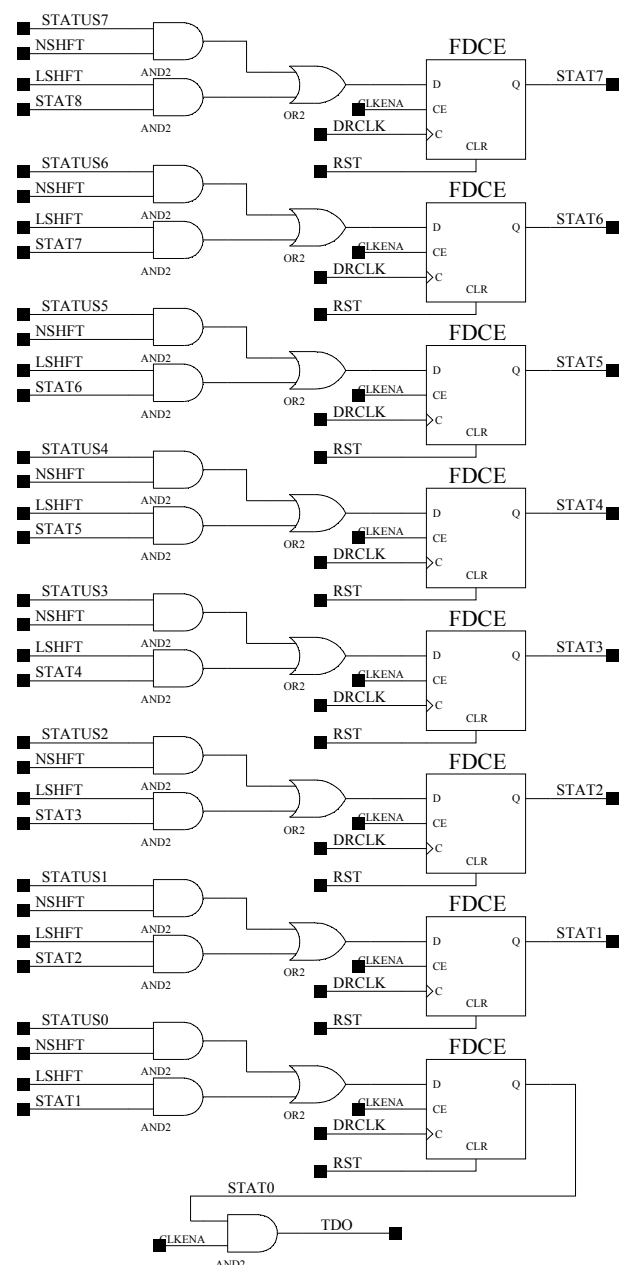
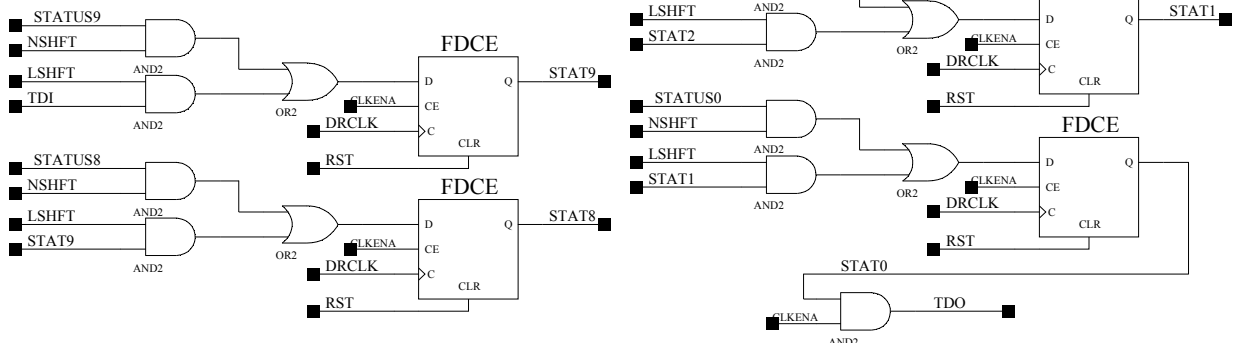
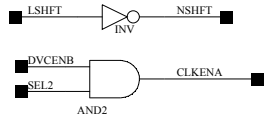
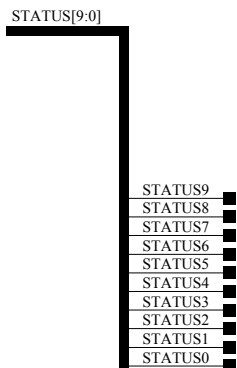




END



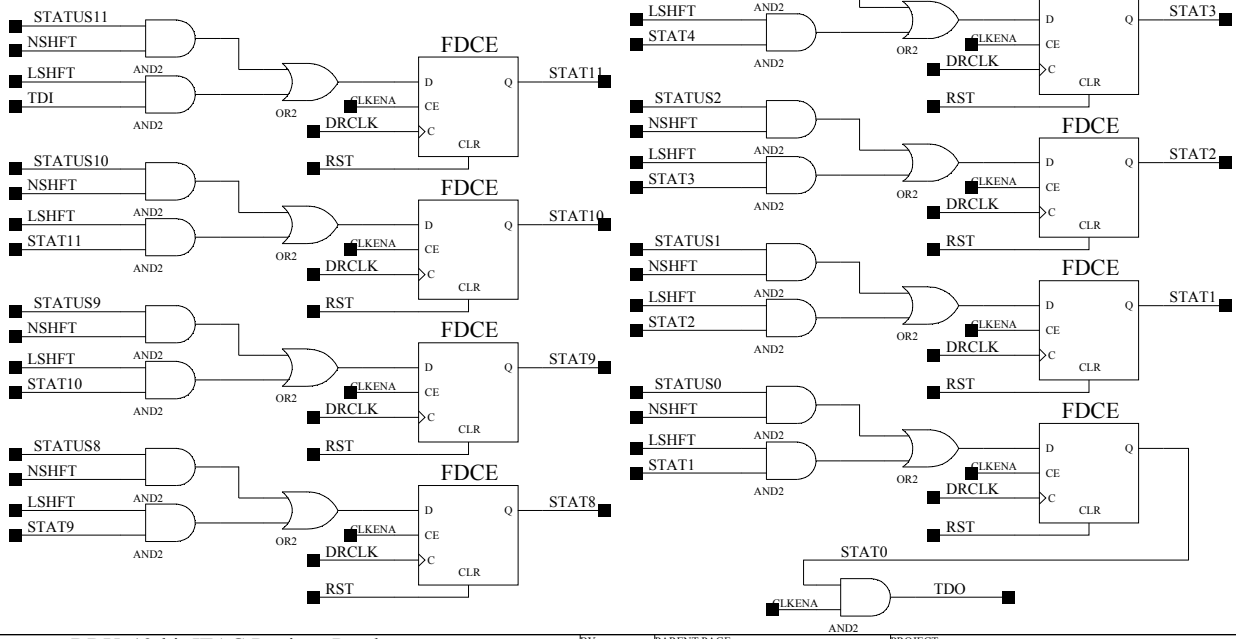
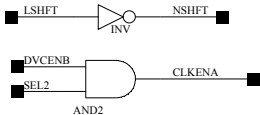
10-bit JTAG Register Read out (on DVCENB)



12-bit JTAG Register Read out (on DVCENB)

STATUS[11:0]

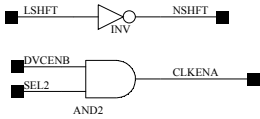
- STATUS11
- STATUS10
- STATUS9
- STATUS8
- STATUS7
- STATUS6
- STATUS5
- STATUS4
- STATUS3
- STATUS2
- STATUS1
- STATUS0



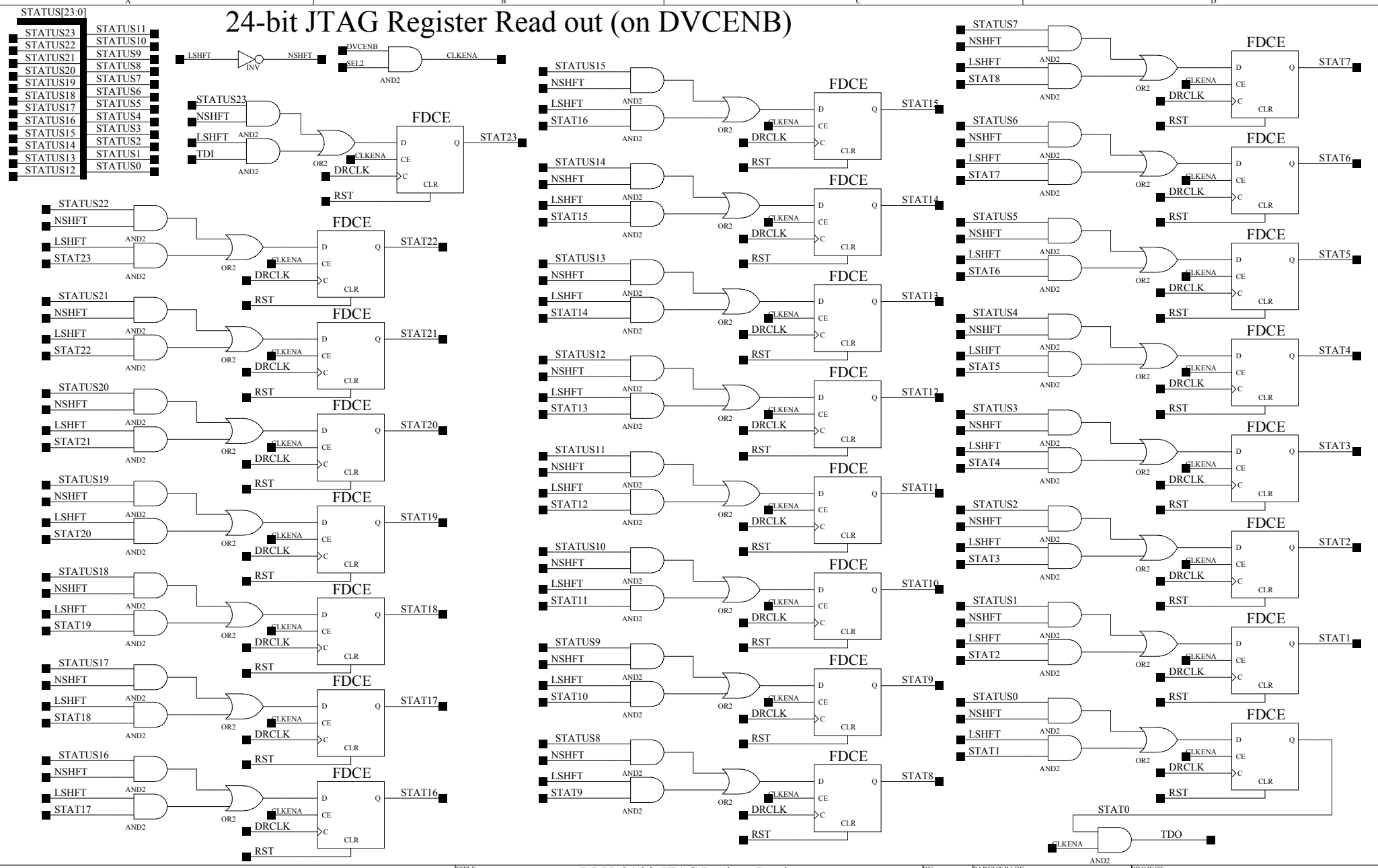
16-bit JTAG Register Read out (on DVCENB)

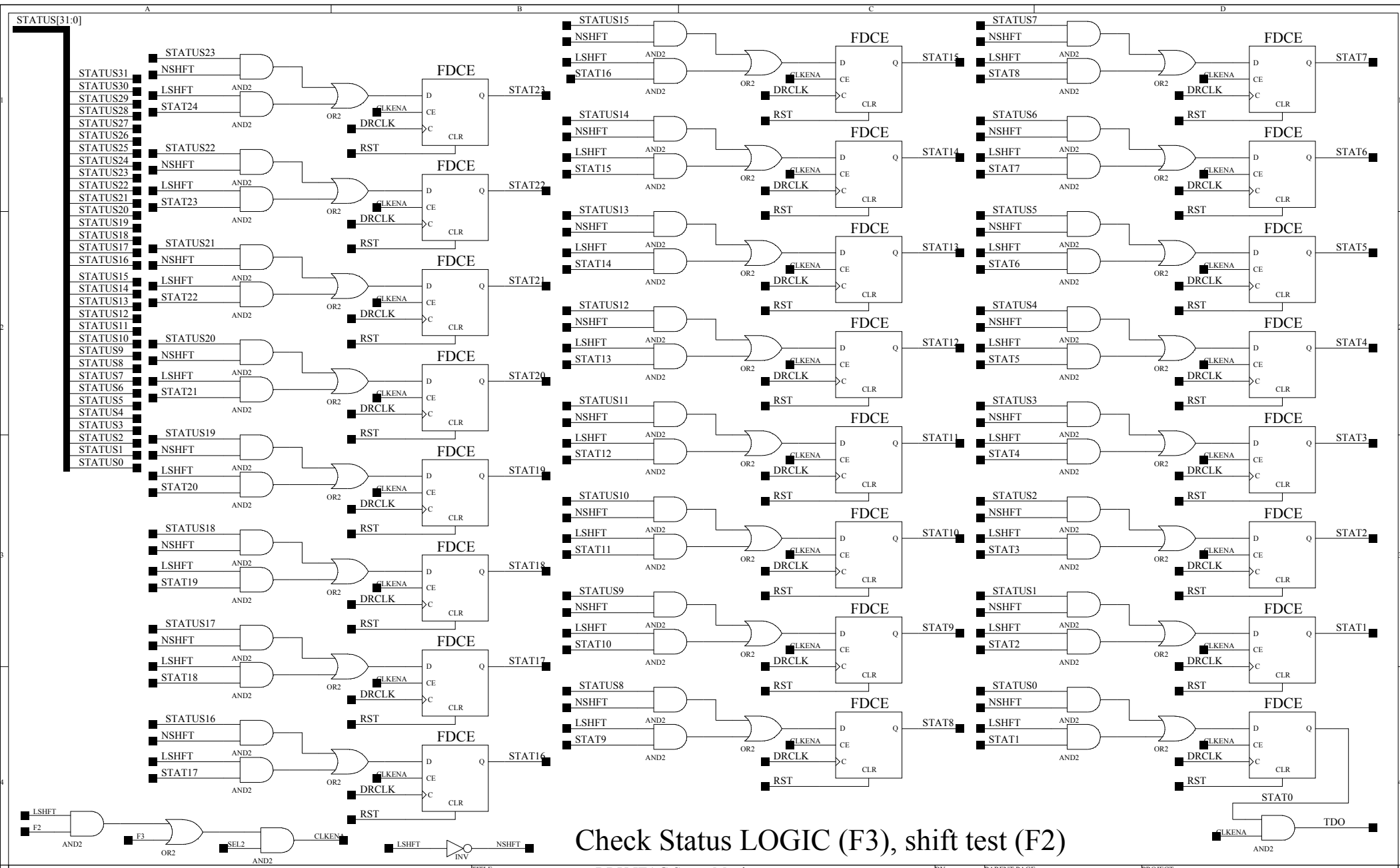
STATUS[15:0]

- STATUS15
- STATUS14
- STATUS13
- STATUS12
- STATUS11
- STATUS10
- STATUS9
- STATUS8
- STATUS7
- STATUS6
- STATUS5
- STATUS4
- STATUS3
- STATUS2
- STATUS1
- STATUS0

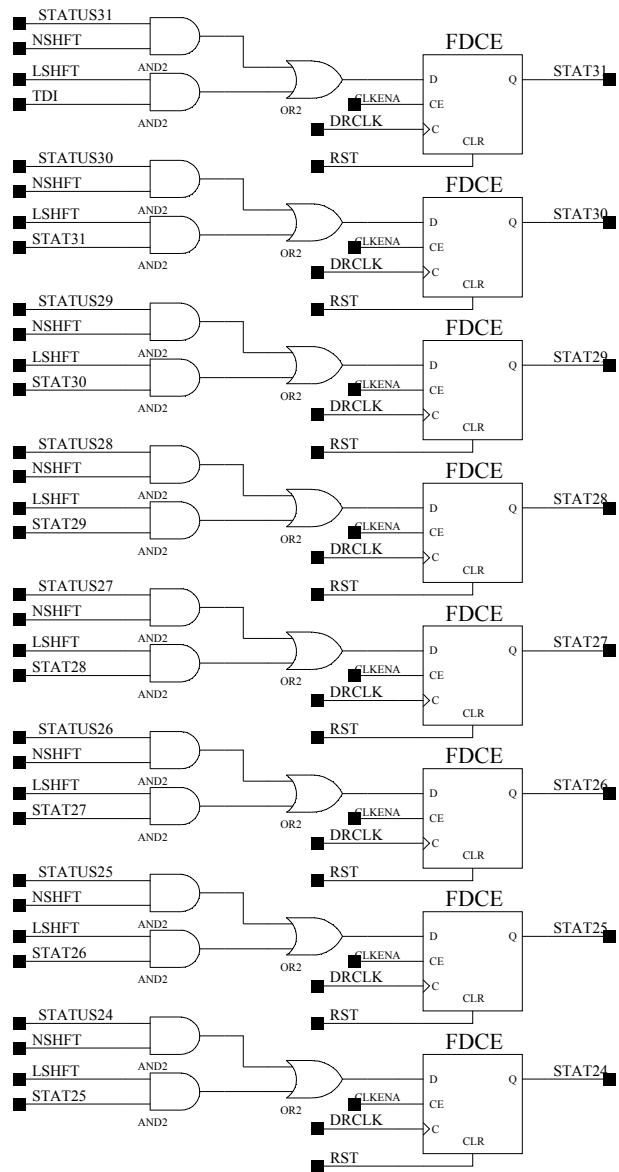


24-bit JTAG Register Read out (on DVCENB)





Check Status LOGIC (F3), shift test (F2)

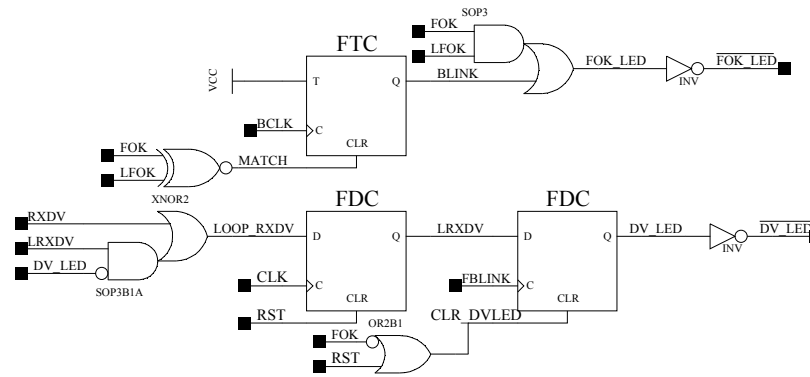


FOK LED

- LIT == Link is alive and well
- BLINK == Link not ready
- OFF == Link not present

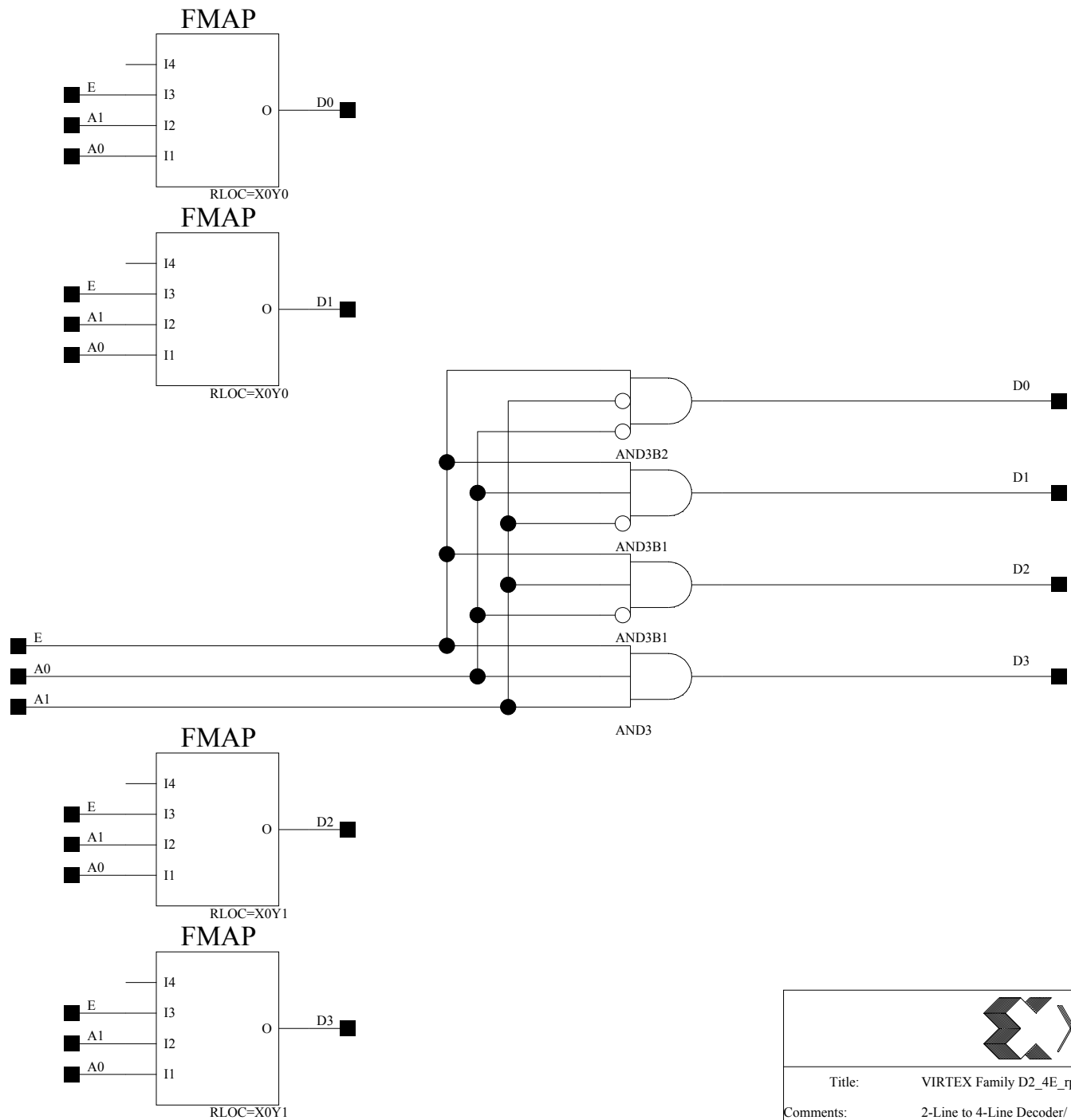
DAV LED


- LIT == Active Data Xmit
- OFF == No data to Xmit

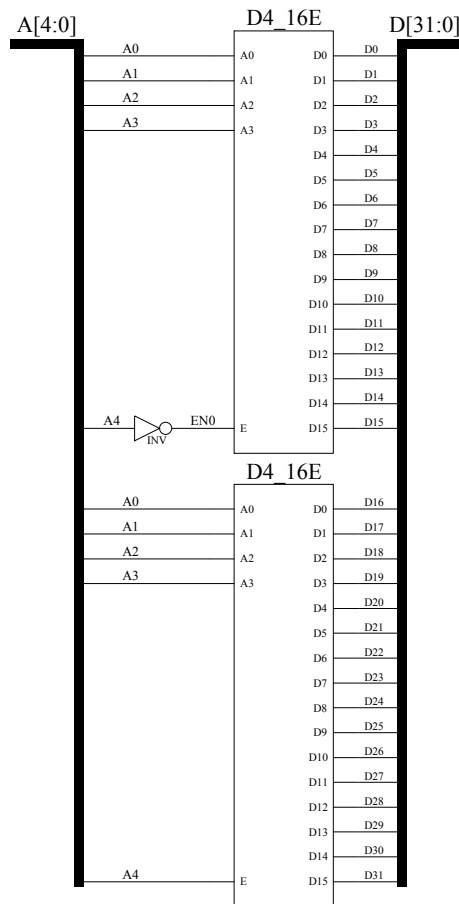


JRG

Title:	FIBERLED	
Comments:	Custom LED Slow-Blink Control for Fiber Inputs	
Date:	27th January 2004	Ver: 1
Sheet Size: B		Rev: A



		JRG
Title:	VIRTEX Family D2_4E_rpm Macro	
Comments:	2-Line to 4-Line Decoder/ Demultiplexer w/ Enable, RPM	
Date:	11th November 2003	Ver: 1
Sheet Size:	A	Rev: A



Title: VIRTEX Family Decode 32E Macro		JRG
Comments: 5-bit to 32-bit Decoder		
Date: 30th September 2003	Ver: 1	
Sheet Size: B	Rev: A	

RPM_GRID=GRID



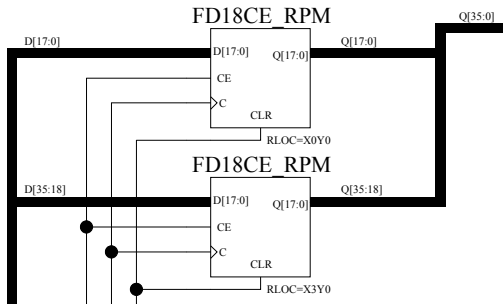
D[17:0]

- CE
- C
- CLR

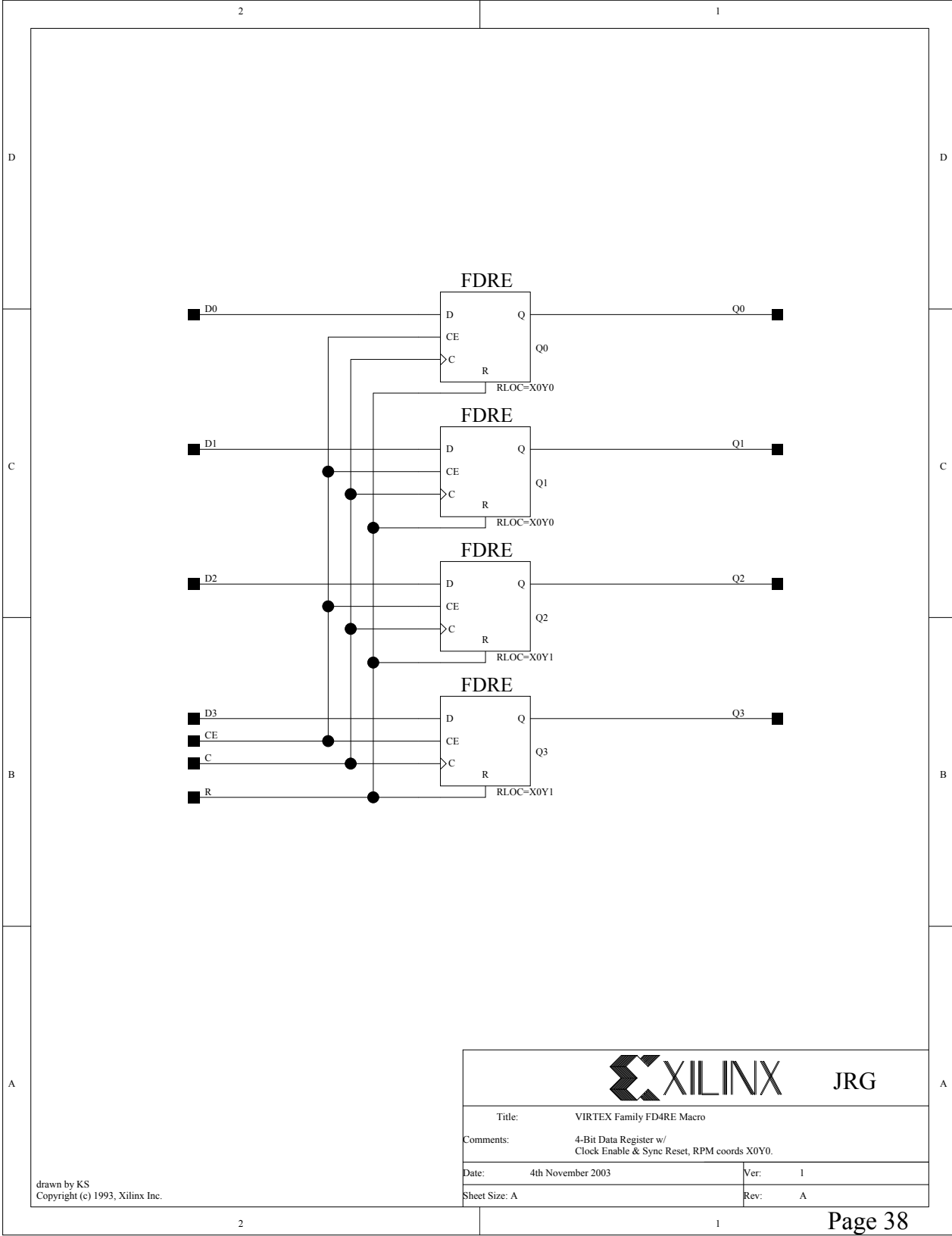


Title:	VIRTEX Family FD18CE_RPM Macro		JRG
Comments:	18-Bit Data Register w/ Clock Enable & Asynchronous Clr, GRID Coords X0Y0-X0Y8		
Date:	29th October 2003	Ver:	1
Sheet Size:	B	Rev:	A


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Title: VIRTEX Family FD36CE_RPM Macro		JRG
Comments: 36-Bit Data Register w/ Clock Enable & Asynchronous Clr, GRID Coords X0Y0-X3Y8		
Date: 30th October 2003	Ver: 1	
Sheet Size: B	Rev: A	

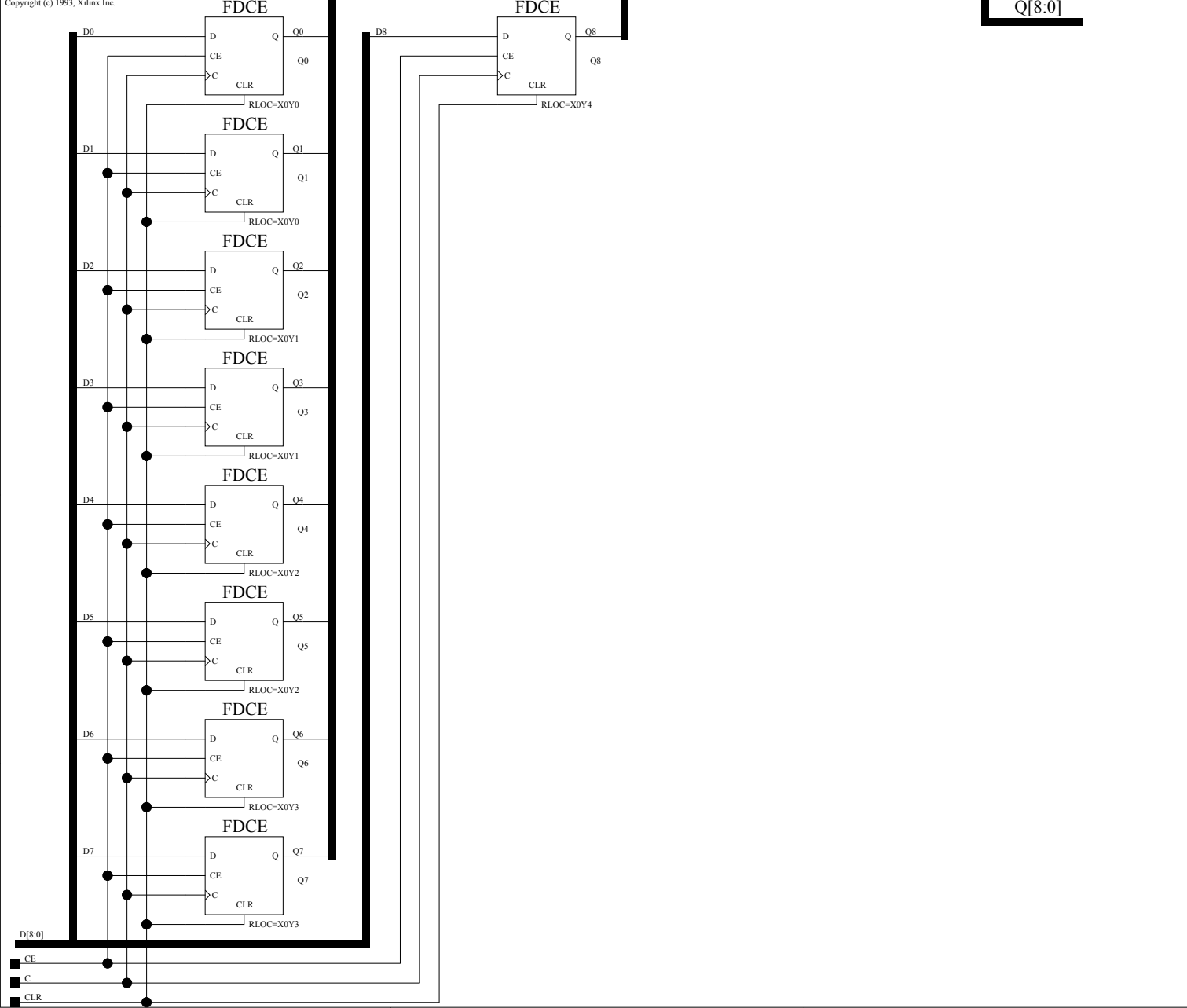


drawn by KS
Copyright (c) 1993, Xilinx Inc.

		JRG
Title: VIRTEX Family FD4RE Macro		
Comments: 4-Bit Data Register w/ Clock Enable & Sync Reset, RPM coords X0Y0.		
Date:	4th November 2003	Ver: 1
Sheet Size:	A	Rev: A

drawn by KS
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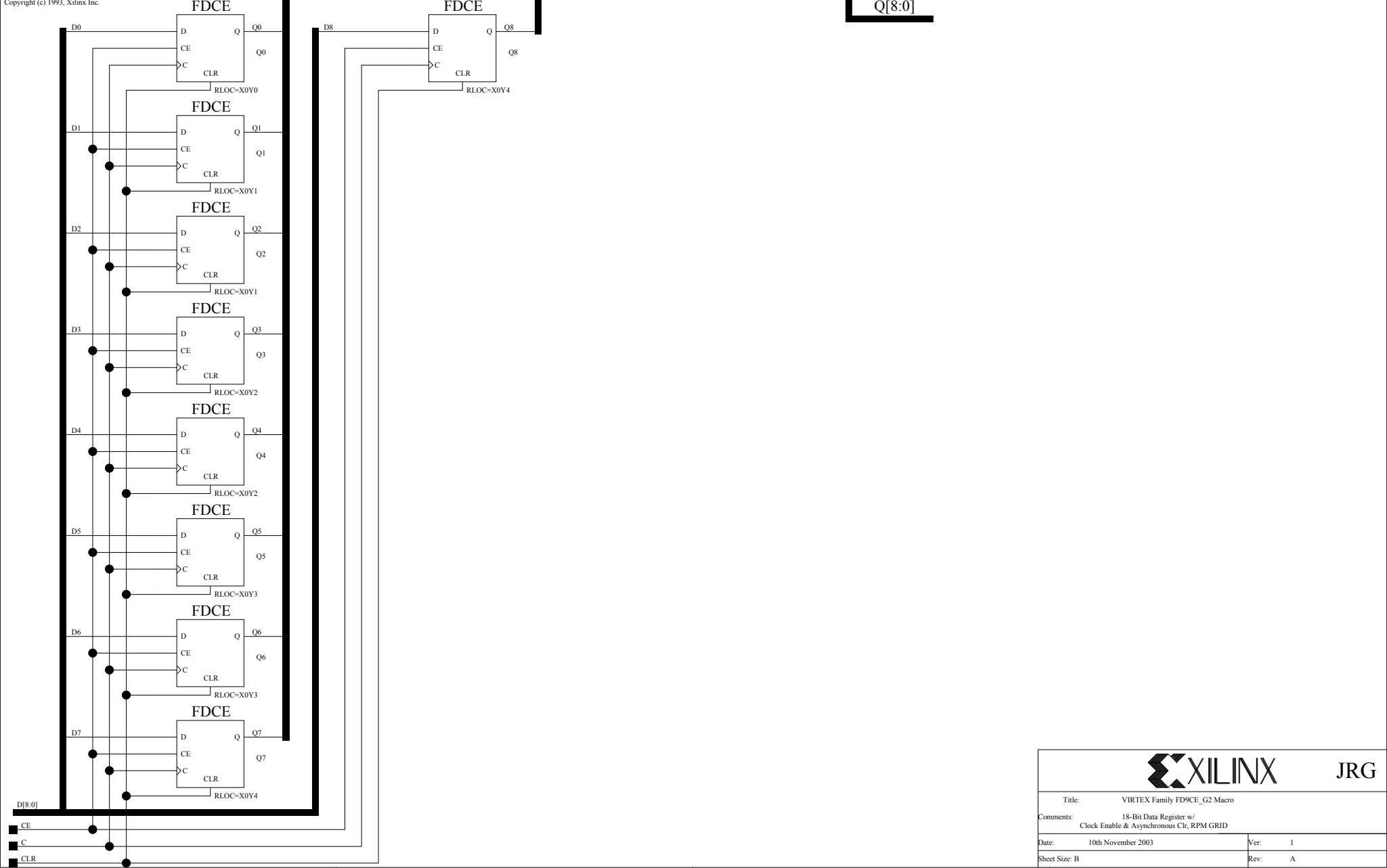
RPM_GRID=GRID



		JRG
Title: VIRTEX Family FD9CE_G Macro		
Comments: 18-Bit Data Register w/ Clock Enable & Asynchronous Clr, RPM GRID		
Date: 10th November 2003	Ver: 1	
Sheet Size: B	Rev: A	

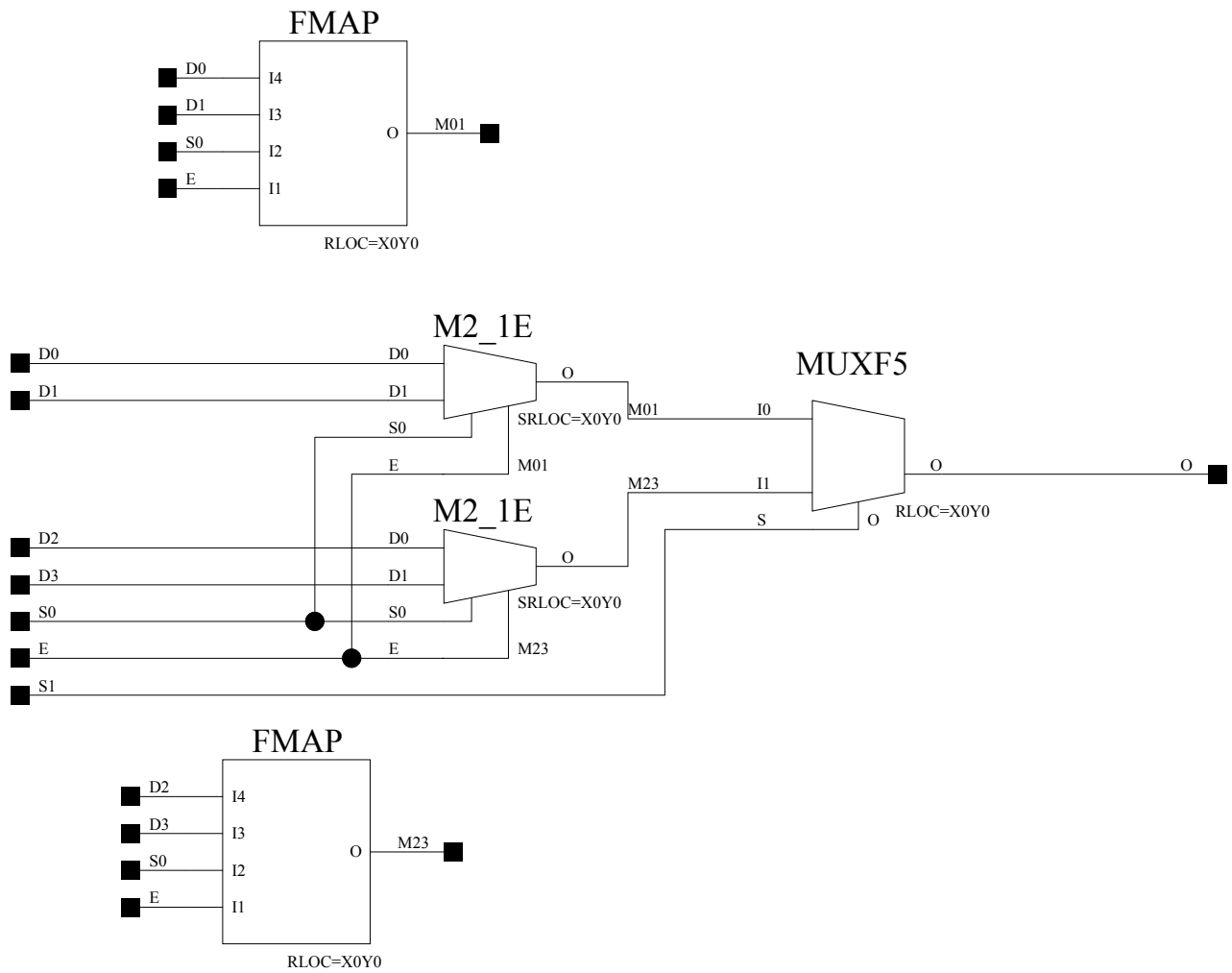
drawn by KS
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RPM_GRID=GRID



JRG

Title: VIRTEX Family FD9CE_G2 Macro	
Comments: 18-Bit Data Register w/ Clock Enable & Asynchronous Clr, RPM GRID	
Date: 10th November 2003	Ver: 1
Sheet Size: B	Rev: A

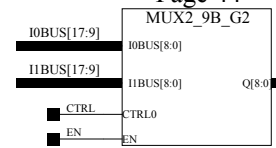


Title:	VIRTEX Family M4_1E_RPM Macro		
Comments:	4-to-1 Multiplexer with Enable		
Date:	31st October 2003	Ver:	1
Sheet Size:	A	Rev:	B

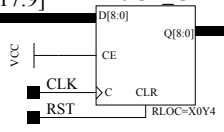
IOBUS[17:0]
IOBUS[17:9]
IOBUS[8:0]

IIBUS[17:0]
IIBUS[17:9]
IIBUS[8:0]

Page 44

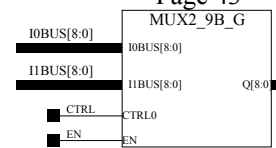


Page 40

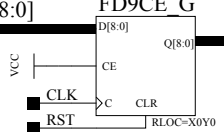


Q[17:0]

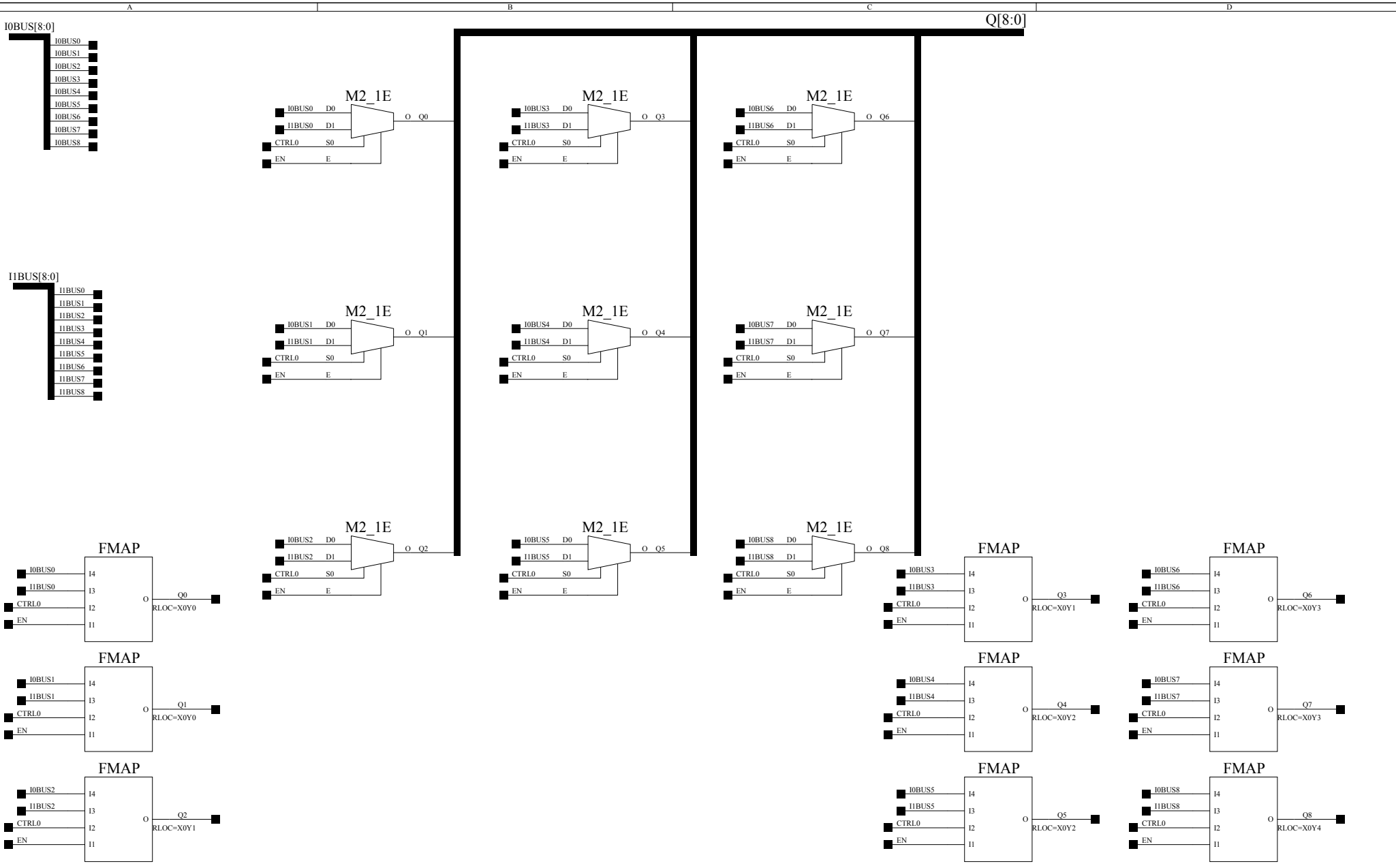
Page 43



Page 39

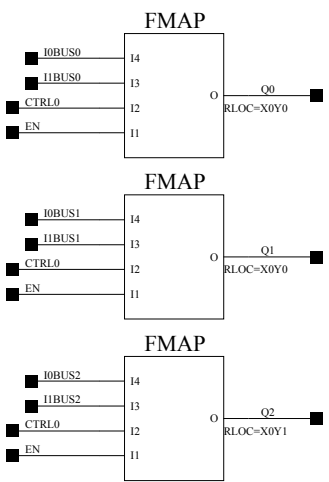


Q[8:0]

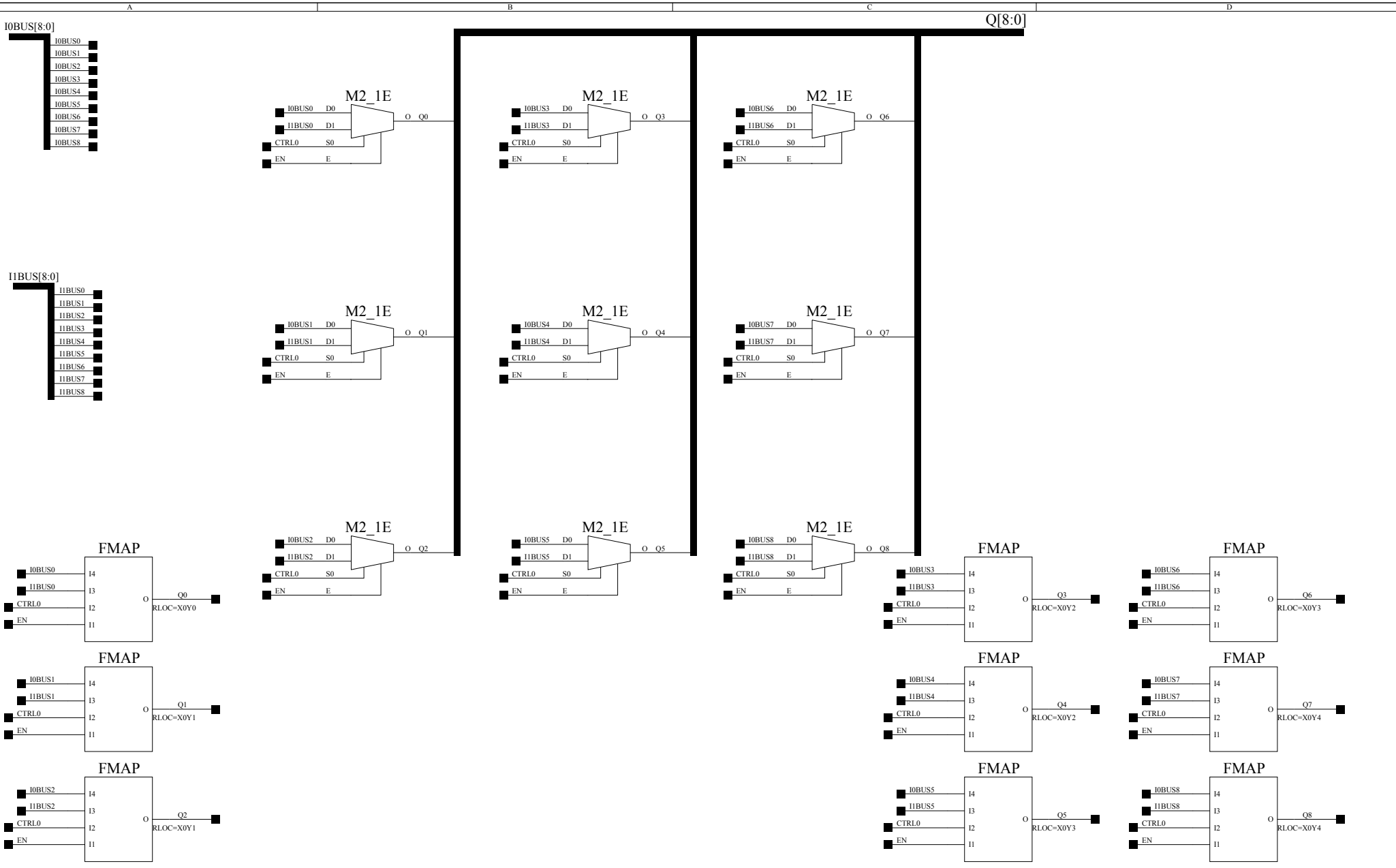


IOBUS[8:0]
 IOBUS0
 IOBUS1
 IOBUS2
 IOBUS3
 IOBUS4
 IOBUS5
 IOBUS6
 IOBUS7
 IOBUS8

I1BUS[8:0]
 I1BUS0
 I1BUS1
 I1BUS2
 I1BUS3
 I1BUS4
 I1BUS5
 I1BUS6
 I1BUS7
 I1BUS8

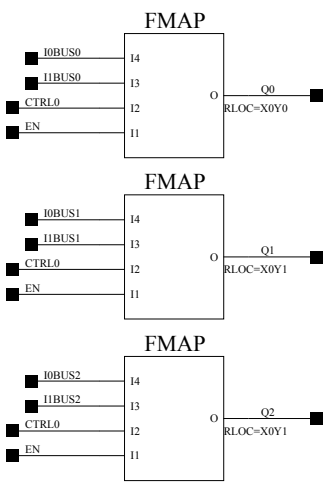


Q[8:0]



IOBUS[8:0]
 IOBUS0
 IOBUS1
 IOBUS2
 IOBUS3
 IOBUS4
 IOBUS5
 IOBUS6
 IOBUS7
 IOBUS8

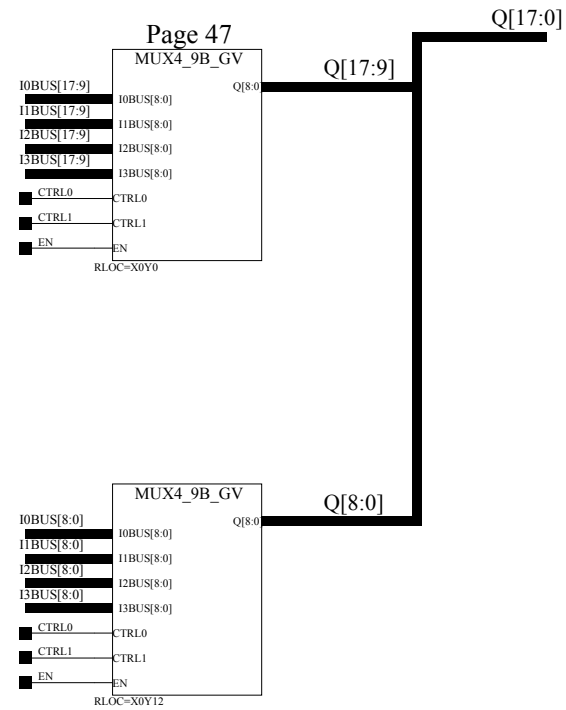
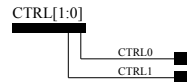
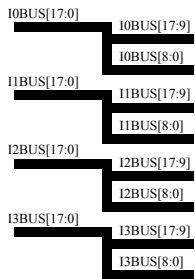
I1BUS[8:0]
 I1BUS0
 I1BUS1
 I1BUS2
 I1BUS3
 I1BUS4
 I1BUS5
 I1BUS6
 I1BUS7
 I1BUS8

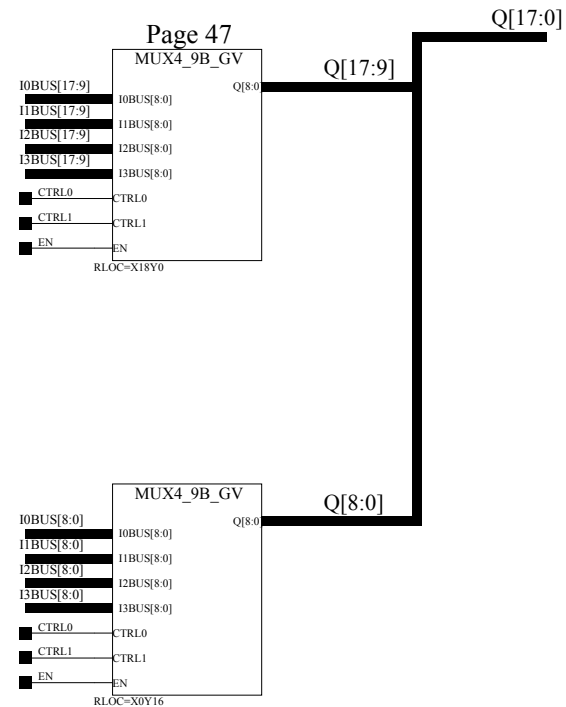
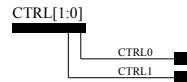
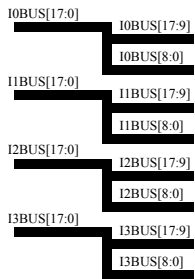


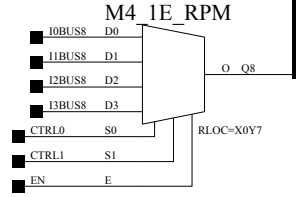
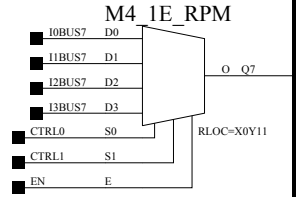
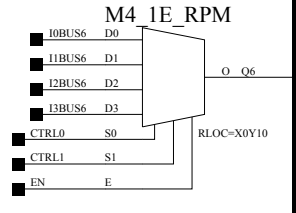
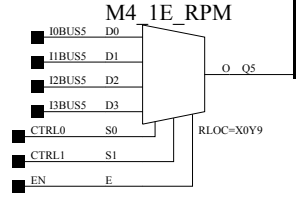
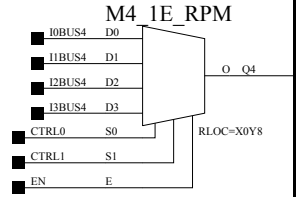
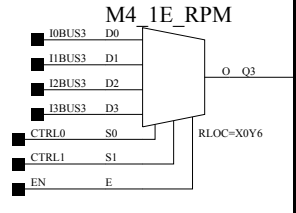
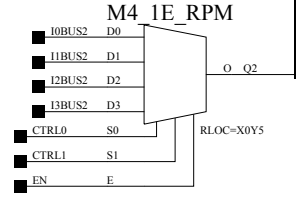
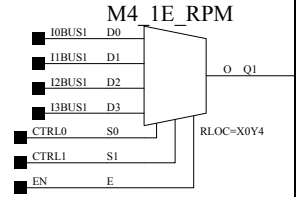
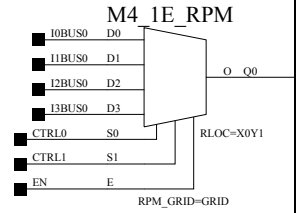
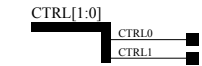
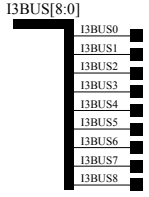
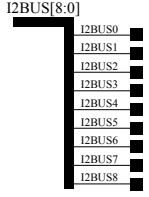
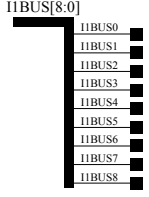
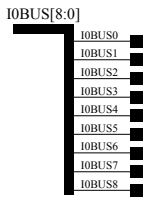
TITLE 9-bit MUX for 2 9-bit Inputs, w/Enable. RLOC=GRID
 DDU Input Controller Logic
 CMS CSC Electronics

BY JRG
 DATE 1-27-2005_10:43

PARENT PAGE 42
 PROJECT D785D
 FILE MUX2 9B G2 .1
 PAGE 44

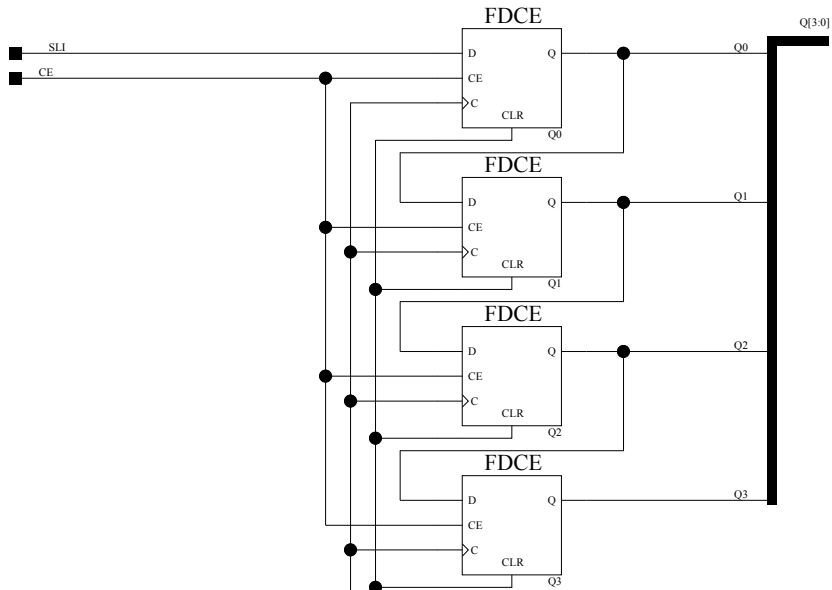






Q[8:0]

drawn by KS
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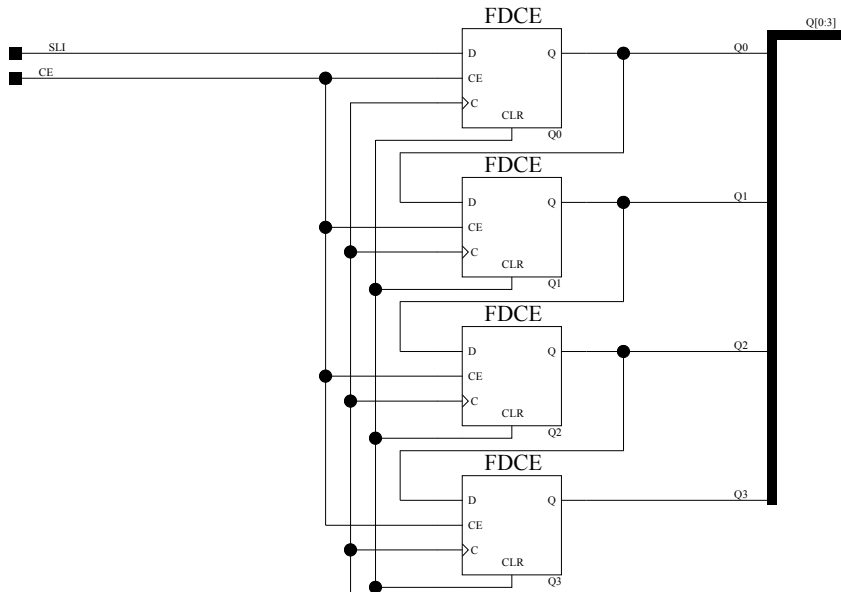
■ C
■ CLR



JRG

Title:	VIRTEX Family SR4CE Macro	
Comments:	4-bit Serial-In Parallel-Out Shift Register w/ Enable and Async Clr	
Date:	3rd October 2003	Ver: 1
Sheet Size: B		Rev: A

drawn by KS
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■ C
■ CLR



Title:	VIRTEX Family SR4CE_R Macro	JRG
Comments:	4-bit Serial-In Parallel-Out, REVERSED ORDER on OUTPUT BUS! Shift Register w/ Enable and Async Clr	
Date:	3rd October 2003	Ver: 1
Sheet Size: B		Rev: A